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VeryFastCCD: a high frame rate soft X-ray detector

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Direct X-ray detection in silicon has been transformative for scattering experiments in biology and materials science. While bump-bonded hybrid pixels have been attractive for hard X-ray detection, the challenge for single photon soft X-ray detection is sufficiently low noise. CCD structures on thick, high-resistivity silicon have been successfully used as sensors over the range of soft to hard X-rays at storage rings and FELs. The VeryFastCCD is a high frame rate, column-parallel CCD sensor with 48 μm pixels. Combined with 256-channel custom readout ASICs, frame rates of 5–10 kHz have been achieved with readout noise as low as 20 e and full-well capacity >4 × 10^5 e/pixel. Thin (10 nm and 100 nm) entrance window contact processes have also been developed which provide >85% quantum efficiency for 285 eV X-rays. Systems are currently being developed for several beamlines at the upgraded Advanced Light Source.

KEYWORDS

soft X-ray detector, direct-detection CCD, readout ASIC, thin contacts, sensors

1 Introduction

The charge-coupled device [1] (CCD) has been a backbone of scientific imaging for 50 years. The CCD, together with a fiber-coupled phosphor, forms a detector that has been used for decades in X-ray and electron microscopies: incident radiation creates optical photons by ionization, which are transported by a fiber optic light guide onto a CCD. Removing the phosphor and directly detecting X-rays in CCDs has proven over the last ~15 years to be attractive for storage ring and free electron laser X-ray light sources, since compared to indirect detection in a phosphor, direct detection provides much better spatial resolution (scintillation photons are emitted in all angles) along with higher detection efficiency and signal/noise (since it takes 3.6 eV to create an e/h pair in silicon vs. 10s of eV to create a scintillation photon).

Key considerations for direct X-ray detection in silicon are the thickness of the sensitive volume and the amount of dead material in front of the sensitive volume. Since the X-ray absorption length λ, in silicon is a strong function of energy–λ = 40 nm at 100 eV, λ = 130 μm at 10 keV and λ = 23 mm at 100 keV–high efficiency X-ray detection is practical up to ~10 keV (100s of μm thick sensitive volume). To maintain high spatial resolution and charge collection efficiency, a fully-depleted sensitive volume is desired (so that the ionization charge is collected by drift to a collection diode rather than by diffusion into all angles). This requires that the sensitive volume is of sufficiently high resistivity that it can be depleted by the application of a substrate voltage below the breakdown voltage [2]. To apply the substrate voltage, an entrance contact is required, and for operation to the lowest energies, the

entrance contact must be thin enough that the incident X-rays are not all absorbed in the contact.

Due to their lower noise compared to hybrid pixel detectors, direct detection CCDs are particularly attractive for soft X-rays (E<2 keV). CCDs are comparatively slow, however, since the CCD structure is based on shifting charge from pixel-to-pixel–rather than reading each pixel directly. In the simplest case, all pixels are individually shifted and digitized through a single readout port. It thus takes time $t_{FRAME} = \frac{N}{f}$ to read out N pixels at a readout frequency f. As source brightness increases, less time is required to collect the same number of photons. Similarly, t_{FRAME} sets the temporal resolution. For these reasons, reducing t_{FRAME} is required as sources improve, and it can be reduced by adding more readout ports, so that $t_{FRAME} = \frac{N}{fm}$ for m ports. Direct X-ray detection CCDs, on thick high-resistivity substrates, with large numbers of readout ports have been developed: such as the pnCCD [3], the FastCCD [4], and the MPCCD [5].

Our prior work is the FastCCD which is a >120 Hz frame rate, megapixel CCD optimized for soft X-rays that has one readout port for every 10 columns. Below we describe the VeryFastCCD, which is the natural follow-on to the FastCCD as a general-purpose soft X-ray scattering detector–increasing speed by having one readout port for every column. Compared to the FastCCD, the VeryFastCCD is much faster, with a 5 kHz frame rate for a 512 × 512 pixel sensor. As described below, through the use of a multi-gain gated integrator, it is possible to tune the full-scale signal vs. noise both by gain selection and variation of integrator timing.

2 CCD design

The metal-oxide-semiconductor (MOS) CCD structure consists of polysilicon gates on a gate oxide above a silicon substrate. The most common CCD pixel, as illustrated in Figure 1A, has three separate gates (φ_1, φ_2,φ_3). By manipulating the voltages on the gates, charge can be stored (integrated) or shifted from pixel-to-pixel. The simplest CCD detector, Figure 2A has a 2D array of imaging pixels and a 1D array of pixels used as an output shift register. In operation (1) an image is exposed, (2) the first row is shifted into the output shift register via the Array Transfer Gate (ATG), (3) the output shift register pixels individually shifted out and captured, (4) and the next row is then transferred to the output shift register. In most CCDs, an MOS source-follower is used to drive the signal off the sensor. An Output Transfer Gate (TG), Figure 2B, collects the charge from the output shift register, and pushes it over a barrier potential (OG) onto the gate of the source-follower. The voltage on the gate is then $V = \frac{Q}{C_G}$, where C_G is the total capacitance of the source-follower gate. A RESET transistor is used to remove charge from the previous sample before the next sample is presented. The digitized pixel value is thus the *voltage* difference between the RESET and SIGNAL levels.

To increase the frame rate of the CCD readout, additional parallelism is used. The simplest is reading out from both sides of the CCD: The 4-port CCD (Figure 2C) is a trivial modification of the single port CCD (Figure 2A). Incorporating more output ports becomes more challenging, since the output shift registers must be modified in order to provide the space required for the output stage. Numerous CCDs with more than 4 readout ports (Figure 2D) have been produced: for example, the FastCCD has one port for every

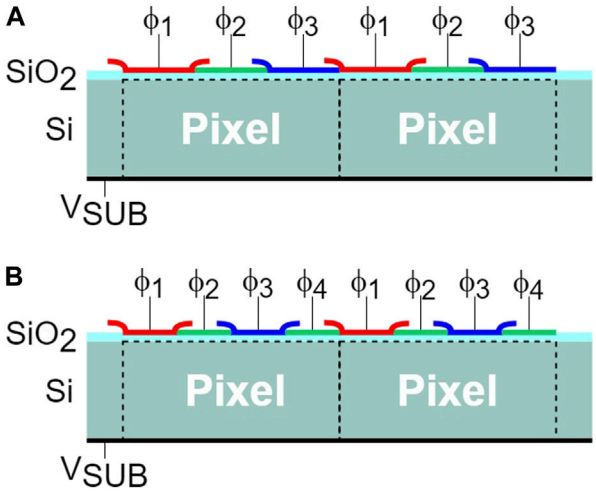

FIGURE 1
3- and 4-phase CCD pixels. Charge moves left-to-right or right-to-left depending on the sequence of clocks, $\varphi_{1\text{-}4}$.

10 columns. The VeryFastCCD is a fully-column-parallel CCD (Figure 2E)—which means that every CCD column has a readout port. Because there is not enough space for an output stage (Figure 2B) for each column, the VeryFastCCD directly outputs a *charge* rather than a *voltage*.

The FastCCD and VeryFastCCD are fabricated in the Dalsa 2.5 μm, triple poly, triple metal process[1] on very high resistivity n-type silicon with buried p channels, using a method developed at LBNL(2). For CCDs operating at high speed, the long polysilicon gates must be "metal strapped"—that is covered with metal lines, which are ~1/1000 the resistivity of the polysilicon, and connected as frequently as possible to the polysilicon. For the FastCCD, we chose to use a single metal layer, and designed a 30 μm, 3-phase (Figure 1A) pixel. For the VeryFastCCD, we chose to use 3 metal layers. Since here a charge, rather than voltage, output, is used, parasitic charge injection (through substrate or other capacitive coupling to the output) can present large transients to any downstream amplifier, and potentially saturate the amplifier output. For this reason, we designed a 4-phase (Figure 1B) pixel in order to minimize parasitic charge injection from the CCD clocks since 4-phase clocking provides first order cancellation at each clock transition ($\varphi_3 = -\varphi_1$ and $\varphi_4 = -\varphi_2$). The larger the pixel, the larger the working distance between the sample and detector can be. The power needed to clock the CCD, though, is proportional to area. To balance the two the pixel size was set at 48 μm.

Since the CCDs are generally thick (100s of μm) to have good X-ray absorption, they are "self-shielding" against radiation damage when back-illuminated. Figure 3 shows the cumulative photon flux per pixel to accumulate 1 MRad in the gate oxide for a 200 μm thick sensor (the thickness of the VeryFastCCD). Measurements at *DORIS*

1 https://www.teledynedalsa.com/en/products/foundry/ccd/

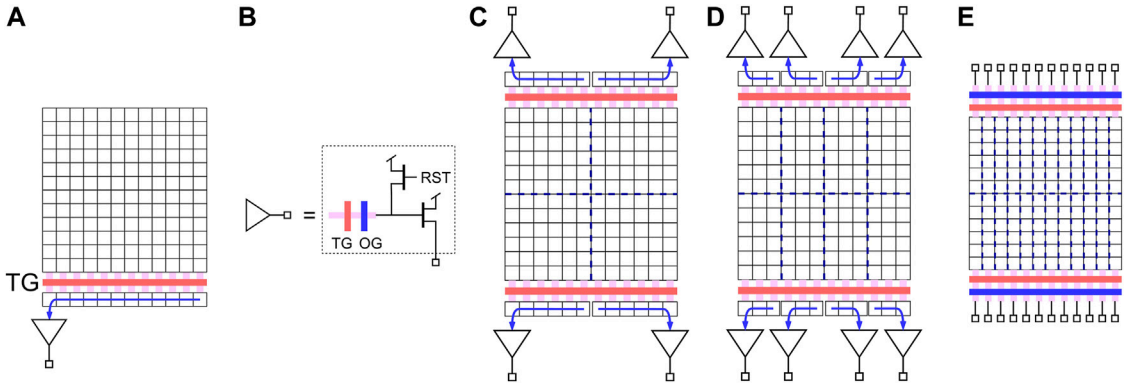

FIGURE 2
CCD structures with increasing parallelism.

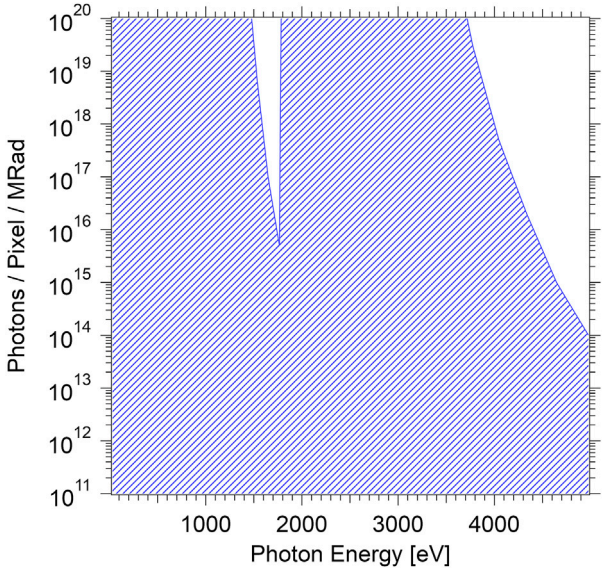

FIGURE 3
Calculated number of photons per VeryFastCCD pixel required to deposit 1 MRad in the CCD gate oxide as a function of energy.

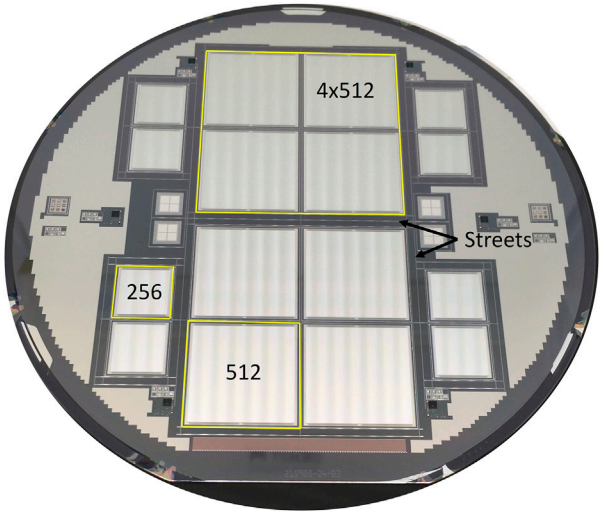

FIGURE 4
A 150 mm VeryFastCCD production wafer, containing 8 256 × 256 and 8 512 × 512 CCDs. Four 512 × 512 CCDs can be diced out as a single 1024 × 1024 CCD.

with hard X-rays on the FastCCD indicate that 1 MRad will induce sufficient leakage current to limit performance with 10 ms exposure times. This suggests no radiation damage for soft X-ray storage ring use, nor at FELs (under normal circumstances).

The VeryFastCCD uses all of the same sensor fabrication and processing methods as the FastCCD. A fabricated wafer is shown in Figure 4. Both 256 × 256 pixel and 512 × 512 devices are present. The 512 devices are arrayed in such a way that four of them can be diced to create a 1024 × 1024 sensor with 90% fill factor.

2.1 Thin entrance windows

High efficiency detection of soft X-rays requires a back side illuminated CCD with minimal dead material between the incident X-ray and the active silicon. To deplete the thick active volume, a voltage must be applied to the back (X-ray entrance) side of the CCD (V_{SUB} in Figure 1). A very thin contact layer is thus required. Soft X-ray detection also requires very low noise, hence the contact must ensure minimal leakage current. While Schottky barrier contacts exhibit a very thin dead layer, they result in leakage currents that are high for soft X-ray applications. An ohmic contact is thus preferred and used here.

The technique initially developed at LBNL for fabricating thick, high resistivity CCDs is to use doped polysilicon to form the thin X-ray entrance contact [6]. However, polysilicon deposition requires temperatures that are too high to be compatible with aluminum metallization. When this technique is used, wafers are (a) implanted and gates formed at the factory (b) thinned and then the doped polysilicon contact is deposited at LBNL (c) final metalization is performed at LBNL. As the LBNL metal process has only one layer, and larger-sized vias than the triple-metal Dalsa process, having a

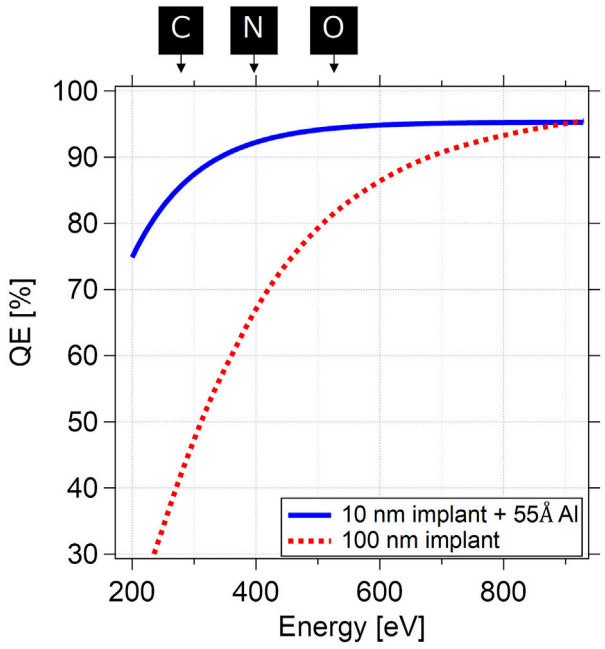

FIGURE 5
Quantum Efficiency for 10 and 100 nm contacts measured at ALS Beamline 6.3.2. Shown are fits of the measurements. Energies of the carbon, nitrogen and oxygen K-edges are highlighted.

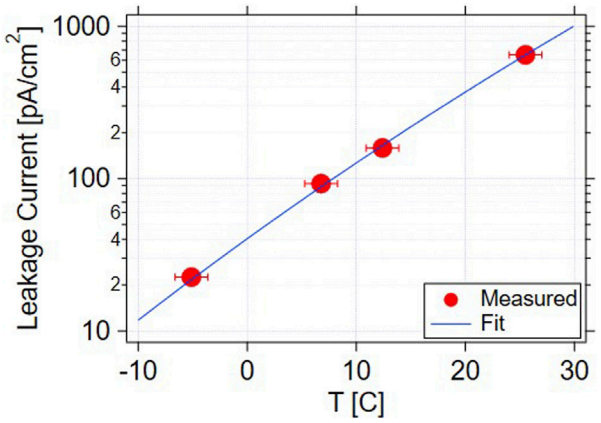

FIGURE 6
Leakage current for 200 μm thick CCD with 10 nm contact as a function of temperature. The points are measured values, and the curve is a fit as described in the text.

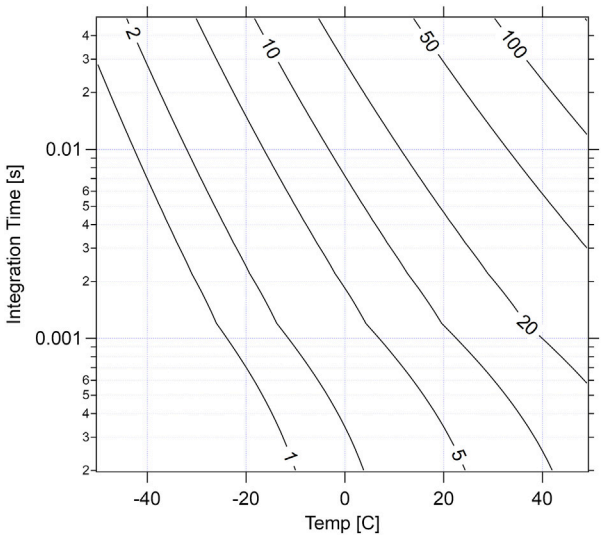

FIGURE 7
Contour plots of added noise [e] as a function of temperature and integration time.

low temperature process that can be performed on fully metallized wafers (a) simplifies the CCD fabrication process since all of the steps except the thin contact fabrication can first be performed at the foundry (b) enables the use of more metal layers, which improves the high-speed CCD clock distribution.

The thin X-ray entrance contact is then added to the device at LBNL as the last processing step. To this end we have developed two low temperature thin contact processes: (1) implantation followed by low temperature annealing (~100 nm thick), and (2) molecular beam epitaxy (MBE) (~10 nm thick). The MBE contact has the added benefit of being even thinner than the doped polysilicon contact (~30 nm thick).

The ion implanted contact generally finds use for applications in which the energies of the incident photons are 500 eV or more. This contact has the advantage of being relatively simple to fabricate. The MBE contact is used to extend the reach to lower energies.

We have evaluated the quantum efficiency (QE) of both of these types of contacts on numerous samples (CCDs and diodes) using the metrology beamline[2] (6.3.2) at the Advanced Light Source [7]. Figure 5 shows the averages of QE measurements for the two types of contacts. Figure 6 shows the leakage current for the 10 nm contact on a 256 × 256 VFCCD as a function of temperature, T. The temperature dependence of the leakage current is modeled [8, 9] as $I_L \propto T^n e^{-E/2kT}$, usually with n = 2, and effective energy $E = E_g + 2\Delta$ ($E_g = E_0 - \alpha T$ is the temperature dependent bandgap of Silicon, and Δ arises from the presence of a charge-generating trap). The curve in Figure 6 is a fit to the model above, with Δ = 0.11 eV. The low value of Δ, and of the overall leakage current, indicates that the MBE contact does not add significant leakage current.

While the VeryFastCCD has a high frame rate, different experimental conditions necessitate different exposure times. A key system design parameter is the camera operating temperature, and this is determined by the noise added by leakage current: that added noise is proportional to $\sqrt{I_L T_{EXP}}$, where I_L is the leakage current, and T_{EXP} is the total exposure time (which for a given row of pixels is the total time that the row can collect leakage current: the image exposure time plus the time needed to shift out the charge from that row). Figure 7 shows noise contours of *added* noise due to the leakage current shown in Figure 6 (in electrons, where 3.6 eV of absorbed energy is required to create one electron/hole pair in silicon). For FEL

2 https://cxro.lbl.gov/als632/

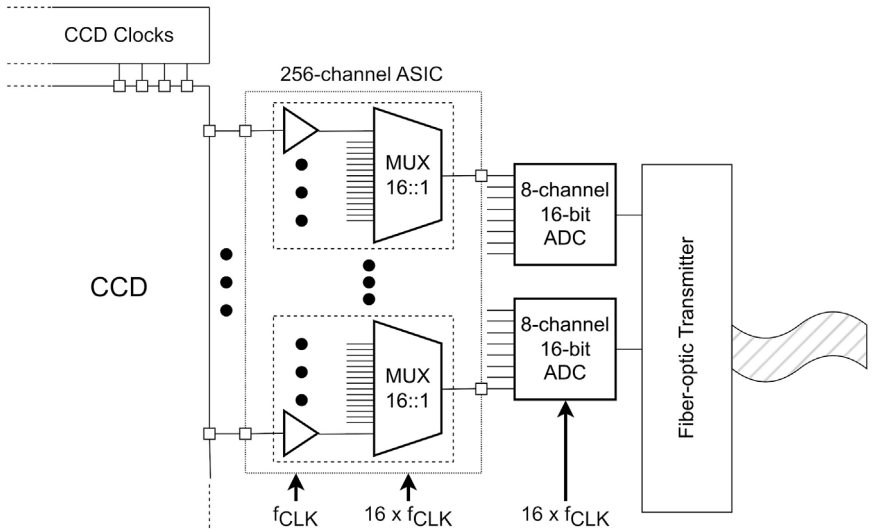

FIGURE 8
VeryFastCCD system overview: 256 CCD outputs are processed by a single VASE ASIC, whose outputs are digitized by 16 ADCs. Output data are transmitted over fiber optic ribbons.

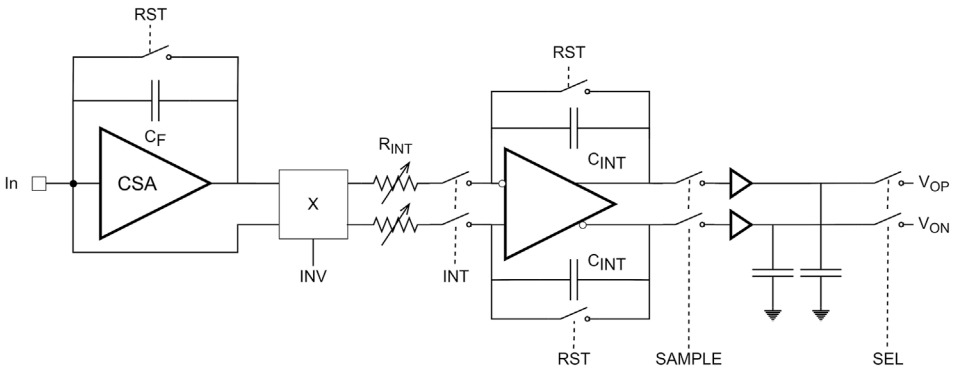

FIGURE 9
VASE2 Front end, with charge-sensitive amplifier, programmable integrator and output sample/hold.

applications, operation near room temperature is possible. For storage ring applications, the operating temperature will depend on the longest exposure time required, and the desired total noise, but operation at −20 °C should cover most use cases.

3 Data acquisition

Data acquisition is illustrated in Figure 8. The CCD signal is read out on two sides (Figure 2E), and the other two sides are used to provide clocks. A 256-channel integrated circuit VASE2 has been developed to read out the charge from the VeryFastCCD. (A prior version VASE1 is described in [10] and was subsequently simplified for VASE2 by removing a ΣΔ gain stage.). One VASE2 handles 256 CCD channels. Each CCD output is wire-bonded to a VASE2 input. Internally, VASE2 consists of 16 modules: each module has 16 front-end circuits and a 16:1 analog multiplexer. Each 8 of the VASE2 outputs are input to a commercial 8-channel, 16-bit ADC (TI ADS52J65). High-speed outputs from the ADCs are converted to optical signals, driven off the camera via fiber-optic ribbons.

For a 256 × 256 pixel camera, 2 VASE2 and 4 ADCs are used; for a 512 × 512 camera, 4 VASE2 and 8 ADCs are used, and this doubles again for a 1024 × 1024 camera.

A single VASE2 front end is shown in Figure 9. Similar to the FastCCD [11], the CCD signal is voltage-integrated, with a programmable gain and analog inversion to allow correlated double sampling (CDS). Unlike conventional CCDs, the VeryFastCCD signal is charge: VASE2 thus incorporates a charge-sensitive amplifier (CSA) with reset. As shown in Figure 10A, the RST switches are closed, removing charge on capacitors C_F and C_{INT}. The RST switches are then opened and switch INT is closed for time T_{INT}, and the reset level (V_{RST}) is integrated on capacitors C_{INT}. Switch INT is then opened, and CCD charge is presented to the CSA. The CSA output is $V_{SIG} = \frac{Q_{CCD}}{C_F} + V_{RST}$. The INV signal inverts the CSA output, so that

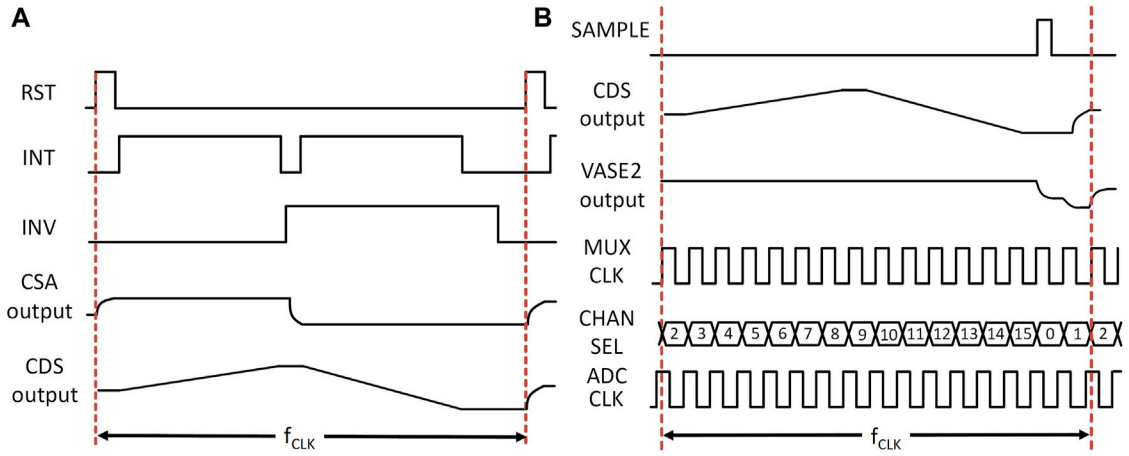

FIGURE 10
(A) VASE2 front-end timing **(B)** back-end timing.

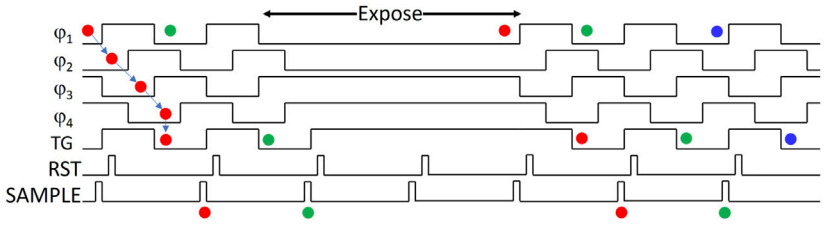

FIGURE 11
CCD and VASE front end timing: VASE clocks run continuously whereas CCD clocks are paused during signal integration. The colored circles represent pixel signals–as they are shifted by the CCD clocks and finally captured by the VASE SAMPLE signal.

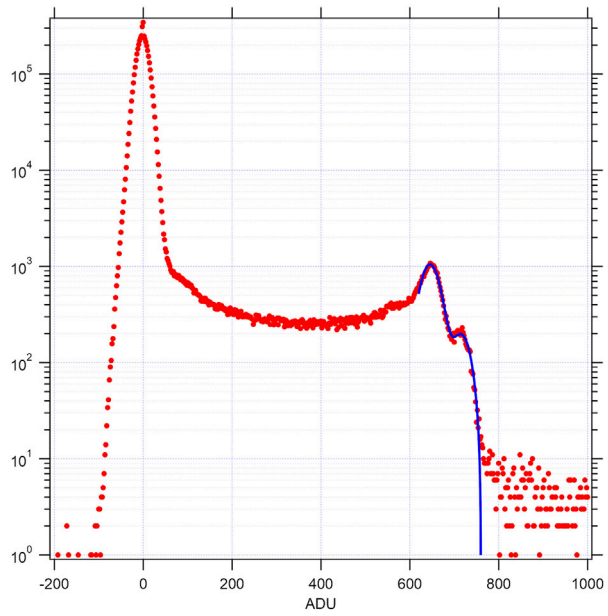

FIGURE 12
Spectrum (red) from all pixels illuminated by a ^{55}Fe source. The blue curve shows a fit to the combined K_α/K_β lines.

after the second integration the integrator output is $V_{INT} = \frac{1}{R_{INT}C_{INT}} \int_0^{T_{INT}} dt \left(\frac{Q_{CCD}}{C_F} + V_{RST} - V_{RST}\right)$. CDS thus removes the kTC noise associated with the CSA reset. Each front end contains 6 different values of R_{INT}, allowing a factor of approximately 5 in gain adjustment. Two versions of VASE2 were fabricated: a high gain (HG) version with $C_F = 14.5$ fF (including parasitic capacitance) and a low gain (LG) version with $C_F = 44$ fF. Further, as discussed below, additional gain adjustment is possible by changing T_{INT}.

The CCD row clocks and the VASE2 front end clocks (shown in Figure 10A) both operate at frequency f_{CLK}. The VASE2 back end and ADC operates at $16xf_{CLK}$. As illustrated in Figure 10B, each front end stores the value of V_{INT} for CCD row N on a sample-and-hold circuit when the SAMPLE command is issued. While the front end proceeds to acquire the signal from CCD row N+1, the 16 stored values for row N are multiplexed and digitized.

All of the measurements described below were performed with 256 × 256 CCD cameras. All of the CCDs were 200 μm thick, and operated at reverse bias of up to 80V. Several versions, equipped with HG and LG VASE2 chips, along with both 10 nm and 100 nm contacts have been tested. Cameras were also tested at the *COSMIC* beamline[3] at ALS [12], and the SXR beamline at LCLS I. The cameras

3 https://als.lbl.gov/beamlines/7-0-1-2/

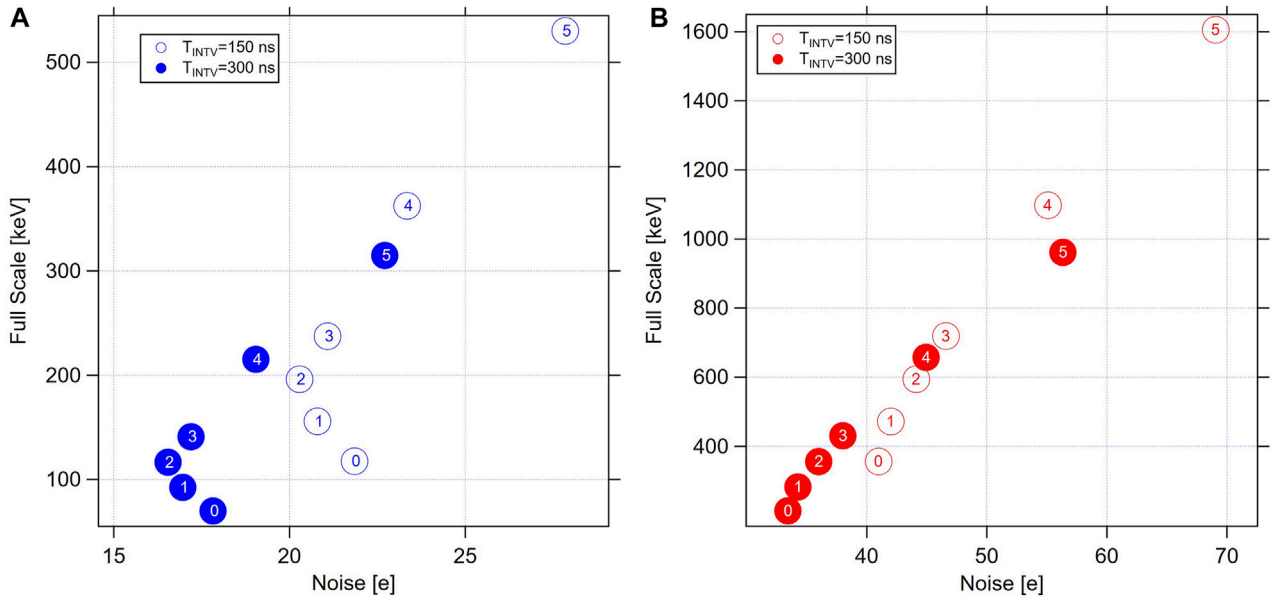

FIGURE 13
Maximum photon energy per pixel that can be recorded vs. Equivalent Noise Charge (ENC) for **(A)** VASE2 HG **(B)** VASE2 LG. The numbers in the circles are the gain setting, with 0 being the highest gain and 5 being the lowest. For both **(A,B)** values are shown for the nominal T_{INT} = **300** ***ns*** VASE integration time (solid circles) and for T_{INT} = **140** ***ns*** (open circles).

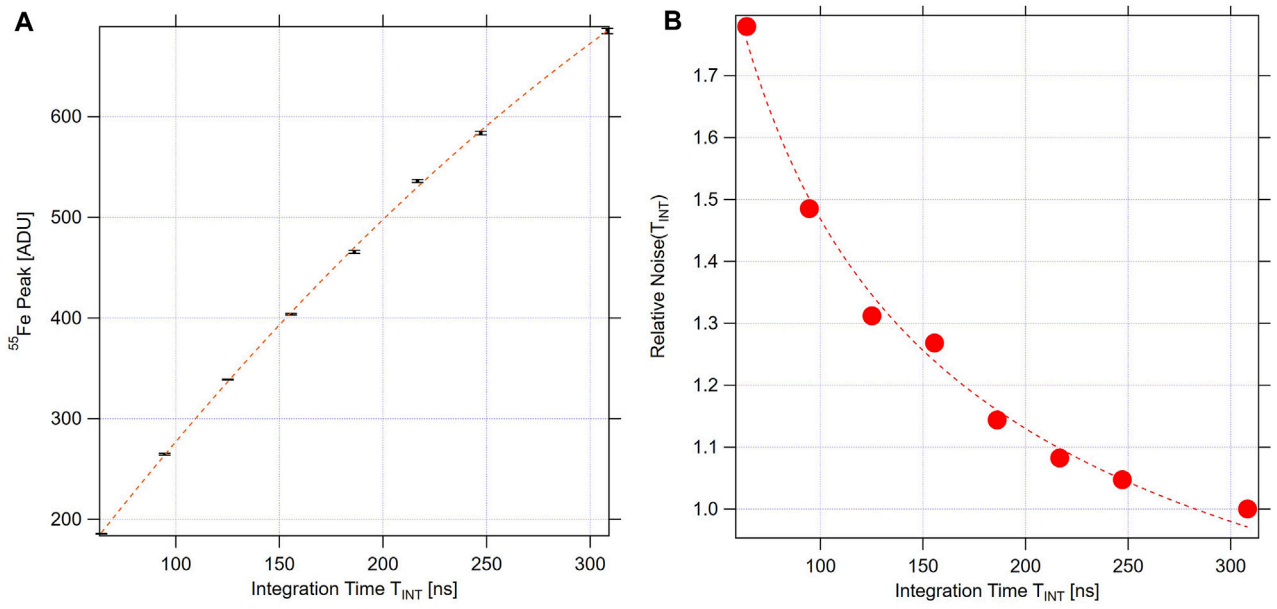

FIGURE 14
(A) ^{55}Fe peak position as a function of integration time. The curve is a quadratic fit. **(B)** Noise relative to nominal integration time of 305 ns. The curve is a fit to $1/\sqrt{T_{INT}}$.

were operated at f_{CLK} = 1.28 MHz, corresponding to up to 10,000 frames/s (equivalently 5,000 frames/s for a 512 × 512 device).

A timing diagram is shown in Figure 11. Clocks to the VASE2s and ADCs are continuous. CCD clocks also operate at f_{CLK} = 1.28 MHz. For storage ring applications, with signal integration times $\gg 1\,\mu s$, the CCD clocks are paused for an integral number of 1.28 MHz cycles. An FPGA-based data acquisition constructs images based on those ADC samples that are flagged as corresponding to charge readout. The FPGA operates at 256 x f_{CLK}, and programs the position and duration of each clock (CCD clocks, VASE clocks) using 8-bit registers to store values for when they should turn on and off.

4 Results

The digitized signal value is $\boldsymbol{G_{ADC}V_{INT}} = \boldsymbol{G_{ADC}G_{INT}}\frac{Q_{CCD}}{C_F}$ where $\boldsymbol{G_{ADC}}$ is the number of ADU per volt for the ADC, $\boldsymbol{G_{INT}} = \frac{T_{INT}}{R_{INT}C_{INT}}$ is the integrator gain, giving a nominal conversion gain $\boldsymbol{G_{ADC}G_{INT}}\frac{1}{C_F}$ (ADU/e). The actual conversion gain for the HG and LG versions of VASE2 at different gain settings was determined by illuminating the CCD with a ^{55}Fe source and constructing spectra of single pixels. Figure 12 shows such a spectrum: the conversion gain is determined from a combined Gaussian fit to the $K_\alpha K_\beta$ lines.

Figure 13A shows the maximum photon energy deposited in a pixel that can be recorded (before the ADC saturates) vs. the ENC for different gain settings of the high gain version of VASE2. Figure 13B shows the values for the low gain version of VASE2. On a given gain range, the full-scale divided by the noise is 10–12 bits (larger as the gain is reduced).

The digitized noise is $\hat{\sigma}_n[ADU] = G_{ADC}(G_{INT}\sigma_{FE} \oplus \sigma_{BE})$ where $\sigma_{FE}[V]$ is the front-end noise (from the CSA and any added noise due to leakage current), and $\sigma_{BE}[V]$ is the back-end noise (from the everything after the CSA and the ADC). The ADC noise is 4.7 ADU[4]. Keeping RST continuously asserted allows us to measure $\hat{\sigma}_{BE} = \boldsymbol{G_{ADC}}\sigma_{BE} = 5.23 \pm 0.01$ ADU (independent of gain setting). The VASE back end thus contributes the quadrature difference of 2.3 ADU. The equivalent noise charge (ENC) is $\hat{\sigma}_n$ divided by the conversion gain. Operating the high gain VASE2 without a CCD gives an ENC of $14.0 \pm 0.5\,e$ on the highest gain settings, and $17.1 \pm 0.5\,e$ with a CCD, so that the addition of the CCD increases the ENC by 9.8 e in quadrature. Note that for an ideal integrator, the noise would be independent of G_{INT}. In VASE2, though, there are two competing effects: as the gain decreases, the noise contribution from R_{INT} increases, while due to slight high frequency peaking in the integrator frequency response, there is a noise increase as the gain increases. This can be seen in the slight noise increase for the highest gains in Figure 13A.

As described above, the VASE signal is proportional to integration time. By reducing the integration time, a larger full scale signal can be accommodated on a given gain range. Figure 14A shows the roughly linear reduction in signal with integration time. Of course, decreasing the integration time increases the noise bandwidth by $^1/_{\sqrt{T_{INT}}}$ as seen in Figure 14B. This can be seen in Figures 13A, B which shows noise and full scale for two different integration times. At 50% of the nominal integration time, the maximum signal on the low gain VASE2 corresponds to $4x10^5\,e$. Adjusting the integration time provides additional flexibility in optimizing full scale signal with noise, such as making the same kind of measurement at different energies, or with large sample-to-sample variations.

5 Conclusion

The VeryFastCCD is the fully-column-parallel successor to the FastCCD. Fabricated in the same CCD process, it has a 25 times higher frame rate. With 10 nm and 100 nm entrance window contacts, it has high quantum efficiency for soft and tender X-rays. The custom readout circuit has programmable gains and can also use integration time as a way to trade full-scale signal for noise. Prototype versions have been tested at ALS and LCLS, and systems for ALS are currently being prepared.

4 https://www.ti.com › dataconverters › ads52j65.

Data availability statement

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

Author contributions

AG: Formal Analysis, Writing–review and editing. CG: Conceptualization, Methodology, Writing–review and editing. JJ: Methodology, Writing–review and editing. AK: Methodology, Writing–review and editing. CT: Methodology, Writing–review and editing. PD: Conceptualization, Methodology, Project administration, Writing–original draft.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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