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Resonant THz detection by periodic multi-gate plasmonic FETs

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We show that a periodic multi-grated-gate structure can be applied to THz plasmonic FETs (TeraFETs) to improve the THz detection sensitivity. The introduction of spatial non-uniformity by separated gate sections creates regions with distinct carrier concentrations and velocities, giving rise to harmonic behaviors. The resulting frequency spectrum of DC voltage response is composed of "enhanced" and "suppressed" regions. In the enhanced region, the amplitude of response voltage can be enlarged up to ~100% compared to that in a uniform channel device. The distribution pattern of those regions is directly related to the number of gate sections (N_s). A mapping of response amplitude in a N_s-frequency scale is created, which helps distinguish enhanced/suppressed regions and locate optimal operating parameters.

KEYWORDS

plasma wave, TeraFET, multi-gate, THz detection, DC response

1 Introduction

Short channel field-effect transistor (FET) operated in plasmonic regime at sub-THz or THz frequencies (often referred to as TeraFETs [1, 2]), are promising devices for THz applications such as sensing [3–7], imaging [8–10], and beyond-5G communication [1, 3]. TeraFETs can work in the plasmonic resonant (ballistic or viscous) regimes [11, 12], in which the plasma waves are generated [13, 14]. Such hydrodynamic-like property allows TeraFETs to break the frequency limitation set for collision-dominated devices and operate at GHz to THz ranges. TeraFETs are also tunable by the gate bias or doping or illumination [15–17], The high speed of plasma waves enables TeraFETs to be a strong candidate for ultrashort pulse detection [18, 19].

To facilitate the industrial applications of TeraFETs, one of the key issues is to improve the detection sensitivity. As was discussed in [1], further improvement in the noise-equivalent power of TeraFETs is required to enable 6G communication applications. A straightforward way is to use better materials, e.g., materials with high mobility (μ) and high effective mass (m^*), so as to elevate the device quality factor ($Q = \omega_p \tau$, where ω_p is the plasma frequency, $\tau = \mu m^*/e$ is the momentum relaxation time) [20]. We have demonstrated that p-diamond could be a valid candidate for high-sensitivity THz and sub-THz detections [21–23]. In addition to the material consideration, one can also resort to new structural designs. The non-uniform structures, such as grating gates [24–28], dense arrays [29–31], and plasmonic crystals [24, 32], were introduced and proved to be effective in improving the TeraFET detection performance.

The introduction of specifically-arranged non-uniform structures in TeraFETs can modify the carrier density, static field distribution, and plasma wave velocity along the device channel, thus altering the THz rectification properties and/or the wave propagation features. For example, with a split-gate structure and a graded doping (i.e., the grating-gate), the circularly polarized THz radiation can be rectified by the TeraFET, inducing DC currents in both parallel and transverse directions [16, 28]. It was shown that the DC current flux in the transverse direction is related to the helicity of the THz radiation, and this current is dramatically enhanced near the plasmon resonant frequencies. The multi-gates can also be rearranged to create a concatenated FETs dense array, where the source, drain, and gate are all split into fingers and nested together to form the repeated unit cells [30, 31, 33]. Such short-period grating of metal contacts strengthens the device asymmetry and serves as an effective antenna coupling incident THz radiations, thereby improving the detection sensitivity. In addition, the grating-gate structure can also synergize with the applied DC current to create full transparency and the amplification of THz radiation [34].

In our recent work [2], we used a spatially non-uniform gate capacitance or threshold voltage to induce the channel nonuniformity. Those structures are capable of modifying the transport properties of plasma waves and enhance or suppress the non-resonant photoresponse [2, 35]. However, those structures contained spatially nonuniform dielectric layer and coordinate-dependent doping, making the device fabrication costly and cumbersome in real-world applications. Inspired by the periodic gate structures in previous works, in this work, we bring periodic multi-gate structures to our TeraFETs, and explore the effects of these structures on the resonant THz detection performance in a wide spectral range, including harmonic plasmonic modes. Compared to the varying capacitance or varying threshold voltage designs, the periodic gate structure is easier to fabricate as it does not require dielectric profiling or coordinate-dependent doping. As will be shown later, the periodic multi-gate TeraFETs possess strong harmonic behaviors and can reach a ~100% improvement in DC voltage response near the resonant peaks. The demonstrated improvement is achieved without a DC current bias, and thus it does not rely on any DC field effect or plasmonic instability mechanism.

2 Model and methods

In addition to the internal TeraFET responsivity, the measured responsivity depends on the THz-antenna coupling efficiency [36, 37] and the impedance matching [38]. The antenna coupling efficiency signifies the ratio of antenna collected power to the THz radiation power, and is related to the design of antenna [36] or the arrangement of dense gate arrays [29]. In this work, we only focus on the device-level improvement of THz detection sensitivity. Our results allow optimizing the TeraFET parameters per unit width, since we consider a one-dimensional model. We consider using a periodic multi-gate TeraFET structure to achieve high-sensitivity resonant THz detection. Figure 1A shows the schematic of the structure. The gates are driven by periodic-in-space DC excitations. The number of gate sections (N_s) is adjustable. In a system design, we could match the TeraFET impedance to the antenna impedance and to the load impedance by choosing the number of gate fingers and optimizing the gate finger dimension. With the repetitive excitation of DC biases V_{g1} and V_{g2}, the spatial distribution of DC gate voltage can be approximated by a square-wave voltage shown in Figure 1B. Here N_s is the number of split gates, P_L and P_H are the duty ratios of high and low voltage in one high-low cycle, respectively. P_C is the ratio of one high-low cycle in the whole channel. N_c is the number of complete high-low cycles. We define $P_L + P_H = 1$, $(N_C + P_L)P_C = (N_C{+}1{-}P_H)P_C = 1$. Besides, α is a voltage modulation factor, V_{g0} is a reference gate voltage. The square-wave approximation can be verified via electrostatic modeling (see Supplementary Material S1). A more realistic consideration is to include the transition regions between each two adjacent sections, as illustrated by dashed lines in Figure 1B. The transition region here results from the separation (i.e., the ungated region) between two adjacent gate segments. We assume that the length of the separated region is short so that carriers underneath can be screened by the peripheral voltage of neighboring gates. Therefore, we still consider the transition regions as gated regions.

We use a 1D hydrodynamic model [12, 15, 39] to simulate the response of the proposed TeraFET structure. The detailed

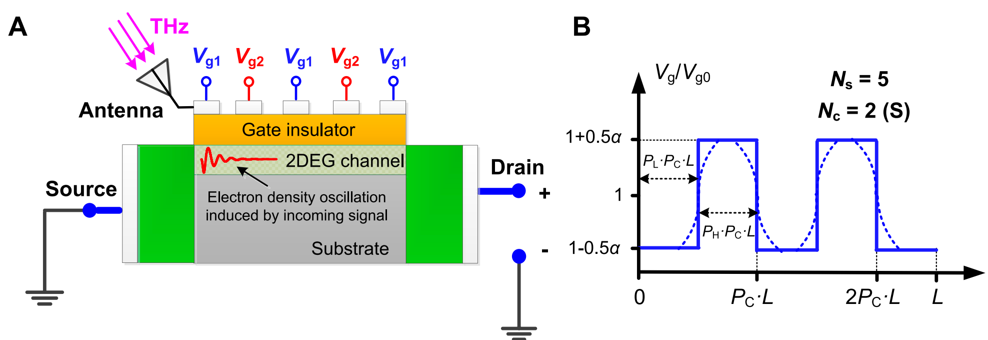

FIGURE 1
(A) Schematic of THz detection by a periodic multi-gate TeraFET. **(B)** The resulting spatial distribution of DC gate bias. The ideal and realistic distribution curves are illustrated in solid and dashed lines, respectively.

introduction and validation of the model can be found in [12]. The key equations are:

$$\frac{\partial n}{\partial t} + \nabla \cdot (n\boldsymbol{u}) = 0 \quad (1)$$

$$\frac{\partial \boldsymbol{u}}{\partial t} + (\boldsymbol{u} \cdot \nabla)\boldsymbol{u} + \frac{e}{m^*}\nabla U + \frac{\boldsymbol{u}}{\tau} - \nu \nabla^2 \boldsymbol{u} = 0 \quad (2)$$

where n, $\boldsymbol{u}$ are the carrier density and hydrodynamic velocity, respectively. m^* is the effective mass of carriers. U is the gate-to-channel voltage defined as $U(x) = U_0(x)—U_{ch}(x)$, where $U_0(x) = V_g(x)—V_{th}(x)$ is the gate bias beyond threshold, $U_{ch}(x)$ is the channel potential. In order to ensure that the device works in hydrodynamic regime, the scattering rates should satisfy $\gamma_{ee} > \max[\gamma_{e\text{-}ph}, \gamma_{e\text{-}imp}]$ [40], where γ_{ee}, $\gamma_{e\text{-}ph}$, and $\gamma_{e\text{-}imp}$ are the electron–electron, electron–phonon, and electron–impurity scattering rates, respectively. With a relatively low mobility set in our device (0.1 m^2/Vs), this condition can be met in the low bias region [21].

A unified charge-control model [41, 42] is used to related n and U:

$$n(U) = \frac{C_g \eta V_t}{e} \ln\left(1 + \exp\left(\frac{U}{\eta V_t}\right)\right) \quad (3)$$

where $V_t = k_B T/e$ is the thermal voltage (k_B: Boltzmann constant, T: temperature, fixed at 300 K). η is an ideality factor. The UCCM is valid as long as 1) the capacitive coupling between the gate and the device channel is valid and 2) the leakage current through the intrinsic capacitances (for example, the gate-to-source capacitance C_{gs}) is not too large as compared to the channel current. We have checked that those conditions can be met for TeraFETs considered in this work (see Supplementary Material S1 for details).

In this work, we focus on the effects of non-uniform V_g on the detection performance of TeraFETs in absence of any helicity-sensitive effects. For multiple-gate TeraFETs, the so-called ratchet effect could lead to the plasmonic enhanced rectification [28]. In this paper, we consider TearFETs with the variable gate voltage swing, where the ratchet effect is not important. We consider a multi-gate whose gate section near the source is connected with a THz coupling antenna, as shown in Figure 1A. In this way, the device absorbs the THz radiation only by the leftmost gate section, and consequently the boundary condition at the source can be approximated by $U(0,t) = U_0(0) + U_a(0,t)$ [20], where $U_a(0,t) = V_{am} \cdot \cos(\omega t)$ represents the AC small-signal voltage induced by the incoming THz radiation. We set V_{am} to 2 mV, which can be treated as a small signal with respect to the bias. On the drain side, an open circuit condition is used, i.e., $J(L, t) = 0$, where J is the current flux density, L is the channel length. With the above design, the plasma waves can be generated near the source side and get rectified by periodic gate biases while propagating along the channel. The DC response voltage can then be obtained by measuring the drain voltage and extracting its DC component.

In addition to the plasmon-induced response, there are other THz rectification mechanisms in TeraFETs, such as photo-thermoelectric effect [43] and junction linearity in tunneling FETs [44], quantum wells [45]. Similar effects has also been observed in HBTs [46]. In this work, we focus on the hydrodynamic nonlinearity enhanced by plasmons. We investigate split-gate Si MOSFET biased at a relatively low voltage at room temperature.

3 Results and discussion

3.1 Frequency dependent profiles

Based on the above model settings, we simulate our device and evaluate the frequency spectrum of DC source-to-drain response voltage (dU). According to Dyakonov-Shur theory [20], dU is proportional to the intensity of THz signal, which, in turn, is proportional to the squared THz voltage amplitude. For a single-gate device, the response has the form [20].

$$dU = \frac{eV_{am}^2}{4m^* s} f(\omega) \quad (4)$$

where ω is the angular driving frequency, $f(\omega)$ is a frequency-dependent function associated with the plasma wave (or damped electron wave) propagation properties. Generally, Eq. 4 applied to uniform-channel devices (i.e., single gate and no drain bias). Our recent work have shown that (4) can also be modified to evaluate the response in spatially nonuniform channel TeraFETs, such as exponentially-varying gate capacitance devices [2] and current-driven TeraFETs [47]. Besides, (4) does not take into account the device loading effect and thus only applies to devices with an infinite load impedance (e.g., an open-drain TeraFET). With a finite load resistance R_L, the output response voltage dU_o can be expressed by $dU_o = dU_I/(1+ R_{ch}/R_L)$ [48, 49], where dU_I is the intrinsic response given by (4), and R_{ch} is the channel resistance. Due to the voltage divider effect, the loaded TeraFET has a lower response voltage compared to the unloaded ones under the same operating conditions.

The results under linear $V_g(x)$ profile and 3 different N_s values under multi-gate structure are presented in Figure 2. These results are for a Si FET with 50% duty ratio ($P_L = P_H$ = 50%, see Figure 1), and $V_{g0} = -0.2$ V, $V_{th} = 0.2$ V, $V_{am} = 2$ mV, and at room temperature. Now the fundamental resonant frequency f_0 is at 0.515 THz, and the device is driven into the subthreshold mode with a low electron density (~10^{14} m^{-2}) but a relatively large voltage response [49, 50]. To improve convergence, the continuous-first-derivative transition regions are set between neighboring gate sections, and the relatively size of those regions (T_z, the ratio of total transition region size over the whole channel size) is fixed at $T_z = 0.1$ (see more details in Supplementary Material S1). The number of sections varied from 2 to 7. The voltage applied to different gates varied (see Figure 1B). Table 1 lists the major parameters used in the simulation.

Figure 2A shows the result under a linear varying gate voltage: $V_g(x) = V_{g0}(1+\alpha(x\text{-}0.5L)/L)$. We can see that with the increase of α (or the decrease of DC gate bias swing from source to drain since V_{g0} is negative), dU decreases when $f < f_0$, where $f_0 = S/4L$ is the fundamental resonant frequency, S is the plasma wave velocity [22, 50]. This region corresponds to the non-resonant operation region of the device. Using the methods in [2, 50], we can get the expression of DC response in this region (see Supplementary Material S1 for detailed derivations):

$$dU = \frac{eV_{am}^2}{4mS^2}\left(1 + \beta - \frac{1 + \beta\cos(2k_r L)}{\cosh(k_1 L)\cosh(k_2 L)}\right) \quad (5)$$

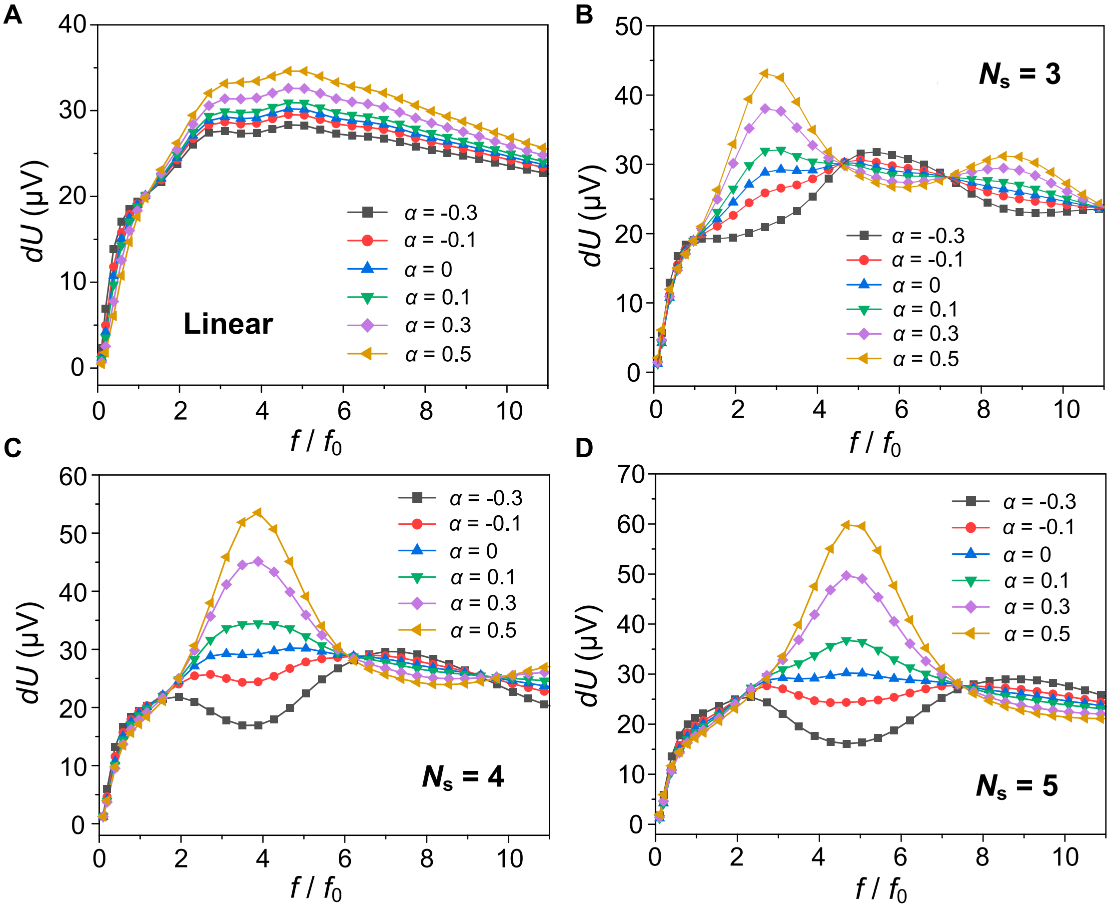

FIGURE 2
DC response voltage (dU) as a function of frequency (f) in a Si TeraFET with different channel designs. **(A)** Linearly distributed gate voltage. **(B)** Periodic multi-gate with N_s = 3. **(C)** Periodic multi-gate with N_s = 4. **(D)** Periodic multi-gate with N_s = 5.

TABLE 1 Simulation parameters used in this work.

Symbol	V_{g0}	V_{th}	L	T	N_s	P_L, P_H	α	T_z
Meaning	References gate bias	Threshold voltage	Channel length	Temperature	# of gate sections	Duty ratios	Voltage modulation factor	Transition region relative size
Value	−0.2 V	0.2 V	130 nm	300 K	2–7	50%	−0.3~0.5	0.1

where $\beta = 1/\text{sqrt}(1+(\omega\tau)^{-2})$, k_1, k_2 are wave vectors of the plasma wave:

$$k_1 = \frac{a_1^*}{2}\left(\frac{S_0}{S}\right)^2 + \sqrt{\left(\frac{a_1^*}{2}\left(\frac{S_0}{S}\right)^2\right)^2 + ik_0^2}$$
$$k_2 = \frac{a_1^*}{2}\left(\frac{S_0}{S}\right)^2 + \sqrt{\left(\frac{a_1^*}{2}\left(\frac{S_0}{S}\right)^2\right)^2 - ik_0^2} \quad (6)$$

Here $\alpha_1^* = \frac{1}{|V_{g0}|}\frac{\partial V_g}{\partial x}$, $S_0 = \sqrt{\frac{e|V_{g0}|}{m^*}}$, $S = \sqrt{\frac{\eta e V_t}{m^*}(1+\exp(-\frac{U_0}{\eta V_t}))\ln(1+\exp(\frac{U_0}{\eta V_t}))}$. Besides, $k_0 = k_0 = (\omega/S^2\tau)^{0.5}$ is the wave vector in the uniform channel ($\alpha_1{}^* = 0$), k_r is the real part of k_1 or k_2. A transition of variation trend with respect to α occurs at around $f = f_0$. Beyond f_0, the plasmonic resonance can be achieved, and dU decreases with increasing α. Now the response curve does not follow Eq. 6. Within $\alpha \in [0,0.5]$, the maximum improvement of dU is around 20%. Those results agree with our observations of linearly varying gate capacitance or threshold voltage [2].

Figure 2B shows the result of dU vs α under $N_s = 3$. Compared to Figure 2A, the 3-segment multi-gate TeraFET exhibits a distinct response profile, and Eq. 6 fails in this case. As f rises, the response voltage oscillates, and the variation trend of dU with respect to α changes multiple times. If we define the regions where dU increases with rising α as the "enhanced" regions, and the regions where dU decreases with rising α as the "suppressed" regions, we can see that the enhanced and the suppressed regions appear alternatively with the increase of frequency. More interestingly, the positions of those

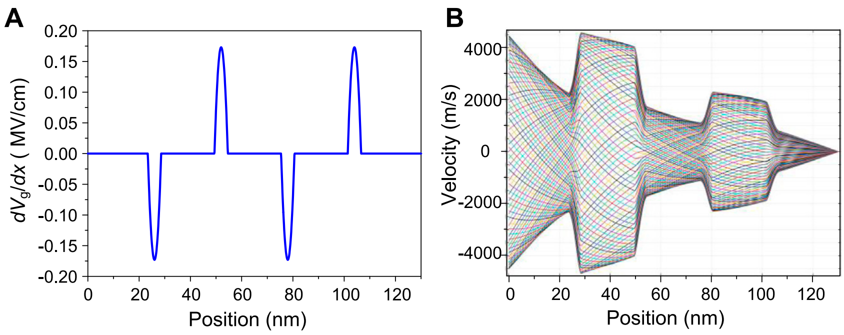

FIGURE 3
Spatial distributions of **(A)** the gradient of DC gate bias (dV_g/dx) and **(B)** variation contour of carrier velocity at $\alpha = 0.3$. Other parameters follow those in Figure 2.

regions are directly related to the number of gate sections. For example, the peak response voltage in the first enhanced region (which is also the peak dU in the whole frequency range) is at $f = 3f_0$, the position of response valley in the first suppressed region is $f = 6f_0$, and the position of peak response in the second enhanced region is at $f = 9f_0$. Thus, we conclude that the frequency at which the maximum response is reached is around

$$f_p = N_s f_0 \tag{7}$$

and the frequency gap between two adjacent peaks or valleys is

$$df_p = 2N_s f_0 \tag{8}$$

Eqs 8, 9 indicate that we can selectively enhance the resonant detection responsivity in a given frequency band by properly selecting the number and length of gate sections in a TeraFET. This result is similar to those reported in [34, 51], where the THz transmission spectra was controlled by the gate separations in grating-gating graphene FETs, and the resonant frequency was determined by the unit finger gate width ($\sim L/N_s$). However, unlike the current-driven boundary condition used in [34, 51], here we used an open-drain condition. Thus the enhancement and suppression of voltage response are independent of plasmonic instability or DC field effects, and solely originate from the setup of plasmonic cavities. Besides, the TeraFETs used in this work operate in the subthreshold region, in which the electron density and plasma wave velocity are less sensitive to the gate bias variations [50]. This helps stabilize the resonant frequency at each order (since $f_0 = S/4L$, where f_0 is the fundamental resonant frequency). This explains why there is no significant redshift or blueshift observed in Figure 2 as α changes.

Eqs 8, 9 can be further verified by the simulations under other N_s values. For example, in Figure 2C where $N_s = 4$, the peak frequency is at $4f_0$ and the distance between two adjacent peaks or two adjacent valleys are $8f_0$. In Figure 2D where $N_s = 5$, the values of f_p and df_p are $5f_0$ and $10f_0$, respectively. Also, a 100% increase in dU (compared to the uniform channel case) is achieved when α reaches 0.5. Note that the peaks and valleys are not located at the fundamental resonant frequency, but at the higher order harmonics. Therefore, the introduction of multiple gate sections activated the harmonic components in the system, resulting in the distribution of enhanced and suppressed regions. The underlying mechanism could be related to the reflection of plasma waves or carrier drift between neighboring sections due to the carrier concentration barriers. Those reflections change the wave propagation properties (i.e., k_1 and k_2) and shorten the effective channel length, thereby leading to the excitation of harmonic peaks and valleys. Figure 3A shows the spatial distribution of gate-induced field (dV_g/dx) along the channel. The abrupt change of DC gate bias in the narrow transition regions creates a large field on the order of 0.1 MV/cm. The electrons passing the transition regions get accelerated or de-accelerated, forming the separated velocity distribution regions, as demonstrated by the velocity distribution contour plot in Figure 3B. Each curve in Figure 3B represents the carrier velocity distribution $u(x)$ at a given moment in one AC period, and 50 consecutive moments are included. The separated velocity distribution regions could induce the reflections of plasma waves in between, thereby altering the DC response properties.

The above harmonic excitation mechanism can be seen as a result of abrupt changes in channel properties, as opposed to the gradual changes reported in our previous work [2]. In a gradually varying channel, the response performance is related to the changing rate of channel parameters (e.g., the gate capacitance, threshold voltage, DC gate bias). While in multi-gate setup, we can verify from simulation that the response dU is insensitive to the transition region size T_z (see supplementary material). This indicates that the response profile is now level-sensitive, as opposed to the gradient-sensitive ones in [2]. Therefore, the analytical approaches developed in [2] can no longer be applied here.

To further investigate the variation trend of dU with frequency, we define a differential response voltage $ddU = dU(\alpha = 0.3) - dU(\alpha = 0)$, and plot its frequency profile at different Ns values, as shown in Figure 4. Here ddU signifies the net enhancement or suppression of dU at $\alpha = 0.3$ as compared to the uniform channel case. In Figure 4A, the amplitude of ddU rises with the increase of N_s. This suggests

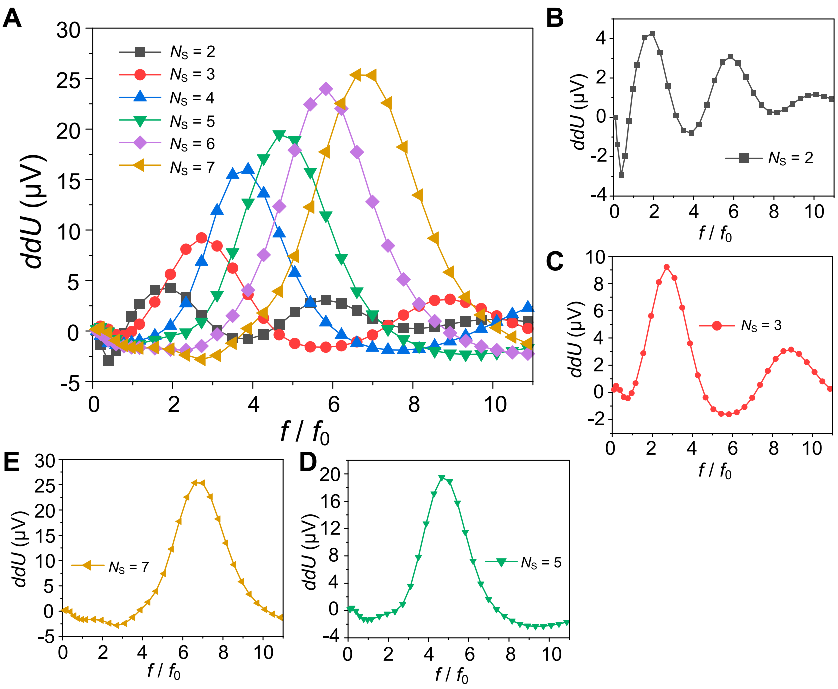

FIGURE 4
(A) *ddU* as a function of f/f_0 for N_s = 2~7 and **(B–E)** separated plots with N_s = 2, 3, 5, and 7, respectively. Other parameters follow those in Figure 2.

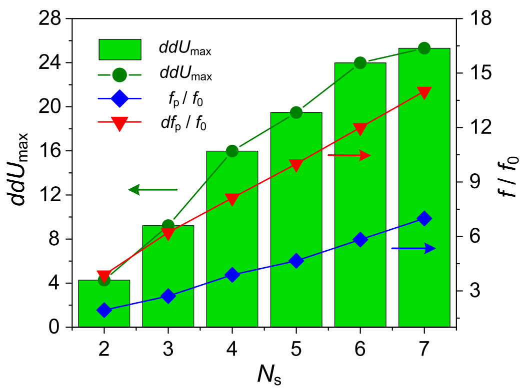

FIGURE 5
The peak value of *ddU* (ddU_{max}, in μV), the frequency at which *ddU* reaches the maximum (f_p), and the frequency gap between two adjacent peaks or valleys (df_p) as functions of N_s.

that the enhancement effect strengthens as the channel becomes more non-uniform. With the rise of frequency, *ddU* oscillates and exhibits multiple peaks and valleys, as shown in the separated plots Figures 4B–D. For quantitative analysis, we plot Figure 5 where ddU_{max}, f_p and df_p as functions of N_s are presented. One can check that the f_p and df_p curves follow Eqs 8, 9. The ddU_{max} increases with the rise of N_s, but a saturation trend is observed when N_s becomes large. This saturation could be related to the change of wave reflection characteristics as the length of each gate section shortens, which sets a limit to the maximum improvement of *dU*.

3.2 Mapping of enhanced/suppressed regions

To better understand how the response changes with frequency and gate structure, we create a map of *ddU* in a N_s-f/f_0 scale, as shown in Figure 6. In the map, the enhanced regions are exhibited as "mountains" while the suppressed regions are presented as "valleys"—a result of the present *ddU* definition. The highest mountain group is located at $f = N_s f_0$, as shown in Figure 6A, which corresponds to the maximum (the first) resonant peak in each case. The second mountain series are at $f = 3N_s f_0$, demonstrating the

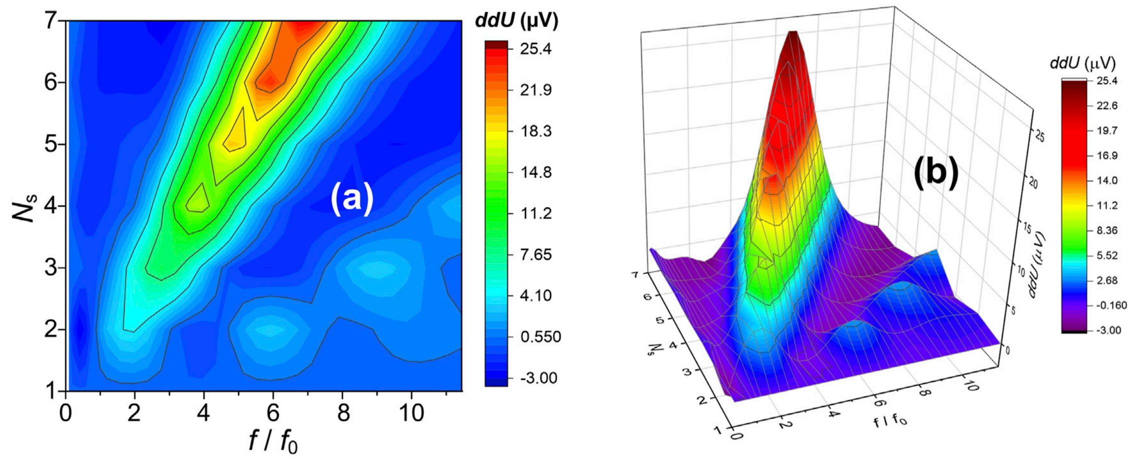

FIGURE 6
2D mappings of *ddU* in a N_s-f/f_0 scale. **(A)** 2D contour plot, **(B)** 3D colormap surface plot. The data presented are the same as those in Figure 5.

TABLE 2 Comparison of maximum response improvement in different TeraFET designs.

TeraFET design	Varying gate capacitance				Periodic multi-gate			
	Exponential			Linear	Sawtooth	Linear	N_s = 3	N_s = 5	N_s = 7
Material	Si	GaN	p-D	Si	Si	Si	Si	Si	Si
Max *dU* improvement	~10%	12%	15%	~10%	~20%	~20%	~50%	~100%	~140%

secondary resonant peaks. Between these two mountain groups is a valley group located at $f = 2N_s f_0$. In general, the mountain clusters can be expressed by $f = (2n+1)N_s f_0$, where n = 0,1,2 . . . , and the valley clusters follow $f = (2n+2)N_s f_0$.

Figure 6B shows the direct comparison of the heights of different mountains (i.e., the amplitudes of response peaks). Clearly, the mountain height in each group increases with the increase of N_s, and the average/maximum height in the first mountain group is much larger than that in the second mountain group. Thus, to achieve a high response, the TeraFET should operate in the first mountain group, and in general a large gate section number is preferred.

3.3 Limits of response tuneability

The results in Section 3.1 and Section 3.2 demonstrate that adopting periodic multi-gate structure in TeraFETs can effectively alter the DC voltage response and achieve over ~100% improvement in *dU* at certain frequencies. The amplitude of *dU* can be tuned by N_s and α. In general, a larger N_s or α leads to a higher responsivity in the enhanced region, but the values of N_s or α cannot grow infinitely due to several built-in limits. Here we discuss those limits.

1) Breakdown voltage (vertical). To prevent the breakdown of the barrier material, the following is required

$$\frac{(1+0.5\alpha)|V_{g0}|}{d_b} < E_b \rightarrow \alpha < 2\left(\frac{E_b d_b}{|V_{g0}|} - 1\right) \quad (9)$$

For example, if E_b = 3 V/nm, d_b = 4 nm, $|V_{g0}|$ = 0.2 V, we get $\boldsymbol{\alpha < 46}$.

2) Breakdown voltage (transverse). Let D denotes the transition region length between two gate sections, and D is related to T_z. To prevent dielectric breakdown in the transition region, we need

$$E_b > \frac{(V_{g1} - V_{g2})}{D} = \frac{\alpha|V_{g0}|}{D} \rightarrow \alpha < \frac{E_b D}{|V_{g0}|} \quad (10)$$

If E_b = 3 V/nm, $|V_{g0}|$ = 0.2 V, D = 2 nm, we get $\boldsymbol{\alpha < 30}$.

3) Conductivity limit. When the gate bias decreases in the subthreshold region, the carrier concentration can reduce to very low, so as to choke the current conduction. Assume that the minimum conductivity required for sustaining current conduction is $\sigma_{cr} = e\mu n_{cr}$, where n_{cr} is the critical carrier density. Using Eq. 3, we get:

$$n_{cr} = \frac{\sigma_{cr}}{e\mu} \le \frac{C_g \eta V_t}{e} \ln\left(1 + \exp\left(\frac{V_{g0}(1+0.5|\alpha|)}{\eta V_t}\right)\right)$$
$$\rightarrow |\alpha| \le 2\left(\frac{\eta V_t}{V_{g0}} \ln\left(\exp\left(\frac{e n_{cr}}{C_g \eta V_t}\right) - 1\right) - 1\right)$$
$$\approx 2\left(\frac{\eta V_t}{V_{g0}} \ln\left(\frac{e n_{cr}}{C_g \eta V_t}\right) - 1\right) \quad (11)$$

If $n_{cr} = 10^{13}$ m^{-2}, $V_{g0} = -0.2$ V, $V_t = 0.026$ V ($T = 300$ K), $\eta = 4$, we get $|\alpha| < 1.29$.

4) Process limit. The fabrication lab conditions determine the maximum number of separated gates that can be built in a TeraFET. If the minimum achievable size is L_{min}, then we get $N_{s\text{-}max} = [L/L_{min}]$, where $[k]$ denotes the nearest integer that does not exceed k. For example, with $L = 250$ nm, $L_{min} = 65$ nm, we get $N_{s\text{-}max} = 3$.

The above conditions, along with other more delicate mechanisms (e.g., the self-capacitance and the built-in voltage between two adjacent gate sections), set limit to the tuning of dU in periodic multi-gate TeraFETs. Despite all those constraints, an ~100% improvement can still be achieved near the maximum resonant peak, as demonstrated in Figure 2D.

3.4 Performance comparison

Table 2 summarizes the THz detection performance of TeraFETs with non-uniform gate capacitances and periodic multi-gate structures. The data in this table are taken either from [2] or from this paper. It can be seen that using gate capacitance profiling, the maximum reported response improvement was around 20%. With periodic multi-gate design, the response improvement can rise beyond 100% if sufficient gate sections are introduced. This further exhibits the advantage of periodic multi-gate design over gate capacitance profiling.

4 Conclusion

When a periodic multi-gate structure is applied in TeraFETs, the resonant THz detection performance can be improved. The hydrodynamic simulation showed that in periodic multi-gate TeraFETs, the harmonic response peaks were excited, and thus the DC response voltage dU near the harmonic frequencies could increase ("enhanced") or decrease ("suppressed") compared to dU in the uniform-channel TeraFETs. The excitation of harmonics peaks could be related to the strong gate-induced field in the transition regions, which accelerates or de-accelerates the carriers and possibly leads to the reflection of plasma waves on the boundaries of gate sections. The frequency spectrum of dU was separated by the "enhanced" and "suppressed" regions, and the distribution of those regions was related to the number of gate splits. The maximum improvement on dU reached beyond 100%. The tunability of dU via gate parameters is limited by the breakdown voltage, conductivity, fabrication resolution, and other more delicate effects. A mapping of variation in dU helps distinguish enhanced/suppressed regions and locate optimal operating parameters.

Data availability statement

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

Author contributions

YZ was primarily responsible for the design and realization of numerical simulations. MS supervised the entire work and provided guidance on the theoretical works. All authors contributed to the article and approved the submitted version.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Supplementary material

The Supplementary Material for this article can be found online at: https://www.frontiersin.org/articles/10.3389/fphy.2023.1170265/full#supplementary-material

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