frontiers | Frontiers in Physics

TYPE Original Research
PUBLISHED 23 December 2022
DOI 10.3389/fphy.2022.1102674

OPEN ACCESS

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SPECIALTY SECTION
This article was submitted to Optics and Photonics, a section of the journal Frontiers in Physics

RECEIVED 19 November 2022
ACCEPTED 15 December 2022
PUBLISHED 23 December 2022

CITATION
Hu Y, Hu L, Tang B and Yi Z (2022), A 10 bit 1 MS/s SAR ADC with one LSB common-mode shift energy-efficient switching scheme for image sensor. *Front. Phys.* 10:1102674. doi: 10.3389/fphy.2022.1102674

A 10 bit 1 MS/s SAR ADC with one LSB common-mode shift energy-efficient switching scheme for image sensor

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A 10 bit 1 MS/s SAR ADC with one LSB common-mode shift energy-efficient switching scheme for image sensor is presented. Based on the two sub-capacitor arrays architecture and the common-mode technique, the proposed switching scheme achieves 98.45% less switching energy over the conventional architecture with common-mode shift in one LSB. The comparator uses a low power dynamic comparator. The sampling switch adopts a bootstrap circuit with low sampling error. SAR logic is composed of Bit-Slice circuit with low power consumption and few transistors. Simulated in 180 nm CMOS process and 1 MS/s sampling rate, the ADC achieves the 60.06 dB SNDR, the 75.43 dB SFDR and the 10.45 μW power consumption.

KEYWORDS

image sensor, SAR ADC, switching scheme, energy-efficient, common-mode shift

1 Introduction

In recent years, successive approximation register (SAR) analog-to-digital converter (ADC) has been widely used in image sensors because of its low power consumption [1–4]. Figure 1 shows the basic processing units in a image sensor application, ADC is an intermediate unit that converts analog signals into digital signals. Among the components of SAR ADC, the energy consumed by capacitor array DAC accounts for a large part of the total energy consumed [5–7]. In order to improve the power efficiency of capacitor DAC, some energy-efficient switching schemes [8–11] have been proposed. Compared to a conventional switching scheme [12], set and down [8], Wang [9], Tri-level [10], and VMS [11] reduce the switching energy by 81.26%, 90.61%, 96.89%, and 97.66%, respectively. However, common-mode shift of these schemes is large.

In this paper, a new one LSB common-mode shift energy-efficient switching scheme is proposed to reduce common-mode shift. Based on the two sub-capacitor arrays architecture and the common-mode technique, the average switching energy of the proposed one LSB common-mode shift switching scheme for 10-bit SAR ADC is 21.08 CV_{ref}^2. Compared with the conventional [12] switching scheme, the switching

FIGURE 1
Block diagram of image sensor.

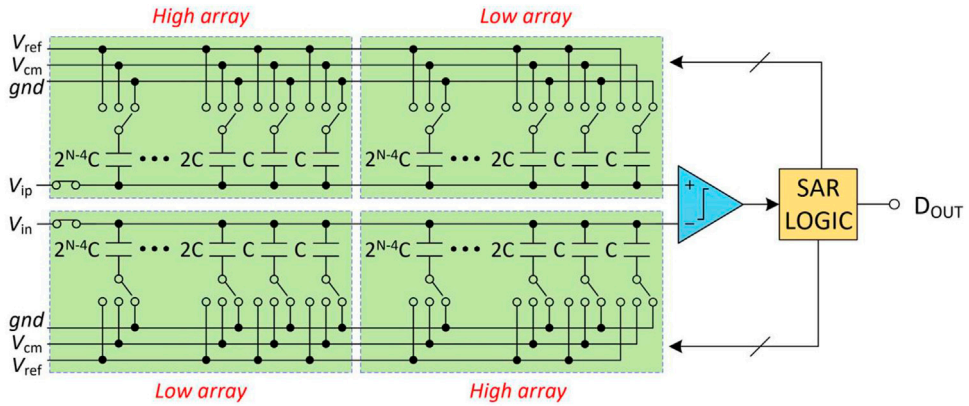

FIGURE 2
The proposed architecture of N-bit SAR ADC.

energy of the proposed switching scheme is reduced by 98.45%. A 10-bit 1 MS/s SAR ADC with the proposed one LSB common-mode shift energy-efficient switching scheme for image sensors is designed and simulated. The comparator uses a fully dynamic low-power comparator. In order to reduce the sampling error, the sampling switch adopts a bootstrap switch circuit [13, 14]. The SAR logic adopts a logic circuit based on Bit-Slice circuit, which can reduce the number of transistors and power consumption of SAR logic [15–17]. This SAR ADC is suitable for image sensor due to the adoption of various low power consumption techniques.

This paper is organized as follows. Section 2 explains the proposed SAR ADC architecture, which includes various low-power design technologies, such as one LSB common-mode shift energy-efficient switching scheme, dynamic comparator, bootstrap sampling switch, SAR logic based on dynamic circuit, etc.; The simulated results and the comparison with the state of the art are shown in Section 3. Finally, Section 4 concludes this article.

2 Proposed SAR ADC

The N-bit SAR ADC of the proposed architecture is shown in Figure 2. The SAR ADC consists of DAC, comparator, sampling switch and SAR logic. The DAC consists of positive capacitor array and negative capacitor array, and each array is composed of the same two sub-capacitor arrays (high array and low array).

2.1 Proposed one LSB common-mode shift switching scheme

To explain the operation of the proposed one LSB common-mode shift switching scheme, a 4-bit proposed SAR ADC is used. As shown in Figure 3, the operation includes four phases: 1st comparison, 2nd comparison, 3rd to (N-1)th comparison and Nth comparison.

1st comparison: The reference voltages of the high arrays are connected to V_{ref}, and the reference voltages of the low arrays are connected to gnd. The input signals are sampled to the top-plates of all capacitors through the sampling switch. The sampling switches are turned off after sampling. Then, the comparator directly compares the top-plates voltages of the positive and negative capacitor arrays, and outputs the comparison result D_1 (MSB). Therefore, the first comparison did not consume switching energy ($E_1 = 0$).

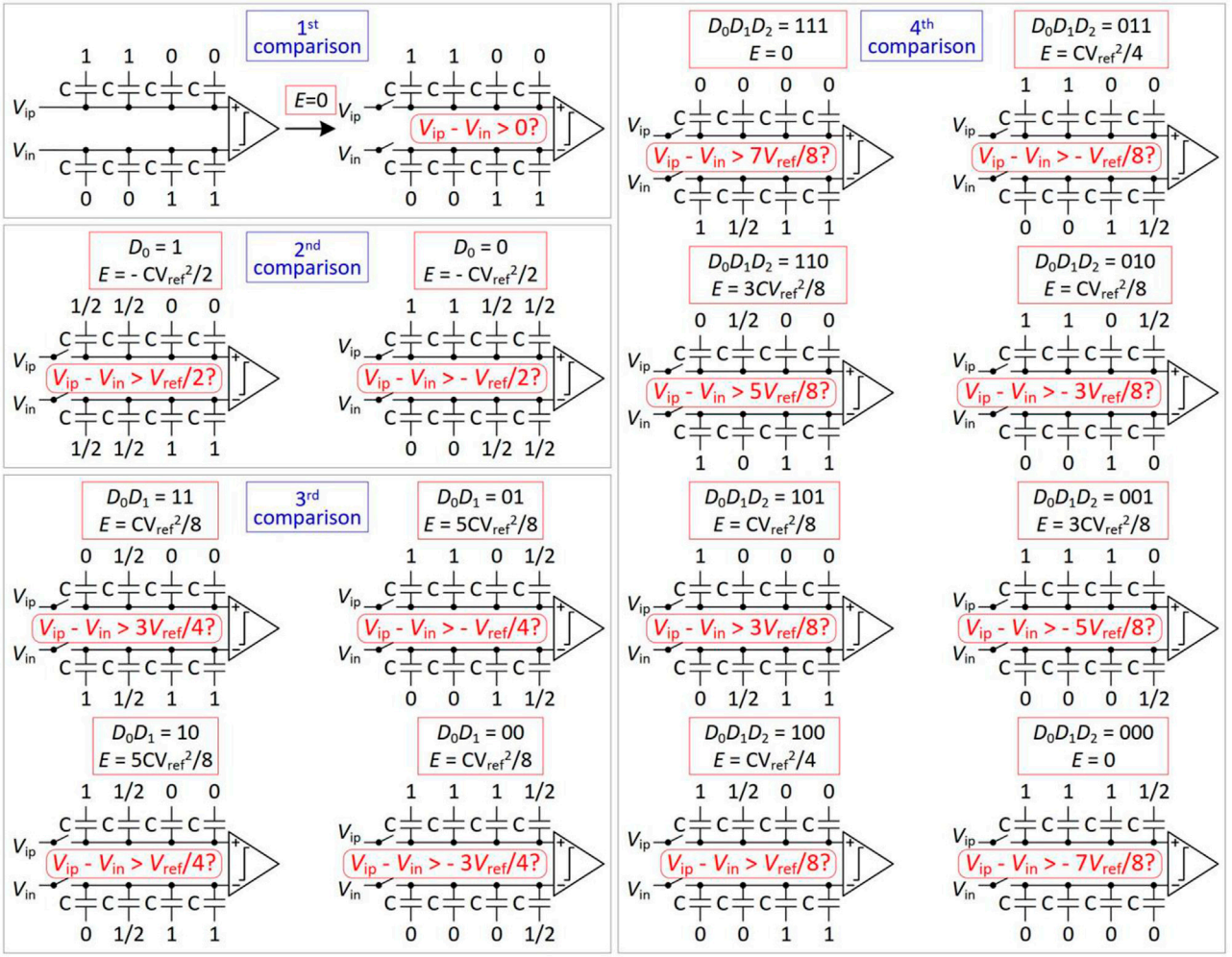

FIGURE 3
Switching procedure of 4-bit SAR DAC.

2nd comparison: If $D_1 = 1$, the reference voltages of the high array in positive capacitor array and the low array in negative capacitor array become V_{cm} ($V_{ref}/2$), and the reference voltages of other capacitors remain unchanged. If $D_1 = 0$, the reference voltages of the low array in positive capacitor array and the high array in negative capacitor array become V_{cm}, and the reference voltages of other capacitors remain unchanged. Therefore, the voltage on the higher side decreases by $V_{ref}/4$, the voltage at the lower side increases by $V_{ref}/4$ Then, the second comparison is performed, and the comparator outputs the result of the second comparison.

3rd to (N-1)th comparison: From the third comparison to the (N-1)th comparison, according to the results of the previous comparison, the reference voltage of the corresponding capacitor in the high-voltage capacitor array changes from V_{cm} to gnd, and the reference voltage of the corresponding capacitor in the low-voltage capacitor array changes from V_{cm} to V_{ref}. For example, in the third comparison, if $D_2 = 1$, the reference voltage of the largest capacitor connected to V_{cm} in the positive capacitor array is changed from V_{cm} to gnd, and the reference voltage of the largest capacitor connected to V_{cm} in the negative capacitor array is changed from V_{cm} to V_{ref}. If D2 = 1, the operation of positive and negative capacitor arrays will be exchanged. ADC repeats this operation until the $(N-1)^{th}$ comparison is completed. During this process, the common-mode voltage remains unchanged. From the third to $(N-1)^{th}$ comparison, the switching energy of each comparison is derived as

$$E_i = 2^{N-i-2} - 2^{N-2i-1} + (1 - 2D_{i-1}) \sum_{1}^{i-2} (2D_j - 1) 2^{N-i-j-2} \quad (1)$$

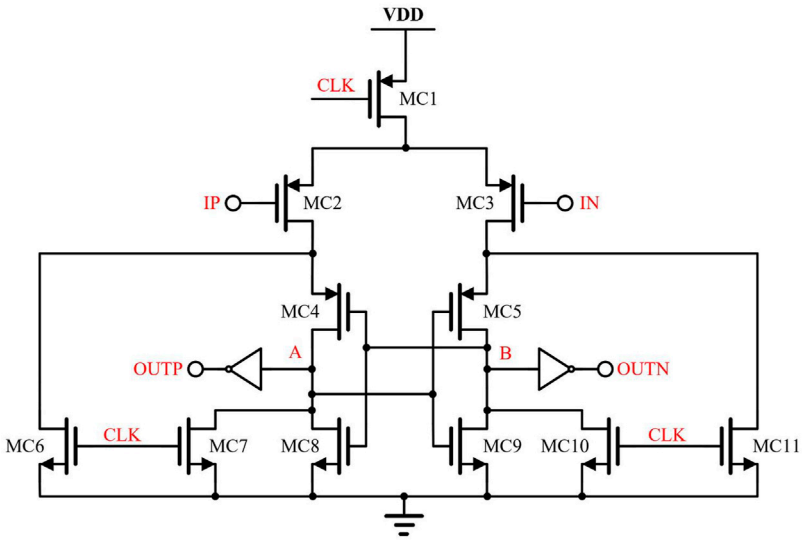

FIGURE 4
Dynamic comparator.

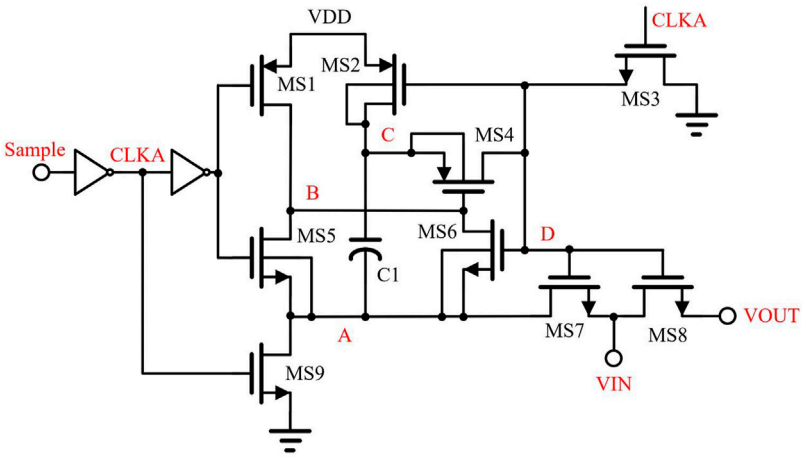

FIGURE 5
Bootstrapped sampling switch.

N^{th} comparison: If $D_{N-1} = 1$, the reference voltage of the last capacitor connected to V_{cm} in the positive capacitor array changes from V_{cm} to gnd, and the reference voltage of the capacitor in the negative capacitor array remains unchanged. If $D_{N-1} = 0$, the operation of positive capacitor array and negative capacitor array will be exchanged. In the N^{th} comparison, the common-mode voltage shifts one LSB. The switching energy in the N^{th} comparison is found to be

$$E_N = 2^{-2} - 2^{-N} + (1 - 2D_{N-1}) \sum_{1}^{N-2} (2D_j - 1) 2^{-j-2} \quad (2)$$

The average switching energy of proposed one LSB common-mode shift switching scheme for N-bit SAR ADC is:

$$E_{average} = 2^{N-2} - 2^{-2} - 2^{-N} + \sum_{1}^{N-1} 2^{N-2i-1} \quad (3)$$

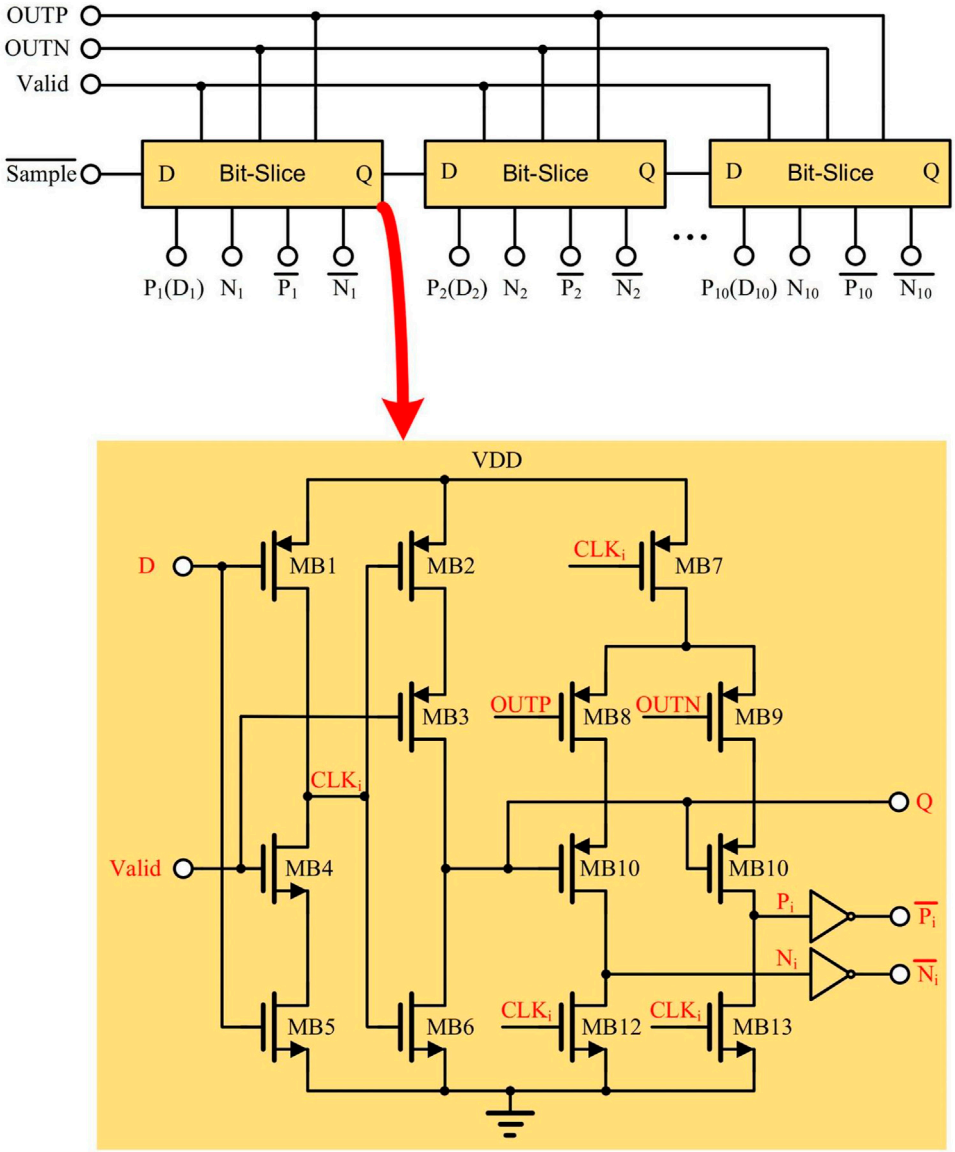

FIGURE 6
SAR control logic.

2.2 Comparator

Dynamic comparators are widely used in ADCs because of their low power consumption. In the application of the dynamic comparator, the NMOS is generally used as the input port [18–21]. As shown in Figure 4, in order to improve the accuracy of comparison, this paper uses PMOS as the input port for low VDD. The comparator work is divided into two phases. In the first phase, when CLK is high, MC1 is OFF, the paths connecting A and B to VDD are OFF, MC6, MC7, MC10, and MC11 are ON, A and B are connected to ground, and the output ports OUTP and OUTN are high. In the second phase, CLK is low, MC6, MC7, MC10, and MC11 are OFF, the paths from A and B to ground are disconnected, MC1 is ON, VDD charges A through MC1, MC2, and MC4, and through MC1, MC3, and MC5 charges B. The charging speed is related to the voltage of IP and IN. If IP > IN, the voltage of A is greater than the voltage of B. Since MC4, MC5, MC8, and MC9 constitute a positive feedback latch circuit, eventually the voltage of A will become low, the voltage of B will become high, OUTP will become high, and OUTN will become low

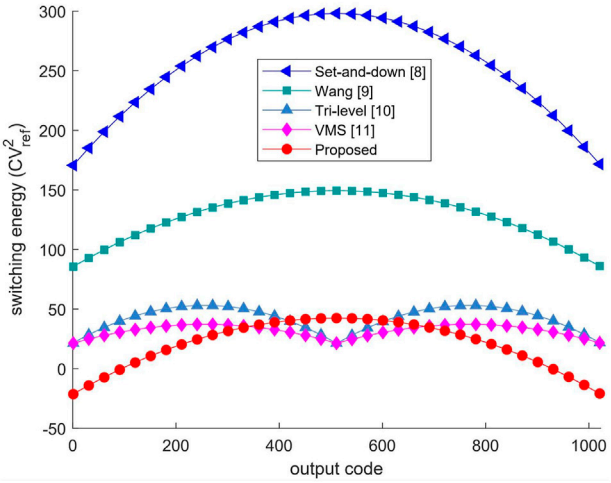

FIGURE 7
Switching energy against output codes.

TABLE 1 Comparison of energy saving and Common-mode shift for different switching schemes of a 10-bit SAR ADC.

Switching scheme	Average energy CV_{ref}^2	Energy saving	Common-mode shift
Conventional [12]	1,363.3	Reference	0
Set-and-down [8]	255.5	81.26%	512 LSB
Wang [9]	128	90.61%	512 LSB
Tri-level [10]	42.42	96.89%	512 LSB
VMS [11]	31.88	97.66%	256 LSB
Proposed	21.08	98.45%	1 LSB

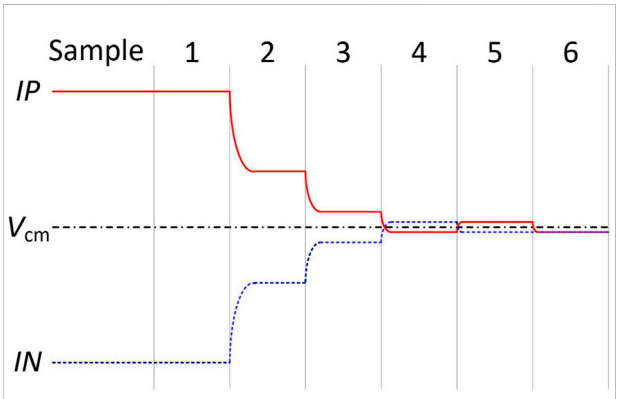

FIGURE 8
Waveform of the proposed switching scheme.

level. If IP < IN, then finally the voltage of A will become high, the voltage of B will become low, OUTP will become low, and OUTN will become high. During the operation of the comparator, there is no DC path from VDD to ground, so only dynamic power is consumed.

2.3 Sampling switch

In order to reduce the sampling error, the sampling switch generally adopts a bootstrap circuit [13, 14]. As shown in Figure 5, the bootstrap process is divided into two phases. In the first phase, when Sample is low, CLKA is high, MS1, MS2, MS3, and MS9 are ON, and MS4, MS5, MS6, MS7, and MS8 are OFF. At this time, A and D are low, B and C

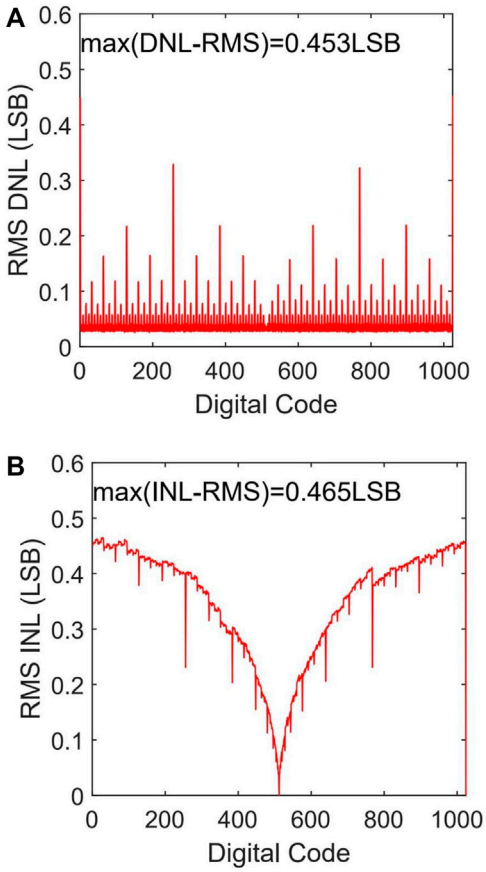

FIGURE 9
DNL and INL of DAC. **(A)** DNL. **(B)** INL.

are high. In the second phase, when sample is high, CLKA is low, MS1, MS2, MS3, and MS9 are OFF, MS4, MS5, MS6, MS7, and MS8 are ON, so the voltages of A and B are the input signals VIN, The voltages of C and D are bootstrapped as VDD + VIN. So the sampling switch MS8 realizes the bootstrap sampling.

2.4 SAR logic

The conventional SAR logic uses D flip-flop [8, 22, 23], which requires a large number of transistors and consumes a lot of power. In order to reduce the power consumption of the SAR logic, some papers use Bit-Slice circuit [15–17]. The Bit-slice circuit has fewer transistors and lower power consumption. As shown in Figure 6, during the sampling phase, Sample and Valid are high, P_i and N_i are low, $\overline{P_i}$ and $\overline{N_i}$ are high. After sampling, Sample becomes low, D of the first Bit-Slice becomes high, CLK_1 becomes low. At this time, if OUTP is greater than OUTN, then P_1 becomes high level, $\overline{P_1}$ becomes low, N_1 keeps low, and $\overline{N_1}$ keeps high. If OUTP is smaller than OUTN, then P_1 keeps low, $\overline{P_1}$ keeps high, N_1 becomes high, and $\overline{N_1}$ becomes low. When Valid becomes low, the result of the first comparison is latched, and Q of the first Bit-Slice becomes high. According to the working principle of the first Bit-Slice, the second to tenth Bit-Slices sequentially save the results of the second to tenth comparisons.

3 Simulation results and discussion

Several switching schemes for 10-bit SAR ADC are simulated in MATLAB. The average switching energy of the proposed one LSB common-mode shift switching scheme for 10 bit SAR ADC is 21.08 CV_{ref}^2. Compared with the conventional switching scheme [12], the average

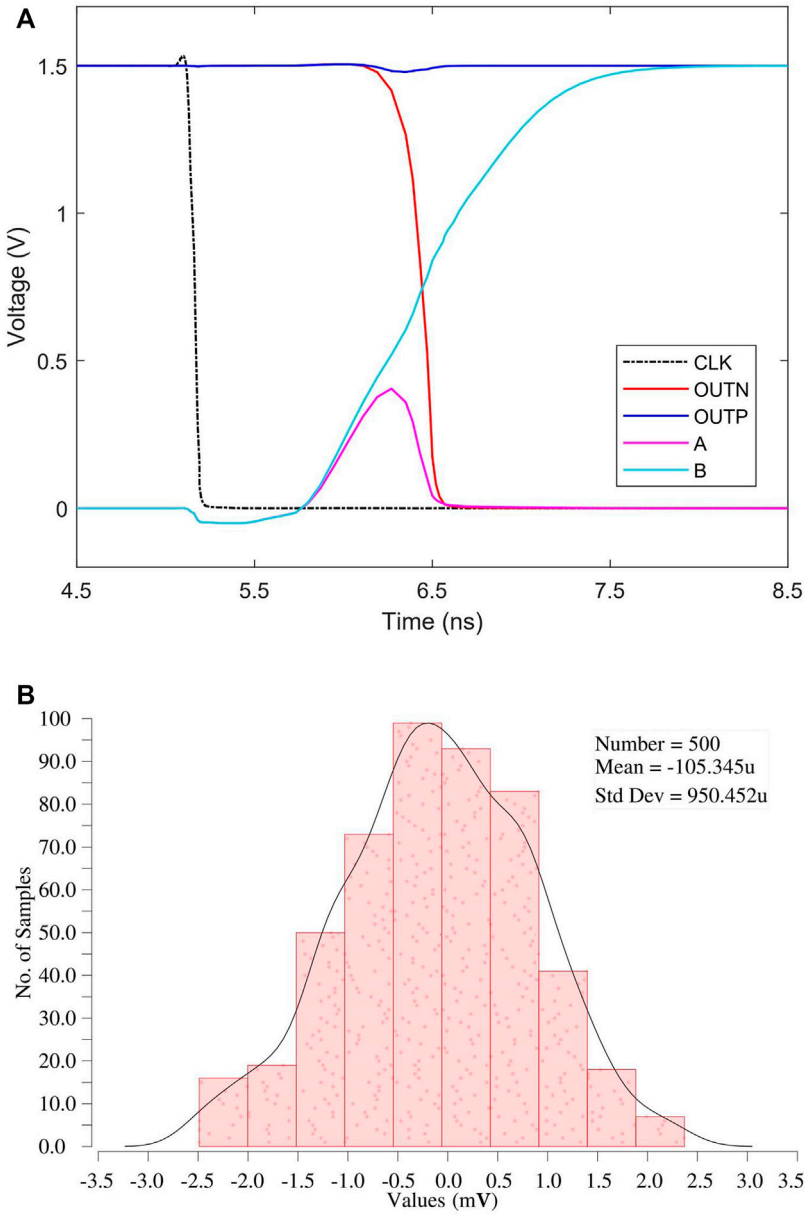

FIGURE 10
Simulation of dynamic comparator. **(A)** Transient simulation. **(B)** Monte Carlo simulation of the offset voltage.

switching energy is reduced by 98.45%. The switching energy at each output code for different switching schemes are shown in Figure 7. The comparison of several switching schemes [8–11] for 10-bit SAR ADC are shown in Table 1. These switching schemes [8–11] show great energy efficiency at the expense of very large common-mode shift. The common-mode shift of the proposed one LSB common-mode shift switching scheme shifts by one LSB which is less than those of the switching schemes [8–11]. The successive approximation waveform of the proposed one LSB common-mode shift switching scheme is shown in Figure 8. From the first comparison to the $(N-1)^{th}$ comparison, the common-mode voltage remains V_{cm}, and in the last comparison, the common-mode voltage shifts by one LSB. Figures 9A, B show the 500 times Monte Carlo simulation results of the proposed DAC switching scheme. When the unit capacitance mismatch is $\sigma_u/C_u = 2\%$, the RMS DNL and RMS INL of the proposed DAC switching scheme

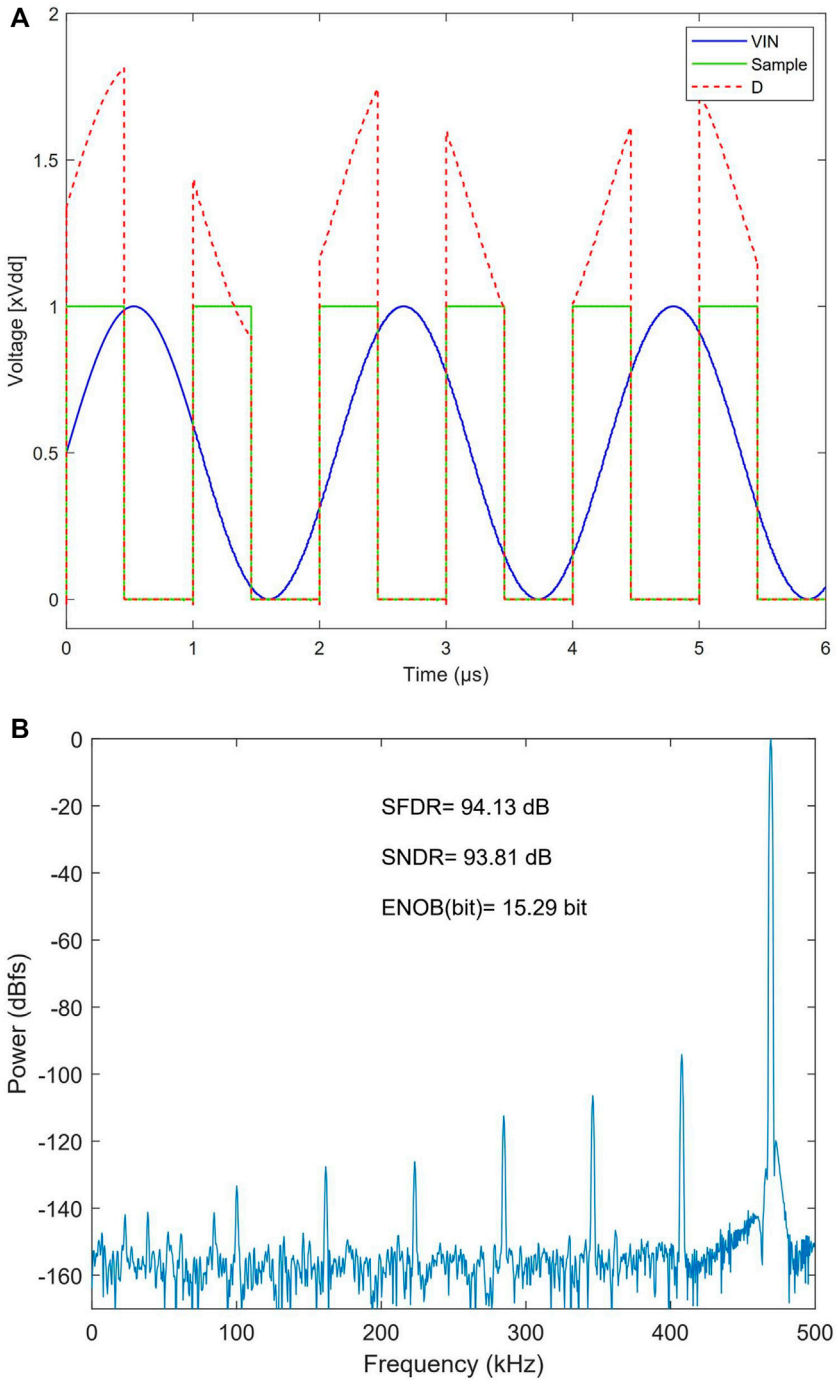

FIGURE 11
Simulation of bootstrapped sampling switch. **(A)** Transient simulation. **(B)** FFT of Bootstrapped sampling switch.

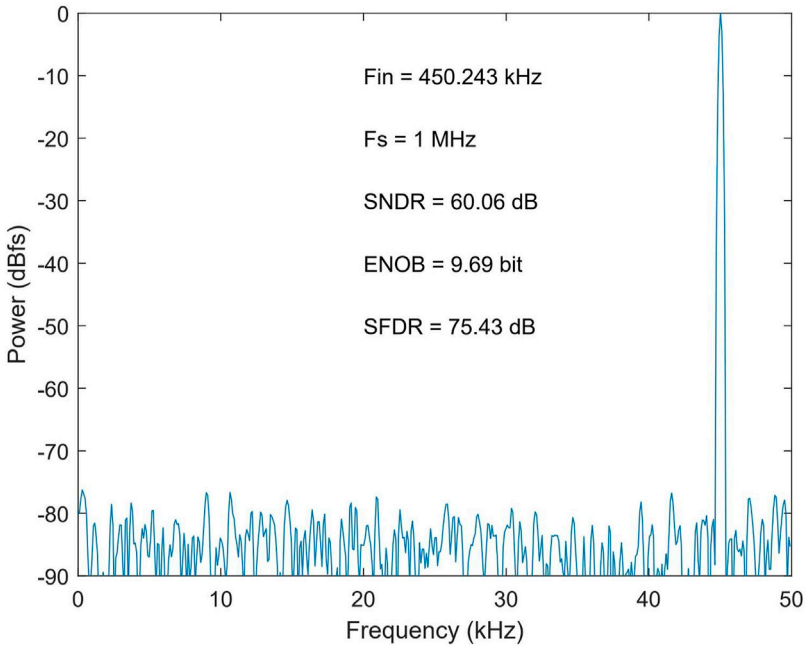

FIGURE 12
FFT of ADC.

are .453 LSB and .465 LSB respectively, meeting the requirement that the ADC non-linear error should be less than .5 LSB.

The transient simulation of the comparator is shown in Figure 10A. The differential input signals IP and IN of the comparator are 752.5 mV and 747.5 mV respectively. It can be seen from the figure that when CLK drops to low, A and B first increase the voltage together, and then gradually separate, one becomes higher and the other becomes lower. Finally, OUTP and OUTN become one high and one low. The comparator completes the output of comparison results. As shown in Figure 10B, the offset voltage of the dynamic comparator is 950.452 μV after 500 Monte Carlo simulations. The offset voltage does not exceed 1.46 (1,500/1,024) mV.

The transient simulation diagram of bootstrap sampling switch is shown in Figure 11A. It can be seen from the figure that when the sampling signal sample is high, the control signal D of the sampling switch is bootstrapped up and changes with the input signal VIN. Therefore, V_{GS} of transistor MS8 remains unchanged during sampling, thus reducing the sampling error. Figure 11B shows the spectrum analysis results of the bootstrap sampling switch. The SFDR and SNDR are 94.13 dB and 93.81 dB respectively, and the ENOB of the sampled signal is 15.29 bit, which can meet the requirements of 10 bit SAR ADC.

The proposed SAR ADC was designed and simulated using 180 nm CMOS technology. The simulation settings are as follows: the power supply is 1.5V, the full swing input signal frequency is 450.243 kHz, and the sampling rate is 1 MS/s. Figure 12 shows the FFT spectrum of the proposed SAR ADC. The ADC achieves 75.43 dB spurious-free dynamic range (SFDR) and 60.06 dB signal-to-noise and distortion ratio (SNDR), respectively. Figures 13A, B show the variation of SFDR and SNDR with input signal frequency and sampling frequency. The simulated DNL and INL of the proposed SAR ADC are shown in Figure 14A, B. The peak DNL and INL are −.30–+.33 LSB and −.36–+.20 LSB, which are both less than .5 LSB. The proposed SAR ADC has a total power consumption of 10.45 μW. Figure 15 shows the percentage of each circuit module in the total power consumption of the SAR ADC. Performance comparison of various ADC [24–28] is shown in Table 2. The proposed SAR ADC is suitable for image sensors. The Figure-of-Merit (FoM) was calculated from the following equation:

$$FoM = \frac{Power}{2^{ENOB} \times f_{sampling}} \tag{4}$$

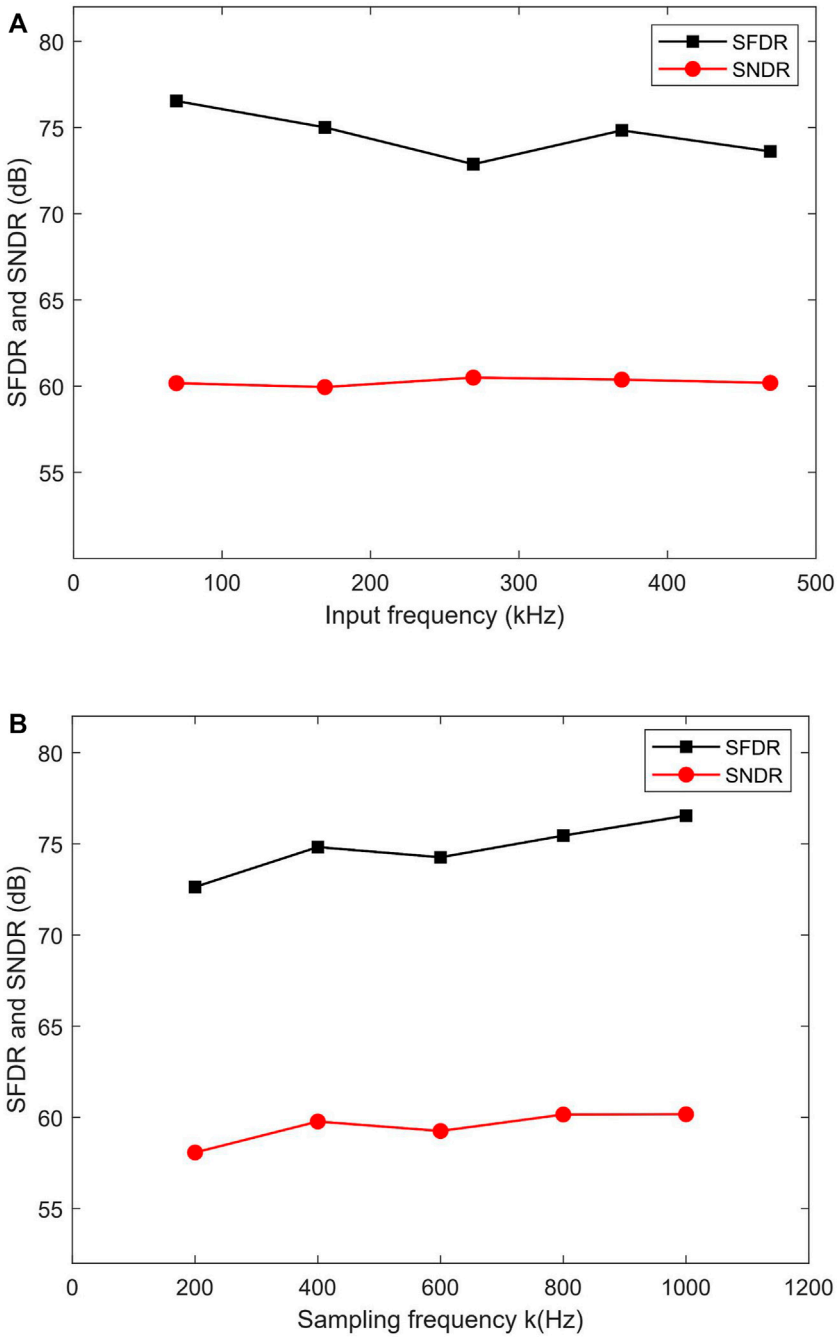

FIGURE 13
SNDR/SFDR with various input frequencies and various sampling frequencies. **(A)** Various input frequencies. **(B)** Various sampling frequencies.

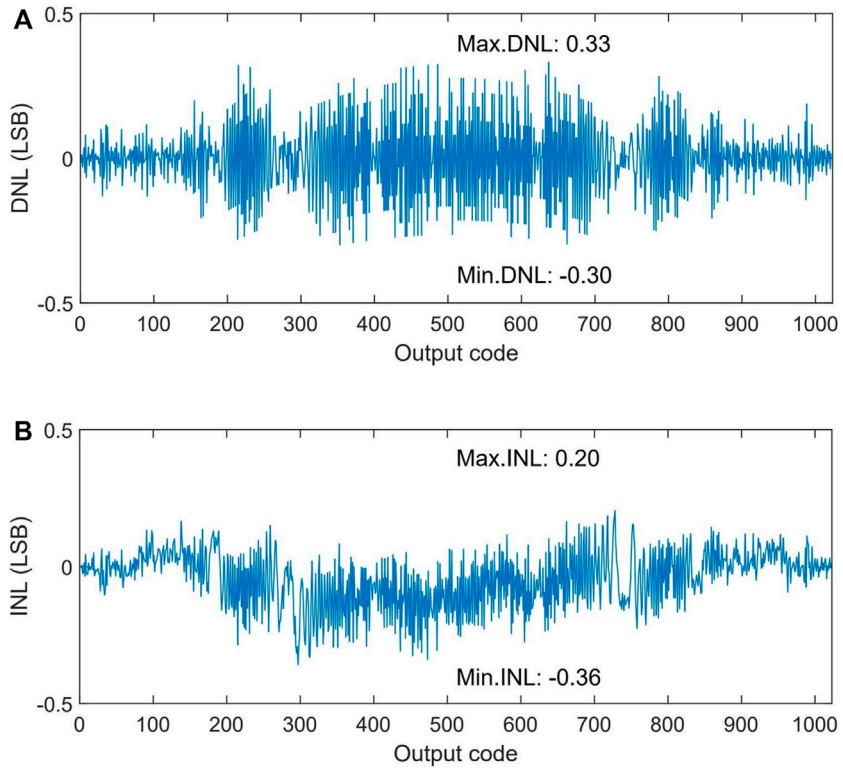

FIGURE 14
DNL and INL of ADC. **(A)** DNL. **(B)** INL.

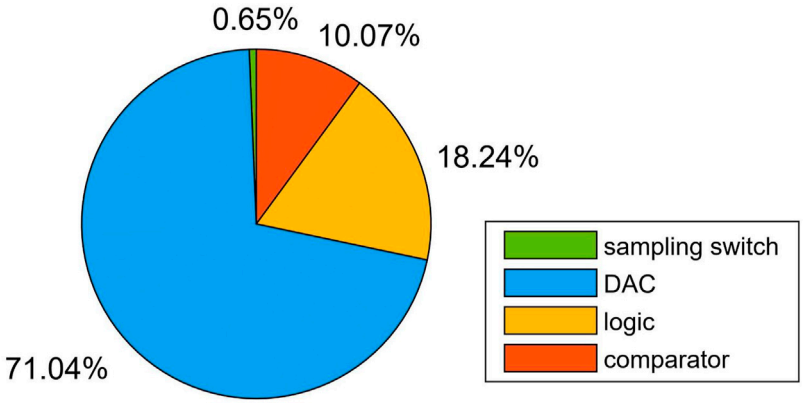

FIGURE 15
Power breakdown of the ADC.

TABLE 2 Performance comparison.

Parameter	[26]	[25]	[24]	[27]	[28]	This work*
Process (nm)	130	180	180	55	180	180
Resolution (bits)	10	8	10	10	12	10
Sampling Rate (MS/s)	1	1	1	1	1	1
Supply Voltage (V)	.8	1.8	1.2	1	1.4	1.5
SNDR (dB)	–	45.3	–	60.39	–	60.06
ENOB (bits)	8.8	7.23	8.7	9.74	11.25	9.69
DNL (LSB)	−.33/.56	.66	.4	−.5/.7	.54	−.30/.33
INL (LSB)	−.61/.55	.61	.46	−.7/.6	.89	−.20/.36
Power Consumption (μW)	9	10.3	34.6	14.8	44.78	10.45
FoM (fJ/conv. Step)	20	67	83	17.3	18.39	12.65

*Simulated results.

4 Conclusion

This paper has presented a 10 bit 1 MS/s low-power SAR ADC for image sensors. The proposed SAR ADC consists of DAC, dynamic comparator, bootstrap sampling switch and SAR logic. The DAC consists of positive capacitor array and negative capacitor array, and each array is composed of the same two sub-capacitor arrays. Based on these sub-capacitor arrays, the DAC uses a one LSB common-mode shift energy-efficient switching scheme to reduce power consumption. Compared with conventional switching scheme, the proposed switching scheme achieves an energy savings of 98.45%. In addition, the simulation shows that the offset voltage of the comparator and the ENOB of the sampling switch meet the requirements of ADC. Bit-Slice circuit makes the power consumption of SAR logic lower and the number of transistors less. Simulated in 180 nm CMOS process and 1 MS/s sampling rate, the ADC achieves 75.43 dB SFDR, 60.06 dB SNDR and 10.45 μW power consumption. The FoM of the proposed SAR ADC is 12.65 fJ/conv.-step. The proposed low-power SAR ADC is suitable for image sensors.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material, further inquiries can be directed to the corresponding author.

Author contributions

YH: Conceived the project, organized the paper content, wrote and edited the manuscript. LH: Designed and simulated the circuit. BT: Drawn the figure. ZY: Edited the manuscript.

Funding

This work was financially supported by the Key Field Project of Colleges and Universities in Guangdong Province (Grant no. 2022ZDZX1044), the Key Project of Social Welfare and Basic Research Project in Zhongshan City (Grant no. 2021B2020), the Construction Project of Professional Quality Engineering in 2020 (Grant no. YLZY202001), the Construction Project of Professional Quality Engineering in 2021 (Grant no. JD202101).

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

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