



Editorial: Neuromorphic Memristive Computation: Where Memristor-Based Designs Meet Artificial Intelligence Applications

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Editorial on the Research Topic

Neuromorphic Memristive Computation: Where Memristor-Based Designs Meet Artificial Intelligence Applications

The definition of a memristor was introduced by Professor L. O. Chua in 1971. By generalizing the definition of a memristor, memristive devices and systems were also proposed. Since the real memristor was implemented at Hewlett-Packard Labs, there has been an increasing interest in memristor and its applications. Memristor displays the relationship between charge and magnetic flux. In recent years, memristive systems have found potential applications in various areas ranging from physics, biological models to engineering.

Memristor-based neuromorphic computing has been introduced as a breakthrough technique and is expected to solve current computational bottlenecks. The memristive neuromorphic system exhibits advanced features, such as a much lower power supply voltage requirement, lower power consumption, and a nano-scale size, therefore opening a very promising memristive era for practical systems.

Besides the rapid development of the field, there are still different issues that should be further investigated. Exploiting the favorable performance merits of mem-elements concerning their non-volatility and switching speed is still an open topic. In addition, the optimization of area and energy dissipation for large array integration architecture is a challenging task. There is a need to propose memristive deep neural networks combining recent advances in the machine learning areas, such as deep learning, with nonlinear dynamics and novel features of memristor elements. Moreover, there is an increasing demand for a practical solution to integrate such systems in low-cost, energy-saving devices for various Internet of Things applications. This Research Topic aims to represent and discuss advanced topics of neuromorphic mem-computation. The contents and contributions of articles in this Research Topic are summarized as follows.

Recurrent neural networks and Long Short-Term Memory (LSTM) are inspired by the neuronal feedback networks. LSTM prevents vanishing and exploding gradients problems faced by simple recurrent neural networks and can process order-dependent data. Such recurrent neural units can be replicated in hardware and interfaced with analog sensors for efficient and miniaturized implementation of intelligent processing. Implementation of analog memristive LSTM hardware is an open research problem and can offer advantages of continuous domain analog computing with a relatively low on-chip area compared with a digital-only implementation. Therefore, Adam et al. have designed generalized analog LSTMs recurrent modules for solving time-series prediction

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problems. Architectures and circuits were tested with TSMC 0.18 μm CMOS technology and hafnium-oxide based memristor crossbars. Extensive circuit based SPICE simulations were performed for benchmarking the system performance of the proposed implementations. The analysis includes Monte Carlo simulations for the variability of memristor conductance, and crossbar parasitic, where non-idealities of hybrid CMOS-memristor circuits are taken into the account.

A variable boostable chaotic system and the Hindmarsh-Rose neuron model are applied by Ma et al. for observing the dynamics revised by memristive computation. Nonlinearity hidden in a memristor makes a dynamic system prone to chaos. Inherent dynamics in a dynamic system can be preserved in specific circumstances. Specifically, offset boosting in the original system is inherited in the derived memristive system, where the average value of the system variable is rescaled linearly by the offset booster. Additional feedback from memristive computation raises chaos, as a case, in the Hindmarsh-Rose neuron model the spiking behavior of membrane potential exhibits chaos with a relatively large parameter region of the memristor.

When implementing a pseudo-random number generator (PRNG) for neural network chaos-based systems on FPGAs, chaotic degradation caused by numerical accuracy constraints can have a dramatic impact on the performance of the PRNG. To suppress this degradation, Yu et al. have proposed a PRNG with a feedback controller based on a Hopfield neural network chaotic oscillator in which a neuron is exposed to electromagnetic radiation. Authors choose the magnetic flux across the cell membrane of the neuron as a feedback condition of the feedback controller to disturb other neurons, thus avoiding periodicity. The proposed PRNG is modeled and simulated on Vivado software and implemented and synthesized by the FPGA device ZYNQ-XC7Z020 on Xilinx using Verilog HDL code.

Memristor is a kind of synaptic element with nanometer size and continuously variable memristance. The bridge synaptic circuit constructed by the memristor has a simple structure and precise control. In practice, because of the non-linear characteristics of memristor, it is not easy to control synaptic circuits and errors in weights appear. Therefore, a novel

memristor synaptic circuit is proposed by Wang et al., named the dual-mode memristor bridge synaptic neural network. The proposed method can make the weights more linear by controlling the input voltages, making the outputs more linear by using symmetrical positive and negative pulses. As a result, the proposed synaptic circuit is more easily controlled. The numerical simulations are conducted and verify the feasibility. Furthermore, the simulation experiments are conducted for edge extraction of grayscale birds' images in the airport for bird recognition applied for the bird repelling applications.

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