

Development of electrostatic supercapacitors by atomic layer deposition on nanoporous anodic aluminum oxides for energy harvesting applications

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Nanomaterials can provide innovative solutions for solving the usual energy harvesting

and storage drawbacks that take place in conventional energy storage devices based on

batteries or electrolytic capacitors, because they are not fully capable for attending the

fast energy demands and high power densities required in many of present applications.

Here, we report on the development and characterization of novel electrostatic

supercapacitors made by conformal Atomic Layer Deposition on the high open surface

of nanoporous anodic alumina membranes employed as templates. The structure of

the designed electrostatic supercapacitor prototype consists of successive layers of

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Aluminum doped Zinc Oxide, as the bottom and top electrodes, together Al₂O₃ as the intermediate dielectric layer. The conformality of the deposited conductive and dielectric Spain layers, together with their composition and crystalline structure have been checked by XRD and electron microscopy techniques. Impedance measurements performed for the optimized electrostatic supercapacitor device give a high capacitance value of $200 \,\mu$ F/cm² at the frequency of 40 Hz, which confirms the theoretical estimations for such kind of prototypes, and the leakage current reaches values around of 1.8 mA/cm² at 1 V. The high capacitance value achieved by the supercapacitor prototype together its small size turns these devices in outstanding candidates for using in energy harvesting and storage applications. Keywords: supercapacitor, nanoporous alumina membranes, atomic layer deposition, leakage current, energy storage, energy harvesting Introduction

Nowadays, most energy harvesting and storage systems are required to fulfill two main properties: high electrical energy density $(W \cdot h)$ and high power supplied (W). Batteries can solve the energy storage problem, but do not reach high enough power density specifications required for many applications such as electric/hybrid vehicles, renewable sources, portable and consumer electronics, etc. Nevertheless, the conventional electrostatic and electrochemical capacitors can supply high power density requirements but sacrificing the energy storage capacity [1, 2]. For these reasons, the researchers' community is looking for innovative strategies that allow increasing the energy density of these devices [3-6]. The outstanding properties exhibited by nanostructured

materials are the key for the next generation of energy harvesting and storage devices. In order to accomplish with these objectives, the combination of patterned 3D nanostructures together with thin film deposition techniques are outstanding candidates to solve the high energy density storage problems, but without sacrifice the increasing power density requests [7-16]. In particular, one of the most promising applications of nanomaterials for energy storage technologies is aimed to the fabrication of electrostatic supercapacitors (ESCs) by taking advantage of the huge specific surface area of nanostructured substrates like patterned templates combined with novel thin film deposition techniques to achieve high capacitance values. These engineered supercapacitors show a similar conductor-dielectric-conductor (CDC) structure to conventional electrostatic capacitors, which are constituted by two conductor (or semiconductor) electrodes and separated by an intermediate dielectric layer [5-7, 17-21].

The plane-parallel configuration is the simplest type of electrostatic capacitor, where its capacitance can be described in this case as follows:

$$C = \frac{\kappa \varepsilon_0 A}{d} \tag{1}$$

where *C* is the capacitance, κ the dielectric permittivity of the electrical insulator, ε_0 is the vacuum permittivity constant (8.85 × 10⁻¹² F/m), *A* is the capacitor area and *d* is the thickness of the insulating layer. Therefore, the capacitance is increased in devices with high dielectric permittivity values, large effective surface area and reduced layer thickness of the electrical insulator.

When aiming to achieve extremely high capacitance densities, it becomes necessary to combine the benefits obtained with a high permittivity insulator material and an increased effective surface area. In this way, highly hexagonally ordered nanoporous anodica alumina membranes (NAAMs) are excellent high open surface-area substrates for being employed as patterned templates, due to their self-assembled porous structure having well defined geometrical lattice parameters and with high aspect ratio values that can be adjusted by controlling the anodization conditions (Figure 1) [3, 22]. The simple production process, low cost fabrication and easily adjustable morphological parameters make that NAAMs are currently used in great number of applications in materials science [23-25]. However, the increased surface area of these NAAM templates requires of the ability to deposit thin films with conformal coverage and uniform layer thickness on the walls and inside the pores of the high aspect ratio nanoporous structure. For most thin film deposition methods this is an extremely difficult task, but the ALD technique can provide a precise control over the thickness of the deposited layers, also providing an excellent conformality of the surface coverage even on surfaces having high aspect ratios. Furthermore, ALD can be straightforward scaled-up and it offers a facile method for introducing dopant elements in the deposited materials [26-28].

Both, the top (TE) and bottom (BE) electrodes material must exhibit good conductivity properties and the bottom electrode must have a low thickness (t_{BE}) to achieve a remarkable increase in the capacitance values. For this reason, Al-doped ZnO (AZO) thin film is a great candidate to constitute the electrodes of the supercapacitor due to its attractive physical characteristics, such



as excellent thermal stability and low electrical resistivity [29, 30]. The role played by dielectric materials is also relevant for the capacitor behavior, because the insulating material must have high dielectric constant and low thickness ($t_{dielectric}$) to improve the capacitor capacitance (Equation 1), but if the thickness is too low, it will lead to the premature breakdown of the ESC. Alumina (Al₂O₃) is usually chosen as the insulating layer due to its ability for being deposited by ALD, its relatively high dielectric constant ($k\sim$ 7), exceptional stability and durability [31].

The total capacitance of the supercapacitor prototype designed on the basis explained above, could be calculated as the sum of the three different contributions to the whole capacitance, according to the supercapacitor geometry displayed in **Figure 1**, by including the planar space among pores (2), the cylindrical part of the pores (3), and finally the bottom of the pores (4) [17].

$$C_{plane} = \frac{\kappa \varepsilon_0}{t_{dielectric}} \left[\left(\frac{\sqrt{3}}{2} \right) \left(2r_{pore} + D_{int} \right)^2 - \pi r_{pore}^2 \right]$$
(2)

$$C_{pore} = \frac{2\pi\kappa\varepsilon_0 L}{\ln\left[\frac{(r_{pore} - t_{BE})}{(r_{pore} - (t_{BE} + t_{dielectric}))}\right]}$$
(3)

$$C_{bottom} = \kappa \varepsilon_0 \frac{\left[r_{pore} - (t_{BE} + t_{dielectric})\right]^2}{t_{dielectric}}$$
(4)

The contribution of the cylindrical part of pores is the major input to the total capacitance of the supercapacitor device given by formula (5), while the top electrode thickness (t_{TE}) hardly influences the total capacitance of the supercapacitor, as it can be deduced from the Equations (2, 3, 4, and 5). Nevertheless, it needs to be thick enough to ensure good electrical contact and to protect the sample surface against external damage.

$$C_{total} \approx \alpha \left(C_{plane} + C_{pore} + C_{bottom} \right)$$
 (5)

Herein, we discuss about the fabrication and development processes, together the morphological, structural and electrical study of a prototype of electrostatic supercapacitor. The prototype of the device follows the same principle as conventional electrostatic capacitors, but takes advantage of the high open surface area of nanoporous alumina membranes and the reduced thickness and elevated dielectric constant of the insulating layer deposited by ALD. The CDC structure of the ESC was formed by successively deposited layers on top-surface of a typical NAAM having pore diameter (D_p) about 65 nm, 105 nm of interpore distance (D_{int}) and pore length (L) around 10 µm. The conductor and dielectric alternating layers forming the CDC structure of the ESC were chosen of Aluminum-doped Zinc Oxide (AZO), as the BE and TE electrodes, with respective thicknesses of 12 and 24 nm, together with an intermediate insulating alumina (Al₂O₃) layer having a dielectric constant between 7-9 and 10 nm in thickness. This ESC prototype exhibits a high capacitance value about $200 \,\mu\text{F/cm}^2$ at the frequency of 40 Hz, and a breakdown voltage about 4-5 V, while the leakage current present values close to 1.8 mA/cm² at 1 V. The high value of capacitance achieved in the supercapacitor prototype together with its small size makes these devices outstanding candidates for using in energy harvesting and storage applications.

Experimental

Fabrication of NAAM Templates

NAAM templates were fabricated starting from high-purity aluminum foil (99.999%, Goodfellow) with a thickness of 0.5 mm. Firstly, the sample was cleaned in isopropanol an ethanol. Then, the aluminum foils were electropolished in a two electrode electrochemical cell with a mixture of perchloric acid and ethanol (25:75 vol. %) at 5°C, under an applied voltaje of 20 V. The cathode was a Pt mesh counter electrode in the electrochemical cell and the aluminum foil was the anodic electrode. An alumina layer displaying a high aspect ratio honeycomb nanoporous structure was grown on top of the Al substrate, by following a well-known two step electrochemical anodization process in 0.3 M oxalic acid at a temperature between $1-3^{\circ}$ C at 40 V_{dc} , (**Figures 2A–D**), as reported elsewhere [32].

As a result, the NAAM template displays a highly spatial and periodically ordered distribution of the pores with hexagonal symmetry, having a pore diameter, D_p , about 35 nm, 105 nm of

interdistance among nanopores, D_{int} , and pore length, L, around 10 µm, resulting in a pore density about 1×10^{10} cm⁻² (**Figure 3**). Afterwards, the pores were widened by chemical etching in a weak dissolution of phosphoric acid (5 wt. %) during 35 min at 30°C, thus increasing D_p up to 65 nm. The pore widening aims to increase the pore size to contain the complete CDC structure constituting the electrostatic supercapacitor.

Optimization of ALD Growth Rates of Conductive BE, TE, and Dielectric Layers

In order to determine the growth per cycle ratio of AZO and Al₂O₃ layers, different thicknesses of these oxides were deposited on Si substrates under the same deposition conditions that were used for NAAM substrates. **Figures 4A,B**) show the respective layer thicknesses measured using ellipsometry (black triangles) and profilometry (blue squares) techniques. The thicknesse exhibits a lineal behavior with the number of cycles. The growth per cycle (GPC) of the AZO and Al₂O₃ layers in ALD expo mode are 0.188 \pm 0.002 nm/cycle and 0.127 \pm 0.001 nm/cycle, respectively, which are comparable values with that reported in the literature for similar deposition conditions to here employed [31, 33].



FIGURE 3 | SEM image on top surface of a typical NAAM after the two-step anodization processes, where it can be appreciated the self-ordered porous structure with honeycomb arrangement, together a cross section break showing the parallel aligned longitudinal nanochannels.



In this work, an Al doping ratio of 20:1 was chosen for the AZO films. Thus, the real concentration of Al follows the "rule of mixtures" at low dopant concentrations and it can be estimated through the expression:

$$%Al = \frac{GPC_{Al_2O_3}}{GPC_{Al_2O_3} + nGPC_{ZnO}}$$
(6)

Where *n* represents de number of ZnO cycles in the AZO supercycle. For the case of the AZO films with n = 20, the estimated %Al was 3.28%. This value of Al doping concentration can be considered the most appropriated according to other previous studies carried out to optimize the microstructure and therefore the electrical characteristics of the AZO films deposited by ALD, in order to obtain high degree of crystallinity, low resistivity and decrease in band gap of the conductive layer [33-35]. The measured resistivity of the AZO films was $1.5 \times 10^{-4} \,\Omega \cdot cm$, which is similar to the experimental values obtained in several reports [33, 34]. Higher Al contents in the AZO composition would increase the electrical resistivity due to the transformation of the conductor AZO film into insulator. In addition, it would also decrease the mobility and concentration of the charge carriers, thus reducing the electrical conduction properties of the AZO films [34].

CDC Layered Structure Deposited by ALD on Nanoporous Alumina Templates

The ESCs were prepared employing the ALD technique by coating the surface and inner pores of the starting NAAM template (**Figure 5A**) with a thin film of AZO as the bottom (**Figure 5B**) and top (**Figure 5D**) electrodes, respectively, and an Al_2O_3 layer as the intermediate dielectric (**Figure 5C**), as it is shown in the complete scheme displayed in the **Figure 5**.

The AZO and alumina thin layer depositions were performed in an ALD reactor (Savanah 100) at 200°C, using N₂ as the carrier and purging gas, and operating in exposure mode. This operating mode provides slower deposition processes as compared to the flow mode, but it is particularly suitable for conformal depositions on surfaces with high aspect ratio, as in the case of NAAM templates [36]. Trimethyl aluminum (TMA) and H₂O were used as precursors to deposit the Al₂O₃ layer at a deposition rate of 0.127 \pm 0.001 nm per cycle to grow a thickness of 10.17 ± 0.07 nm dielectric layer. The AZO films were composed of alternate 20 cycles of ZnO and 1 cycle of Al₂O₃. The precursors utilized to deposit AZO were DEZ (diethyl zinc), TMA and H_2O at a deposition rate of 0.188 \pm 0.002 nm per cycle. This provided thicknesses of 11.9 \pm 0.1 nm and 23.7 \pm 0.3 nm for the BE and TE, respectively. The trilayer structure CDC reaches a thickness of 45 nm, but due to the cylindrical shape of the pore, it constitutes a total thickness of 90 nm, filling completely



FIGURE 4 | Thickness of different AZO (A), and Al₂O₃ (B), films deposited on Si substrates. The thicknesses were measured by using ellipsometry (black triangles) and profilometry (blue squares) techniques.



the nanopore diameter of NAAM template, as it is depicted in **Figure 5D**).

Electrical Contacts

The separated electrical contacts for the bottom and top electrodes were fabricated by masking a part of the supercapacitor after the first deposition of the bottom electrode with Kapton tape. Afterwards, the dielectric and top electrode layers were deposited and after the CDC structure was completely deposited, the mask was then removed, therefore exposing the bottom electrode. Later on, both the bottom and top electrodes were contacted using a conductive epoxy resin to make two electrical contacts by separately.

Microstructure and Electrical Characterization

Material characterization was carried out using a JEOL 6610 LV SEM (Scanning Electron Microscopy) and JEOL JEM 2100 TEM (Transmission Electron Microscopy), proving the deposition conformality and layer thicknesses. Structure and compositional characterizations were conducted using an X-Ray diffractometer and STEM (Scanning Transmission Electron Microscopy). Prior to TEM and STEM characterization, the NAAM coated with the CDC structure, was thinned by ion milling with Ar on the upper and lower sides of the nanocapacitor, employing a Gatan 691 Precission Ion Polishing System, operated at 3– 5 kV. Resistivity measurements of conductor AZO films were performed with a four-point probe. Device capacitance and electrical impedance were measured with an Agilent 4294a LCR meter at frequencies ranging between 40 Hz and 100 MHz, and applying 500 mV (AC). Likewise, the leakage current and the breakdown voltage measurements were carried out by means of a homemade experimental setup consisting of a DC power supply model Keithley 2400 Source Meter, a variable resistor and the supercapacitor prototype, all together connected in series. For each leakage current measurement performed at any certain value of voltage, it has been waited long time enough (about 1 min) in order to ensure the stabilization of the leakage current value.

Results and Discussions

SEM images shown in **Figure 6** summarize the top-view surface evolution of the pore diameter during the successive ALD depositions of conductive and dielectric layers of the CDC engineered structure that constitutes the electrostatic supercapacitor prototype, starting from the initial NAAM template displayed in **Figure 6A**). The first conductive thin layer was formed by 63 cycles of AZO as the BE (**Figure 6B**), followed by 80 Al₂O₃ cycles as the dielectric layer (**Figure 6C**), and finally 126 cycles of AZO as the TE (**Figure 6D**), which verified the correct deposition rates for the different CDC layers. Moreover, the thickness measured for the AZO layer at the BE was $t_{BE} = 10 \pm 2$ nm and the corresponding one for the Al₂O₃ dielectric layer was $t_{dielectric} = 8 \pm 3$ nm. These layer thicknesses values were in good agreement with the fitted ones estimated from the AZO and Al₂O₃ GPC.



FIGURE 6 | SEM top view images of NAAM templates showing the evolution of the pore diameter after successive ALD depositions for the supercapacitor prototype. (A) top view of the starting NAAM before the ALD process; (B) after deposition of 63 cycles of AZO as the

BE; **(C)** top surface of nanopores after deposition of the BE and 80 cycles of Al_2O_3 dielectric layer; **(D)** SEM image after deposition of the complete CDC structure (63 cycles BE + 80 cycles dielectric layer + 126 cycles TE).



TEM top-view images displayed in **Figures 7A,B**), that were taken from samples after ion milling of the top and bottom sides of the CDC structure, confirmed the existence of three concentric layers with the expected spatial distribution and thicknesses near the values calculated from the GPC. The contrast differences in the images are due to the different density of both materials: AZO electrodes mainly composed of ZnO (density of $5.61 \text{ g} \cdot \text{cm}^{-3}$), and the Al₂O₃ in the NAAM and dielectric layer (density of $3.95 \text{ g} \cdot \text{cm}^{-3}$). Moreover, STEM mode image (**Figure 7C**) and compositional analysis profile (**Figure 7D**) confirm the existence of three concentric layers from the pore

center: AZO top electrode, next to dielectric layer of Al_2O_3 and finally the layer of AZO constituting the bottom electrode. These experimental results evidence the CDC morphological structure of the engineered ESC, as schematically described in **Figure 5**.

By analyzing with more detail the inner part of the pores, the crystalline structure of the AZO top electrode can be evidenced in the HR-TEM analysis shown in **Figure 8A**). X-Ray diffraction analysis shown in **Figure 8B**), displays the diffraction peaks corresponding to aluminum substrate and zinc oxide. However, there are not peaks coming from the alumina due



FIGURE 8 | (A) TEM image of the inner pore shows the crystalline structure of AZO films, inset corresponds to the SAED (Select Area Electron Diffraction) analysis; (B) X-Ray diffraction pattern study of the supercapacitor device surface.



to its amorphous structure. Using the width of the zinc oxide peaks and the Scherrer equation [37], it is possible to calculate the grain size of AZO nanocrystals, obtaining a value of 5.6 \pm 0.6 nm. This value is in agreement with the data extracted from the selected area electron diffraction spectra (SAED) and the high resolution TEM image displayed in **Figure 8A**). The AZO crystallinity is related with an enhancement of the electrical conductivity and improves the properties of capacitor electrodes.

The impedance measurements shown in **Figures 9A,B**, display the module of impedance and phase behavior for the supercapacitor prototype and its comparison with a typical commercial capacitor, in the wide frequency range of 40 Hz up to 110 MHz. The impedance module decreases at low frequencies until it reaches the supercapacitor resonance frequency at about 2.5 MHz. When frequency increases, the module of the impedance rises up and the supercapacitor exhibits an inductive behavior at high frequencies. This is also the typical behavior of the impedance in a conventional capacitor, while the values for the module of the impedance and its resonance frequency are both lower than the corresponding ones compared with the supercapacitor prototype.

On the other part, negative values for the phase of the impedance are reached at frequencies below that of the supercapacitor resonance, while at frequencies close to 40 Hz the phase of the impedance takes anomalous negative values, but that does not reach -90° , as it would be expected for a conventional capacitor, also displayed in the **Figure 9B**. Nevertheless, for frequencies higher than the resonance frequency, the impedance phase increases reaching positive values, which is characteristic of an inductive behavior. The unusual phase performance at low frequencies could be due to a high device leakage current (**Figure 10A**), which provokes a strong resistive contribution in the supercapacitor prototype behavior at frequencies near 40 Hz.

Additionally, the frequency variation of the capacitance of the device, which is shown in **Figure 9C**, has been estimated with the LCR meter by modeling the supercapacitor behavior with an equivalent circuit composed by a capacitor, a resistance and an inductance all together connected in series. This basic equivalent circuit is commonly used to represent the performance of the conventional capacitors. Maximum capacitance value about $200 \,\mu\text{F/cm}^2$ is reached at the frequency of 40 Hz, which decreases drastically when the measurement frequency is increased. This



property indicates that the future device applications should be focus on the low frequency range where the supercapacitor prototype exhibits the largest electrical energy storage properties. Furthermore, by using the Equations (2–5), it is also possible to calculate a theoretical value of the device capacitance, by introducing the morphologic parameters of the studied ESC prototype ($r_{pore} = 65 \text{ nm}$; $D_{int} = 105 \text{ nm}$; $L = 10 \,\mu\text{m}$; $\alpha = 1 \times 10^{10} \text{ cm}^{-2}$; $t_{BE} = 11.9 \text{ nm}$; $t_{dielectric} = 10.17 \text{ nm}$). The estimated calculation of the capacitance gives a result of $201 \pm 20 \,\mu\text{F/cm}^2$, which is in good agreement with the capacitance value obtained from the LCR approach.

In spite of that, the anomalous phase behavior displayed by the impedance at low frequencies, together the high resistance value obtained, suggests that the LCR equivalent circuit chosen to represent the behavior of the supercapacitor prototype may not be the most appropriate for modeling the impedance response of the supercapacitor device in this frequency range. Due to the complex engineered structure of the device/sample, the impedance behavior of the prototype should be adjusted with another more complicated model of equivalent circuit composed of serial and/or parallel associations of resistors and capacitors, as those reported in the literature for other similar prototypes of supercapacitor devices [38–40].

Leakage current of the supercapacitor device was measured for different applied voltages, obtaining a linear behavior with high leakage current values of 1.7 mA/cm² at voltages up to 1 V, as it can be seen in Figure 10A). The obtained leakage current values are high, which may be a handicap for applications of this ESC prototype in long-term energy storage applications. The origin of such high leakage current values could be due to the existence of local defects in the CDC structure, or chemical impurities that increase the conductivity of the dielectric alumina layer, as well as the strong electric field localized at the sharp tips of the membrane surface. However, different strategies can be further explored to improve this feature of the ESC prototype, such as by increasing the thickness and uniformity of the dielectric layer, by introducing a passivation layer or an anodic alumina barrier to soften the NAAM profile and get avoided the electrical losses due to the sharp tips on the membrane surface [12, 18].

Finally, the characteristic current-voltage curve (I-V) shows a breakdown voltage about 5 V, as it can be shown in Figure 10B. On the upwards curve slope of the characteristic I-V representation, it is noticed that the current increases forcefully at this value of voltage, indicating the completely dielectric breakdown in the device. However, in the marked area between the two discontinuous bars, it is possible to appreciate that the dielectric breakdown is not abrupt, but it seems to take place gradually by breaking different parts of the dielectric layer as the voltage is continuously increased, which is consistent with the parallel arrangement of individual nano-capacitors embedded in the NAAM template. Nevertheless, on the slope of the descending curve it can be observed a higher current flow through the supercapacitor prototype as compared with the upward curve, clearly indicating the dielectric breakdown and hence, an irreversible damage in the supercapacitor prototype ability for storing the electrical energy.

Conclusions

In summary, we report on the fabrication and characterization of ESCs by ALD conformal deposition of a CDC engineered structure on the high open surface of a NAAM as template. The excellent conformality of both deposited conductive and dielectric layers, together with their composition and crystalline structure have been checked by means of different XRD and electron microscopy techniques. The complete electric characterization was carried out in the frequency range of 40 Hz up to 100 MHz by using a LCR impedance analyzer. It is found that the capacitance per unit area decreases strongly with the frequency, but at the low frequency of 40 Hz it reaches about $200 \,\mu$ F/cm². This result is well correlated with the theoretically calculated capacitance according with the geometric structure of the ESC prototype. Additionally, the frequency dependence of the impedance module and phase indicate that ENCs follow a frequency behavior similar to commercial capacitors, but showing enhanced capacitance areal density. This comprehensive study is particularly interesting because the electrostatic capacitors can usually exhibit higher power densities than compared to batteries, but their capacitive properties do not degrade over the time such as the electrolytic capacitors. Looking forward it becomes necessary to improve the features of the ESC prototype device in order to minimize the leakage current and breakdown voltage, thus optimizing the impedance behavior and power density of the supercapacitor, but without sacrificing the energy storage density of the device.

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Conflict of Interest Statement: The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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