frontiers | Frontiers in Neuroscience

TYPE Review
PUBLISHED 05 October 2023
DOI 10.3389/fnins.2023.1253075

OPEN ACCESS

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RECEIVED 04 July 2023
ACCEPTED 13 September 2023
PUBLISHED 05 October 2023

CITATION
R RT, Das RR, Reghuvaran C and James A (2023) Graphene-based RRAM devices for neural computing. *Front. Neurosci.* 17:1253075. doi: 10.3389/fnins.2023.1253075

Graphene-based RRAM devices for neural computing

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Resistive random access memory is very well known for its potential application in in-memory and neural computing. However, they often have different types of device-to-device and cycle-to-cycle variability. This makes it harder to build highly accurate crossbar arrays. Traditional RRAM designs make use of various filament-based oxide materials for creating a channel that is sandwiched between two electrodes to form a two-terminal structure. They are often subjected to mechanical and electrical stress over repeated read-and-write cycles. The behavior of these devices often varies in practice across wafer arrays over these stresses when fabricated. The use of emerging 2D materials is explored to improve electrical endurance, long retention time, high switching speed, and fewer power losses. This study provides an in-depth exploration of neuro-memristive computing and its potential applications, focusing specifically on the utilization of graphene and 2D materials in RRAM for neural computing. The study presents a comprehensive analysis of the structural and design aspects of graphene-based RRAM, along with a thorough examination of commercially available RRAM models and their fabrication techniques. Furthermore, the study investigates the diverse range of applications that can benefit from graphene-based RRAM devices.

KEYWORDS

chemical vapor deposition (CVD), cryptography, graphene, neuromorphic computing, resistive random access memory (RRAM)

1. Introduction

Graphene-based resistive random access memory (RRAM) devices have gained significant attention in recent years for their potential applications in neural computing. Graphene, a two-dimensional carbon material, has exceptional electrical and mechanical properties, making it an attractive candidate for RRAM devices. RRAM is considered one of the most promising emerging non-volatile memory, a potentially universal memory device that comes under the broad category of memristive systems (Meena et al., 2014). The advantage of RRAM is attributed to the ease of fabrication of a two-terminal structure that can be used to create efficient crossbar arrays, high read speeds, and low area overheads. The RRAMs in the crossbar can emulate multiply and accumulate (MAC) computations that are universal operations essential for implementing neural computations.

RRAM is a memory based on a resistive switching mechanism where the conducting filament is created and broken due to a change of external voltage (Yu et al., 2011a). The binary RRAMs operate in two states: low resistance state (LRS) and high resistance state (HRS). Various types of electrodes and metal oxides can be used for RRAM structure. Titanium, hafnium, silicon, germanium, and nickel are the most common oxide materials, whereas silicon, silver, indium, and tantalum are familiar electrode materials used in RRAM memory devices.

Unfortunately, RRAM memory devices face various limitations with the aforementioned electrode and oxide materials (Zhu et al., 2015). For accomplishing the resistive switching property, the electrode, and conducting filament can be modified with a wide variety of materials. The electrode materials used for RRAM are divided into the following five categories: (i) elementary substance electrodes, (ii) silicon-based electrodes, (iii) alloy electrodes, (iv) oxide electrodes, and (v) nitride-based electrodes (Zahoor et al., 2020). Depending on the electrode material, the number of possible states in the RRAM varies (Prakash and Hwang, 2019). As the number of states increases, the device finds application as an analog data storage device.

In RRAM, the graphene-related materials have been incorporated to increase the switching speed, retention time, endurance, and power consumption to improve the performance as a non-volatile memory (Rehman et al., 2020). Graphene provides additional properties such as transparency, flexibility, enhanced heat dissipation due to the high thermal conductivity of graphene, and chemical stability. Other than these properties, as a two-dimensional system, graphene can provide more than two states for the memristive device in implementing synapses for neuromorphic computing. It is reported that till now more than 16 states are possible with graphene in the memristive system (Schranghamer et al., 2020). Building more than two stable states in RRAMs to form analog computing systems or using them for analog storage is a open problem in RRAM-based systems.

With graphene-enabled RRAMs, it is expected that the higher number of states can improve the storage density and improve the reliability of the device. Graphene-enhanced RRAM exhibits faster switching speeds and enduring performance due to high carrier mobility, and the unique two-dimensional structure minimizes filament variability, ensuring stable set/reset processes in RRAM devices. Exceptional thermal and mechanical stability of graphene boosts RRAM features by optimizing performance across varying conditions (Galashev and Rakhmanova, 2014; Pan et al., 2017; Rehman et al., 2020). It is reported that RRAM devices offer a switching speed of less than 10 ns, power losses of about 10 pJ, lower threshold voltage of less than 1V, long retention time of greater than 10 years, high electrical endurance with more than 10^8 voltage cycles, and extended mechanical robustness of 500 bending cycles. These advantages are complemented by its ability to tolerate high-temperature variations. Graphene as an interface layer acts as a resistive switching medium which help to minimize power dissipation with low contact resistance. Graphene helps to optimize the surface effect such as photodesorption and chemisorption which are varied due to the increase and decrease of the temperature.

This review starts with an overview of neuro-memristive computing, graphene, and its synthesis techniques. Furthermore, the RRAM, working principle, and the resistive switching mechanism are discussed. The incorporation of graphene and graphene oxide in RRAM as an electrode, and the middle layer is elaborated in detail. The role of graphene in RRAM, to enhance the properties such as endurance, and retention is analyzed, and the enhancement in flexibility and transparency is discussed. The progress of multilevel cell storage in RRAM is reviewed in detail. Furthermore, the commercially available RRAM models and their fabrication methods, complementary metal-oxide-semiconductor (CMOS) compatibility with RRAM are also discussed.

2. Neuro-memristive computing

2.1. Memristive devices and neural dynamics

Memristive devices have been studied for their potential to create artificial neural networks that can learn and adapt in a manner similar to biological neural networks (Huang et al., 2020). These devices can be used to build artificial synapses that can modify their strength based on the pattern of electrical signals they receive. This is similar to how biological synapses modify their strength in response to the timing and frequency of incoming electrical signals (Zhang et al., 2023). Based on this, one potential application of memristive devices in neural dynamics is in the development of neuromorphic computing systems (Ma et al., 2018). These systems are designed to mimic the way the brain processes information, and memristive devices could provide a way to build artificial neural networks that are more efficient and flexible than traditional computing systems (Shehab et al., 2022). This section will cover the details of different kinds of memristive devices, their working, and their viability for application in neuromorphic computing systems.

Memristor is one kind of two-terminal device, considered a new-generation non-volatile memory (NVM) device. This new computing system proposed by Sano et al. (2013) can store information by changing the resistance of a material, whereas conventional memory devices program data by change of capacitance (Im et al., 2020). A pinched hysteresis loop is a characteristic feature of a memristor. The loop represents the behavior of the memristor as the voltage or current applied to it is varied as shown in Figure 1. The pinched hysteresis loop is a distinctive characteristic of memristors and distinguishes them from other electronic devices such as resistors, capacitors, and inductors. The pinched hysteresis loop arises due to the inherent properties of the memristor's material and structure, which allow it to exhibit memory and resistance variations based on the history of applied voltage or current. The exact shape and characteristics of the loop depend on the specific properties of the memristor, including its materials, fabrication methods, and operating conditions. The pinched hysteresis loop of a memristor has significant implications for applications in areas such as memory devices, neuromorphic computing, and analog signal processing. It enables the memristor to store information based on its resistance state and offers unique opportunities for non-volatile memory and computing architectures. The conventional memristor model and its symbol are shown in Figures 2A, B.

These devices offer several advantages over conventional memory technologies such as flash, dynamic random access memory (DRAM), and static random access memory (SRAM), including high density, low power consumption, and fast switching speeds (Yang and Williams, 2013). The combination of metal electrodes and insulators constructs a memristor configuration. The schematic diagram of the cross-point device, showing metallic

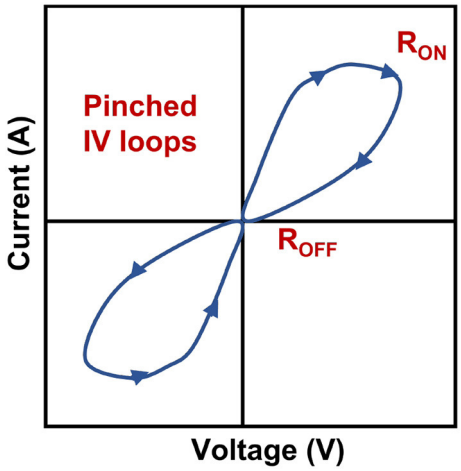

FIGURE 1
Example of pinched hysteresis loop of memristor.

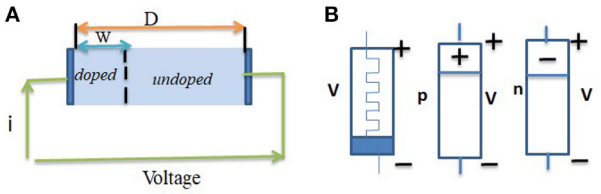

FIGURE 2
(A) Memristor model according to Strukov et al. (2008). **(B)** Traditional symbol, p-type and n-type memristors (copyright Starzyk et al., 2014).

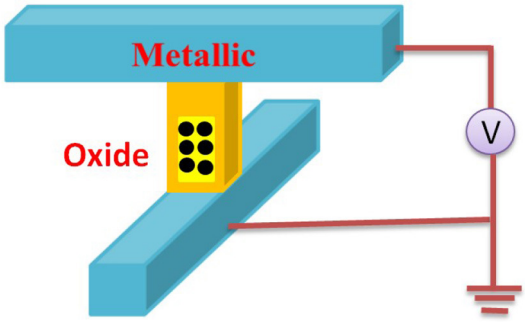

FIGURE 3
Schematic of the cross-point device, showing metallic top and bottom electrodes, and switching oxide (Yang and Williams, 2013).

top and bottom electrodes and switching oxide is shown in Figure 3. Resistive switching, phase change, spintronics ferroelectric, etc. are the various kinds of properties of memristor devices that are contributing to the development of emerging electronic technologies. Among them, a resistive switching memristor (RSM) is the most common memristive device which has low power consumption, high endurance, and potential for use in neuromorphic computing (Prodromakis and Toumazou, 2010; Yu et al., 2018). The applied voltage to the electrodes in the RSM device creates an electric field across the metal oxide layer, causing a change in the oxidation state of the material. This oxidation state changes the resistance of the material which can be detected and used to store data. Phase change element based phase change memory (PCM) is another type of memristive device that uses a material to change its physical state between a crystalline phase (low resistance) and an amorphous phase (high resistance) in response to heat or electric current. Spintronics memristors are a new type of magnetic RAM (MRAM) that works on magnetic tunnel junction (MTJ) (Xue et al., 2011) and offers high speed and high endurance performance. The resistance value has changed due to the spin of the electron and the storage of the data. Two ferromagnetic layers (FM) of these devices are separated by a non-magnetic (NM) layer. When an electric current is applied to the device, the spin of electrons in the magnetic layers is affected, causing a change in the resistance of the device. Ferroelectric tunnel junction (FTJ) (Ambriz-Vargas et al., 2017) is the most significant ferroelectric memory device for neuromorphic computation, having an insulating layer in between two metal electrodes. This ferroic nanostructure is comprised of an ultra-thin ferroelectric barrier, and its dominant mechanism is quantum electron tunneling. In this structure, electrons are able to penetrate through the potential barrier of the ultra-thin insulator. As research in this field continues to progress, memristive devices are expected to play an increasingly important role in the development of advanced computing and memory technologies.

Memristive devices are of great interest in the field of neuromorphic computing because they can be used to emulate the synaptic connections between neurons in the brain. The neural dynamics of memristive devices refers to the behavior of these devices when they are used to implement neural networks. When memristive devices are used as synapses in a neural network, their resistance values change over time in response to the input signals that they receive (Boybat et al., 2018). This behavior can be used to implement learning in the neural network, allowing it to adapt to new inputs and improve its performance over time. The dynamics of memristive devices in neural networks are highly non-linear and can be difficult to predict (Brivio et al., 2021). However, researchers have developed models and simulations to study the behavior of these devices in neural networks.

2.2. Memristors in crossbar

Memristors in crossbar arrays are a type of non-volatile memory technology that holds promise for high-density, low-power, and high-speed computing applications (Xia and Yang, 2019). In a crossbar array, memristors are arranged in a grid pattern, with one set of wires running vertically and another set of wires running horizontally, forming a series of intersecting points. At each cross-point, a memristor can be programmed to either a high or low resistance state, representing a binary 1 or 0, respectively. By applying voltage to the appropriate sets of wires, the resistance state of the memristor can be read or written. This allows for parallel access to multiple memory cells, making crossbar arrays

a potential solution for memory-intensive tasks such as machine learning and artificial intelligence.

A single memristor or one-transistor/one-resistor (1T, 1R) memristor array typically refers to a configuration where memristors are organized in a regular grid pattern. The purpose of a single memristor array is to enable the simultaneous operation and interconnection of multiple memristors (Xu et al., 2021). In a 1T, 1R memristor array, each memristor is paired with a transistor. The transistor serves as the access device or switch, allowing individual memristors within the array to be addressed and read or written to Kim et al. (2012). The key advantage of a 1T, 1R memristor array is its high density and potential for low-power operation. By combining the storage element (memristor) and the access device (transistor) into a single unit, the overall footprint of the memory array can be reduced. There are various ways to arrange the memristors, depending on the desired application and circuit design (Lu et al., 2022). The two-memristor crossbar array is a grid-like structure where the two memristors are positioned at the intersection of a row and a column. The rows and columns are connected to input and output nodes or other circuit elements. This configuration is commonly used in memristive crossbar arrays, where the resistance states of the memristors can be manipulated to enable or disable the connections between rows and columns (Vourkas et al., 2016). Crossbar arrays are particularly relevant in applications such as memory arrays, neural networks, and digital logic circuits (Li et al., 2021). In a bridge memristive crossbar array, two memristors are connected in series between two nodes, forming a bridge structure. The nodes can represent inputs, outputs, or intermediate connections in a larger circuit. The bridge configuration allows for specific control over the flow of current or signals through the array. By adjusting the resistance states of the individual memristors in the bridge, it is possible to selectively enable or disable the connection between the two nodes. This can be achieved by applying appropriate voltage or current across the bridge.

Memristors in crossbar arrays also have the potential for use in neuromorphic computing, which seeks to emulate the structure and function of the human brain (Xia and Yang, 2019). Memristor-based crossbar arrays can potentially perform tasks such as pattern recognition and decision-making in a highly efficient and parallelized manner. Starzyk et al. (2014) developed a novel neural network architecture that utilizes a compact crossbar layout of memristors, which allows us to preserve a high density of synaptic connections. Yakopcic et al. (2019) studied a memristor-based neuromorphic system for ex-situ training of multi-layer perceptron algorithms. This technique facilitates the direct translation of neural algorithm weights onto the resistive grid of a memristor crossbar. It is observed that a parallel crossbar improves the speed and power dissipation. Hu et al. (2012b) proposed a memristive crossbar array for high-speed image processing. It exhibits automatic memory, continuous output, and high-speed parallel computation, making it well suited for implementation in VLSI (very large-scale integration) technology. Huang et al. (2021) developed a vertical crossbar MIM (metal insulator metal) RRAM device for neuromorphic computing that is based on the 2D material $ReSe_2$. This design has been shown to exhibit improved accuracy when used in brain-inspired neuromorphic computing systems.

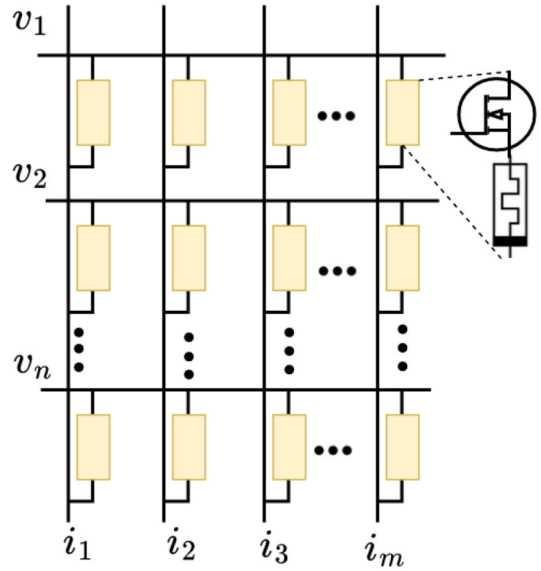

FIGURE 4
ITIM configuration for implementing DNN neural network.

2.3. Neuro-memristive architectures

The memristive circuits and computing architectures are one of the promising solutions for implementing neuromorphic computing. The memristor implementations provide various advantages such as scalability, on-chip area and power reduction, efficiency, and adaptability, especially for device scale-up architectures. There are existing different memristive neuromorphic architectures in the literature used for edge computing applications. The section reviews the most popular neural architectures for edge computing applications.

2.3.1. Deep neural network (DNN)

The DNN is implemented using memristor crossbar arrays. Each DNN layer is implemented using one transistor/memristor (1T 1M) configuration as in Figure 4. Each layer consists of M word lines (WLs) and N bit lines (BLs). The transistor switch enables or disables the column-wise memristor nodes. In Figure 4, v_1, v_2, ... v_n from the inputs, conductance $g_{i,j}$ of memristors as weights and columns current $i_1, i_2, \ldots i_m$ as outputs, where i, j are the coordinates of the crossbar node. The output currents indicate the weighted summation of input voltages. The bias is included as an additional input line.

2.3.2. Convolutional neural network (CNN)

There are several analog memristive crossbar implementations of CNN architecture (R et al., 2022). Figure 5 shows the hardware

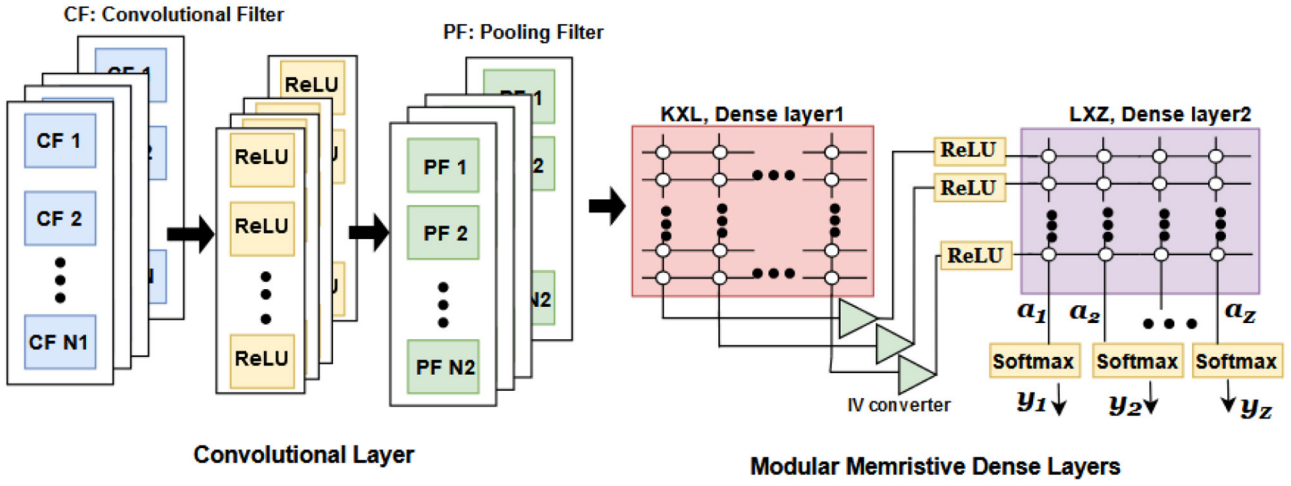

FIGURE 5
CNN implementation using memristor crossbar arrays (R et al., 2022).

implementation of CNN consisting of a convolution layer, mean pooling layer, and dense layers. The convolution filters are realized as memristive crossbars. The conductance of memristive devices is the trained weights of the convolutional filter (CF). The number of memristors in each layer is determined by the required feature maps. The features are then fed to the pooling layer circuit. The pooling layer reduces the dimensionality by performing mean-pooling operation (R et al., 2022). The output of the mean-pool operation is flattened and is connected to dense layers for classification. The current-to-voltage (IV) converter block is used to convert currents to corresponding voltages. The activation functions used are ReLU (rectified linear unit) and softmax.

2.3.3. Cellular neural network (CeNN)

The CeNN is developed by Chua and Yang by mimicking the features of neural networks and cellular automata finds applications in the area of image processing (Chua and Yang, 1988a,b). The CeNN network in Figure 6 consists of $I \times J$ cells. Each cell is connected only to its neighboring cells. The connections from each cell $C(i, j)$ to its neighbors is defined by cloning templates, $A(i, j; k, l)$ and $B(i, j; k, l)$, for feedback and feedforward connections (Chua and Yang, 1988b; Duan et al., 2015). The input signal U is connected to $C(i, j)$ through the feedforward weights $B(i, j; k, l)$. The output of the cell $y_{k,l}$ is fed to $C(i, j)$ through the feedback weights $A(i, j; k, l)$. The state equation can be mathematically expressed as Chua and Yang (1988b).

$$\frac{dx_{i,j}}{dt} = -x_{i,j} + \sum_{c_{k,l}} A(i, j; k, l) y_{k,l} + \sum_{c_{k,l}} B(i, j; k, l) u_{k,l} + I_b, \quad (1)$$

where I_b is the bias current, $x_{i,j}$ is the cell state, and $y_{i,j}$ is the output, respectively. There are various memristive implementations of CeNN in the literature (Duan et al., 2015; Hu et al., 2016). In Figure 6, the feedback and feedforward connections in the CeNN network are implemented using memristor crossbar arrays.

2.3.4. Recurrent neural network (RNN)

The recurrent neural networks-based methods demonstrated outstanding ability in prediction tasks using time-series data by combining large dynamical memory and adaptable computational capabilities. Long short-term memory (LSTM), the special configuration of RNN, is aimed at overcoming the vanishing gradient problems in conventional RNN (Adam et al., 2018). The memristive hardware implementation is presented in Figure 7A (Adam et al., 2018). The input data to the network is the concatenation of input data x_t, data from previous cell h_{t-1} and b_t. The input is multiplied by a weight matrix which is the programmed conductance value of the memristor crossbar array. The crossbar outputs are the input to the activation functions (either sigmoid or hyperbolic tangent) to get the gate values. f_t is the output value of forget gate, $i(t)$ is the output of input/update gate, $o(t)$ denotes the output from the output gate, and $c(t)$ denotes the cell state.

The calculation time in LSTM is very heavy and time-consuming. Echo state network (ESN), a reservoir computing architecture, has emerged as an alternative to the gradient descent training method for RNN (Yu et al., 2022). ESN consists of an input layer where the inputs are associated with a weight matrix w_{in}, followed by a recurrent and sparsely connected reservoir using weight matrix w_{res} and finally, a readout layer associated with a weight matrix w_{out}. The memristive architecture of the ESN reservoir layer is shown in Figure 7B. In ESN, the output readout layer is only trained, and the input and reservoir weight matrices are randomly generated and fixed throughout. The input weights are sampled from a uniform distribution $u(-a, a)$, using a scaling factor a and not trained. The weights of the reservoir are sampled from $u(-1, 1)$. Hence, the ESNs are conceptually simple and practically easy to implement.

2.3.5. Spiking neural network (SNN)

The main advantage of SNN hardware implementation is reduced power dissipation in comparison with the pulse-based

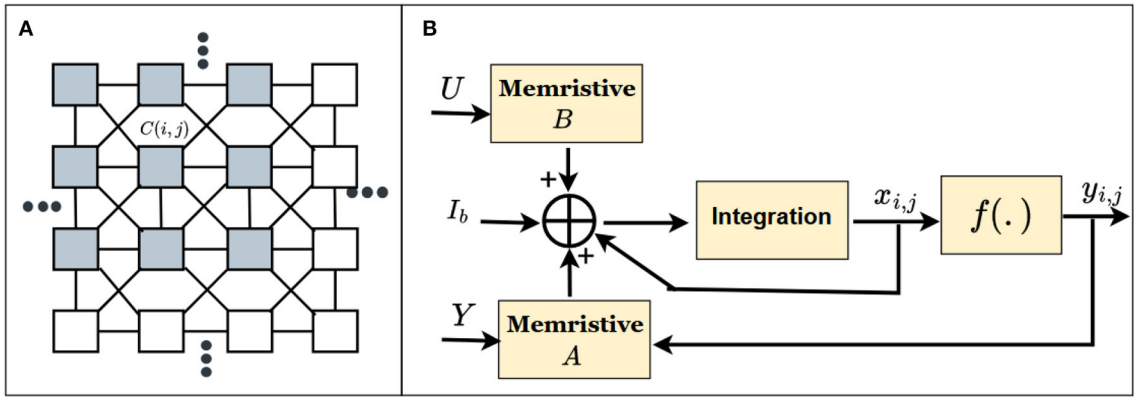

FIGURE 6
(A) Structure of CeNN and **(B)** CeNN implementation using memristor crossbar array (Hu et al., 2016).

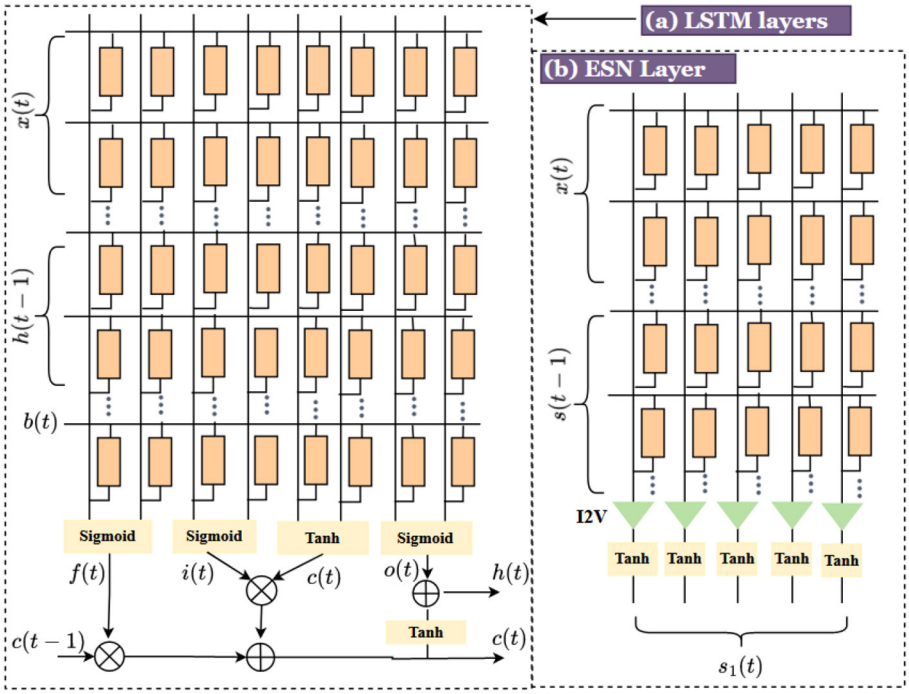

FIGURE 7
(a) Memristive crossbar LSTM architecture (Adam et al., 2018), **(b)** ESN architecture.

systems. The data signals are transmitted as spikes in SNN. The SNN is based on the emulation of brain processing using particular spike events represented by spike-timing-dependent plasticity (STDP). STDP is based on presynaptic and postsynaptic impulses. The implementation of SNN architectures with STDP using memristive crossbar arrays is presented in Figure 8. The architecture consists of presynaptic and postsynaptic neurons connected through memristor crossbar arrays. Most cases use a winner-takes-all (WTA) approach for implementation (Wu et al., 2015b). Recent studies introduce stochasticity by adding noise to WTA architecture (Bill and Legenstein, 2014; Krestinskaya et al., 2020). Stochasticity introduces the biological concept of the probabilistic behavior of neurons in the brain.

As discussed in the section, the field of neuromorphic computing using memristor crossbar arrays is advancing and the exploration of novel materials and devices for in-memory computing is required to improve efficiency and scalability. The RRAM devices are promising candidates for synapses and neurons in neuromorphic circuits. The analog tunable capability of RRAM devices enables novel computing functions for the realization of neuromorphic computing. The material class for RRAM devices is from magnetic alloys, metal oxides, 2D materials, and organic materials. Existing studies in the literature report

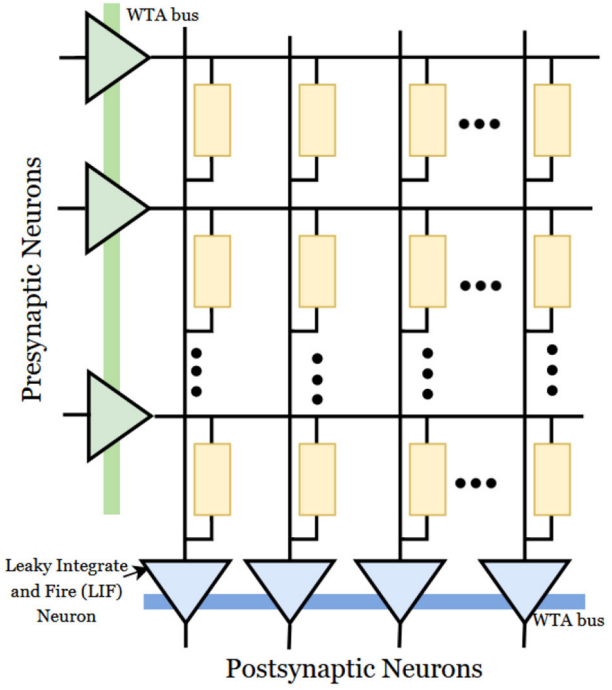

FIGURE 8
Memristive spiking neural network (Wu et al., 2015b).

that 2D material-based RRAM devices have better properties compared to conventional electrode materials which enhances the characteristics of RRAM in such a way to improve its application in neural computing. The coming section reviews the mechanism of the working principle of RRAM and the use of 2D materials for enhancing the properties are discussed in detail.

3. Graphene and 2D materials based RRAM for neural computing

Graphene and other 2D materials have the potential to revolutionize neural computing due to their unique electrical, mechanical, and optical properties. Graphene is a single layer of carbon atoms arranged in a hexagonal lattice, and it is a highly conductive and transparent material. Other 2D materials, such as transition metal dichalcogenides (TMDs) and hexagonal boron nitride (h-BN), also exhibit interesting properties that make them promising for use in neural computing (Zhang et al., 2022).

TMDs have gained significant attention in recent years due to their unique properties and potential applications in various fields, including neural computing. TMDs are a class of materials composed of transition metals (such as molybdenum or tungsten) and chalcogen elements (such as sulfur or selenium). TMDs can be used to create synaptic devices, which are fundamental building blocks of artificial neural networks (Cao et al., 2021). TMDs exhibit excellent electrochemical properties, allowing them to function as efficient and reliable synapses. By controlling the electrical current through TMD-based synaptic devices, the strength of synaptic connections can be modulated, mimicking the synaptic plasticity observed in biological neural networks (Sung et al., 2022). TMDs can also be utilized in the development of neuromorphic computing systems. These systems offer advantages such as parallel processing, low power consumption, and efficient data processing (Lu et al., 2023). TMD-based devices can be integrated into neuromorphic architectures to perform tasks such as pattern recognition, data analysis, and decision-making (Ko et al., 2020).

Another 2D material suitable for neural computing is h-BN (Xie et al., 2022). h-BN is a two-dimensional material, similar to graphene, but with insulating properties. It can serve as a platform for fabricating electronic components, such as transistors, interconnects, resistive memory, and sensors, with potential applications in neural computing. h-BN has been explored as a material for developing neuromorphic devices that can emulate the behavior of biological neurons. The two-dimensional nature of h-BN allows for the integration of multiple components into compact and efficient architectures.

Graphene-based electrodes have been shown to be biocompatible and capable of recording neural signals with high resolution and sensitivity. Additionally, graphene-based transistors have demonstrated fast switching speeds and low power consumption, making them suitable for use in neural signal processing. Another potential application is in the development of neuromorphic computing, which aims to mimic the structure and function of the human brain (Schranghamer et al., 2020). Graphene and other 2D materials can be used to create artificial synapses, which are the connections between neurons that allow them to communicate with each other. The details of fabrication techniques and applications of 2D materials are shown in Table 1.

Overall, graphene and other 2D materials and their combinations hold a great promise for advancing the field of neural computing and could lead to the development of more efficient and powerful neural interfaces and neuromorphic computing systems. Among the 2D materials, the present review focuses mainly on the role of graphene and graphene oxide for RRAM for application in neural computing. There are still many challenges to overcome, such as improving the scalability and reproducibility of these materials and devices, before they can be widely adopted in practical applications (Lin et al., 2016). In this section, the importance and synthesis methods of graphene are discussed in brief and a detailed analysis on the structure and working principles of RRAM is included for a better understanding of the applications of graphene-based RRAM in neural computing.

3.1. Properties of graphene and the different methods for its synthesis

Graphene is a 2D material made up of a single layer of sp^2 hybridized carbon atoms, arranged in a hexagonal lattice. The one atomic layer thickness makes graphene lightweight and flexible. The strong atomic bonding with the nearest carbon atoms provides high mechanical strength to the system, greater than that of steel. Many of these properties vary based on the quality of graphene synthesized. Figure 9 shows the classification of graphene synthesis methods prevalent today. The most popular approaches include those as follows:

TABLE 1 Review on 2D materials for neuromorphic computing applications.

Sl no.	References	2D Material	Fabrication method	Target application	switching voltage
1	Schranghamer et al. (2020)	Graphene	Chemical vapor deposition (CVD)	High precision neuromorphic computing	5.5 V
2	Qian et al. (2016)	h-BN	CVD	Resistive memory	0.72 V
3	Xu et al. (2019a)	MoS_2	MOCVD	Synapse	0.2 V
4	Kumar et al. (2019)	WS_2	RF sputtering	Memristors	1.6 V
5	Krishnaprasad et al. (2019)	MoS_2/ Graphene	CVD	Synapse	1V
6	Liu et al. (2012)	MoS_2/r-Graphene oxide	Liquid exfoliation	Resistive memory	3.5 V

1. Chemical vapor deposition (CVD) - The copper or nickel substrate is heated in a reactor chamber while introducing a hydrocarbon gas (such as methane) to the chamber. These hydrocarbons react with the substrate to form graphene.
2. Epitaxial growth - Substrates similar to crystal structure of graphene [e.g., silicon carbide (SiC) or hexagonal boron nitride (h-BN)] can be used to grow graphene for obtaining epitaxial growth via CVD process.
3. Mechanical exfoliation - The bulk crystal graphite consists of multiple layers of graphene. These layers are peeled off using tape or a sharp object.
4. Electrochemical exfoliation - The electrolyte solution is used to exfoliate graphene from graphite.
5. Solvothermal synthesis - The exfoliation of graphene from a bulk crystal of graphite is done in an autoclave having high pressure and temperature.
6. Thermal reduction of graphene oxide - The repeated reduction of graphene oxide by heating in a hydrogen gas environment can result in graphene formation.

The discovery of graphene was through the mechanical exfoliation (Novoselov et al., 2004) of graphite. Different exfoliation techniques such as mechanical exfoliation, liquid-phase exfoliation (Nicolosi et al., 2013; Farajian et al., 2019), and electrochemical exfoliation (Chen et al., 2019; Ejigu et al., 2019) are used for the synthesis of graphene. In the case of mechanical exfoliation of graphene, highly ordered pyrolytic Graphite (HOPG) is used. The simplest method to exfoliate is by using a scotch tape, and the graphene layer is transferred to the required substrate by sticking the tape on it. However, large-scale synthesis of graphene through this approach is time-consuming, expensive, and not practical. In practice, the use of CVD is more commonly used to obtain high-quality graphene films (Fujita et al., 2017). In the CVD process, the gaseous reactants combine to produce the graphene layer on the substrate surface. Depending on the substrate temperature, the formation process of the sample can be controlled. With the CVD process, relatively high-quality graphene can be produced. The modern CVD techniques can be classified into LPCVD (low-pressure CVD) and UHVCVD (ultrahigh vacuum CVD) (replace with PECVD, hot wall, and cold wall) (Mueller et al., 2014; Sharma et al., 2020).

In CVD, the deposition of a monolayer graphene on the surface of a metal substrate is relatively easy and has a large area scalability potential. Several other growth techniques have been reported for graphene synthesis toward RRAM applications including atomic layer deposition (ALD) (Zhang et al., 2014a), solution deposition techniques (Zhong et al., 2015), plasma-assisted techniques, reduction of graphene oxide (Kurian, 2021), arc discharge (Li et al., 2011). Solution coating methods such as spin coating (Long et al., 2019), dip coating (Kim et al., 2019), and drop coating (Puah et al., 2020) offer attractive platforms for obtaining high-quality graphene films due to their low-cost and large area processability. Laser scribing technology can be used to convert GO to rGO using laser, and RRAM realized using laser scribed reduced graphene oxide was reported in Li et al. (2016). CO_2 laser-induced graphene (LIG) can be used for the fabrication of RRAM, where the graphene is transferred to polydimethylsiloxane (PDMS) from polyimide (PI) (Jung et al., 2021) and SnO_2 is deposited on it. This will provide a flexible RRAM device. Graphene is the thinnest material discovered to date, and properties such as transparency, and flexibility make this suitable for various electronic device applications.

3.2. Features and working mechanisms of RRAM

RRAM is a non-volatile memory that makes use of a material sandwiched between two metal electrodes that have resistive switching properties. The resistance of the RRAM changes depending on the voltage applied across it.

The popular resistive switching material such as titanium dioxide (TiO_2) resistance can be changed by the application of electrical current to the RRAM. The change in resistance to a high or low resistance is mapped to binary states of "0" and "1", thereby allowing digital storage. By applying voltage pulses to the RRAM electrode resistance of the TiO_2 film can be changed. The change in resistance is dependent on the frequency as well as the amplitude of the pulses applied. The RRAM can be read by applying a small voltage pulse and reading the output currents without disturbing the resistance state.

The MIM layer format is used to create the structure of RRAM as shown in Figure 10. The resistive switching mechanism

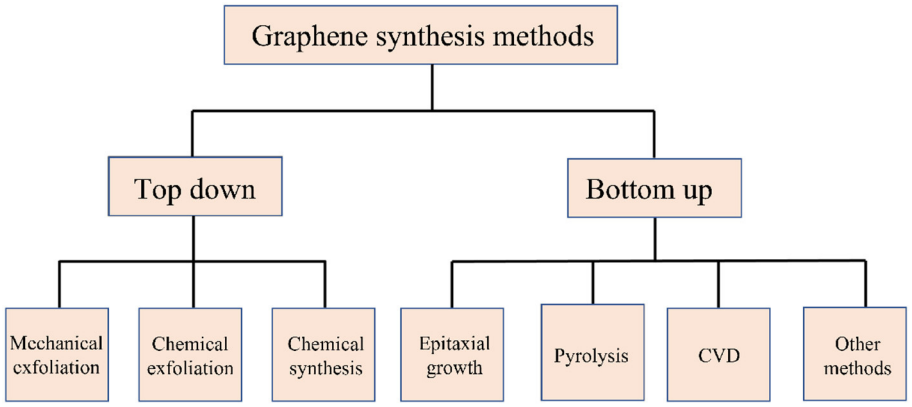

FIGURE 9
Schematic representation of different methods of graphene synthesis.

is enabled with applications of voltage across the two terminals of RRAM to define the resistive state. The HRS is considered the OFF state, and the LRS is regarded as the ON state. The switching mechanism from HRS to LRS happens through the application of external voltage. Some of the materials which exhibit this switching include the oxides of hafnium (Long et al., 2013; Zhao et al., 2014b; Feng et al., 2016), titanium (Yang et al., 2009; Bousoulas et al., 2016), tantalum (Chiu et al., 2012; Prakash et al., 2015; Huang et al., 2016), zinc, nickel (Lee et al., 2008b), manganese (Zhang et al., 2009), magnesium (Chiu et al., 2012), aluminum (Wu et al., 2010), and zirconium (Lin et al., 2007; Wang et al., 2009). In RRAM, the choice of electrode material is critical since it affects the switching property of the system. A small read voltage is applied to understand the system's current state (either ON or OFF) without disturbing the system's state. Since RRAM is a non-volatile memory, it will preserve the state even after removing the external voltage.

RRAM can be classified into two types depending on the voltage polarity to unipolar and bipolar resistive switching. The RRAM is unipolar when the used voltage polarity is the same, and it is called bipolar if reverse voltage polarity is used for switching between the different resistance states (LRS and HRS).

The insulating and conducting mechanisms in the RRAM occur from the breakdown and growth of the filament on the application of an external voltage. Depending on the resistive mechanism, RRAM can be classified into (i) metal ion-based RRAM and (ii) oxygen vacancies filament-based RRAM. In metal ion-based RRAM, the switching mechanism happens by the migration of metal ions in the filament and the oxidation and reduction mechanism. The steps followed in the process of transitioning of conducting state to the insulating state are depicted in Figure 11.

This type of mechanism happens in the case of metal electrodes such as Au, Ni, or Cu at the top-level electrode. The migration of metal ions occurs through the dielectric layer, and the subsequent reduction or oxidation happens at the bottom. This will create a metal filament between the two metal electrodes through the dielectric barrier. This metal filament formation possesses the LRS state, and the disappearance of the same enables the HRS state. In Figure 11, the Ag/a-ZnO/Pt RRAM cells demonstrate the resistive

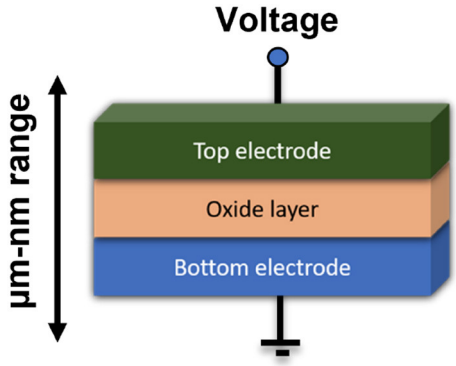

FIGURE 10
Schematic structure of RRAM with metal-insulator-metal layer structure.

switching mechanism. In this case, the Ag electrode is the active element that takes part in the filament formation mechanism, and the Pt electrode is inert. The state of the RRAM devise in the absence of an external electric field is shown in Figure 11A. On applying an external voltage, the oxidation of silver takes place, and it starts to get deposited on the dielectric layer. The bottom electrode, having a negative polarity, will attract these ions, and the ions get deposited on the bottom layer. The formation of metal filament through this process puts the device in the LRS state, as shown in Figures 11B–D. The device can be switched to the HRS state by applying the voltage in the reverse direction, as shown in Figure 11E. We can use graphene as a top/bottom electrode as well as an active insulating layer instead of other materials, as discussed in the following section.

In the case of oxygen vacancies-based RRAM, the resistance-switching mechanism occurs with the creation of oxygen vacancies. The reaction of oxygen ions with the anode material will create the conducting filament. The properties of RRAM will depend on the type of materials present in the top electrode, bottom electrode, and middle layer. Different substitutions of the top and bottom electrodes and middle layers with different materials can enhance

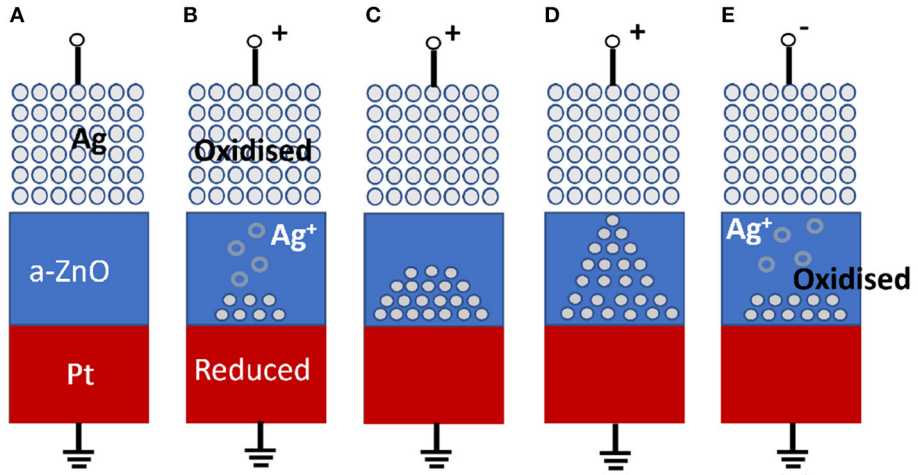

FIGURE 11
Schematic of the switching mechanism of conductive bridge RRAM. **(A)** The pristine state of the RRAM device. **(B, C)** Oxidation of Ag and migration of Ag+ cations toward the cathode and their reduction. **(D)** Accumulating Ag atoms and Pt electrodes leads to the growth of highly conductive filaments. **(E)** Filament dissolution takes place by applying a voltage of opposite polarity (Zahoor et al., 2020).

the properties of RRAM. The use of 2D materials has shown an enhancement in endurance, switching speed, threshold voltage, retention time, etc. The graphene-based RRAM shows promising results in the modification of RRAM toward better performance and for making the system a multilevel cell storage device for the application of MAC computing.

Different parameters will affect the performance of the RRAM device. This study mainly focuses on the variability-averse multi-level cell storage in the graphene-based RRAM system. The RRAM devices have shown a large variability due to the stochastic nature of the switching process.

4. Graphene-based RRAM

Improving the reliability, scalability, and cost-effectiveness of the RRAM device is an essential requirement for practically realizing in-memory and neural computing applications. Graphene-based RRAMs (GRRAM) have different characteristics: low power consumption, higher density, transparency, and homogeneity. GRRAM can be divided into two sub-parts: graphene RRAM and graphene oxide (GO) /reduced graphene oxide (rGO) RRAM. In graphene RRAM, graphene is used as an electrode, whereas in graphene oxide/reduced graphene oxide RRAM, GO or rGO can either be used as a dielectric layer or electrode to enhance the device's performance.

4.1. Graphene as the electrode in RRAM

The main property of RRAM is the resistive switching mechanism which has various difficulties related to the selection of electrodes and the dielectric layer. The high conductivity and high surface area-to-volume ratio of graphene makes it suitable for electrodes. The power consumption is significantly less in graphene-based electrodes in RRAM compared to conventional metal electrodes in RRAM memory devices. Graphene as an electrode offers various advantages over traditional metal electrodes. The greater mechanical scalability, higher conductivity, and ultrathin nature of graphene help to design non-volatile RRAM memory devices. The mechanical properties of graphene, including exceptional strength, flexibility, and elasticity, make it an ideal candidate for use in RRAM devices. These properties enable the fabrication of ultrathin memory cells and provide the potential for integrating RRAM into complex, multi-layered device architectures (Novoselov et al., 2005; Zhang, 2015). The mechanical scalability of graphene allows for the creation of densely packed memory arrays, contributing to higher storage capacities and improved device performance (Papageorgiou et al., 2017). Furthermore, graphene exhibits exceptional electrical conductivity due to its unique electronic band structure (Yung et al., 2013). The switching mechanism in RRAM involves the controlled migration of ions within the memory cell, leading to changes in resistive states. Graphene's high conductivity facilitates efficient charge transport during these switching processes, resulting in fast and reliable switching. The high conductivity of graphene also helps reduce power consumption and enables high-speed read and write operations in RRAM devices.

Lee et al. (2010) report a detailed study on resistive switching characteristics of non-volatile memory devices with nano-materials. 2D material and nanomaterial are the extreme candidates in the nano industry where organic channels and metal electrodes decrease the transmittance value (transmittance decrease of 25%) of the memory devices (Lee et al., 2010). Graphene is used as electrodes, and single-wall carbon nano-tube (SW CNT) is assumed as active layers between metals in non-volatile memory devices. They implemented this memory device with ozone treatment as graphene and oxygen atoms are bonded together. The fabricated memory device revealed that it provides an acceptable transmittance value. Graphene as an electrode provides

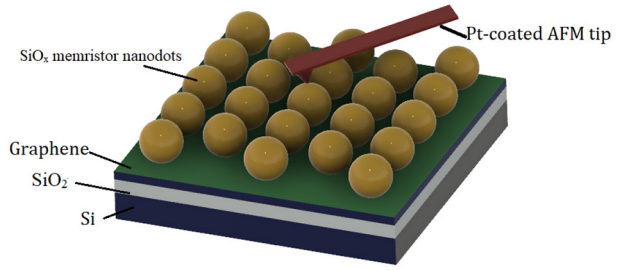

FIGURE 12
Schematic structure of memristor nanostructures on metal and graphene electrodes by a block copolymer self-assembly process.

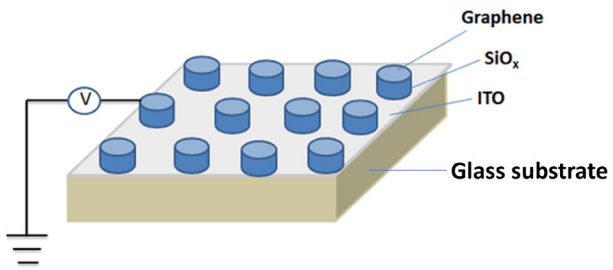

FIGURE 13
Schematic diagram of graphene-SiO_x -indium tin oxide (ITO) device.

a minimum decrease of transmittance of 3.6 %, which is 11.4 % and 25 % in Au and Al. They discovered that the non-volatile memory device with graphene electrodes exhibits better conduction with high mobility of $44 cm^2 V^{-1} s^{-1}$ and a switching speed of 100 ns. The graphene-based memory device performs better than metallic electrodes such as Au, Al, and Ag. The graphene SWCNT memory device improves switching characteristics enhanced by 2×10^2 (Yu et al., 2011b).

Ji et al. (2011) approached a design to integrate an 8×8 crossbar array of organic memory devices with graphene. This multi-layer graphene is an intermediate layer between insulating polyamide (IP) layers. A fabrication process integrates this device with the help of PET (polyethylene terephthalate) substrate. This device offers a high switching ratio current of 10^6 with write-once-read-many (WORM) characteristics. The bending cycle is 10 orders larger (Lee et al., 2010) and exhibits excellent cell-to-cell uniformity. The retention time of the memory device has been controlled in the order of 10^4. Their approach has maintained stable and reliable device characteristics without degrading the current performance. The WORM-type devices store the data permanently without losing any unintended data.

Park et al. (2012) demonstrated a detailed fabrication and characterization of high-density memristor nanodots with platinum and graphene electrodes by a block copolymer self-assembly process. Graphene is used as the bottom electrode, and Pt is a top electrode, where silicon dioxide (SiO_2) is considered an active layer for resistive switches where the memory device has been fabricated with a minimum process cost and less complexity. The fabricated device exhibits a switching ratio of 10^2, an endurance of 80 voltage sweeps, and a unipolar switching mechanism independent of the supply voltage. The formation of a memristor on a graphene electrode is shown in Figure 12.

As transparent electronics devices are in high demand for the electronics industry. Yao et al. (2012) have configured a transparent non-volatile memory device based on SiO_x active layer, indium tin oxide, and graphene as bottom and top electrodes with the glass substrate. Studies on the various device sizes are pursued to enhance the reliability of non-volatile memory. Their study revealed that the conduction filament generated in SiO_2 active layer maintains the constant current as the device size increases or decreases. The switching ratio (10^5) and electrical endurance (300 voltage sweeps) have improved compared to Park et al. (2012). They have also explored how the proposed device with graphene electrode offers better transparency characteristics and low retention time would be beneficial for device application. Figure 13 shows the graphene-SiO_x-indium tin oxide (ITO) device.

A glass platform is a suitable choice for constructing transparent memory devices. The RRAM is constructed with indium tin oxide as the top electrode, alumina as the functional oxide layer, and graphene as the bottom electrode. The non-volatile memory device of this composition has a high transmittance of 82% in the visible region. It is stable and has non-symmetrical bipolar switching properties with low set and reset voltages (less than 1 volt). With its vertical two-terminal configuration, the device has good resistive switching performance and a high on-off ratio (switching ratio) (5×10^3) (Dugu et al., 2018). The figure representing the device structure is shown in Figure 14. Furthermore, transparent materials can be integrated with other optical components to manipulate and direct light within the sensing system. This integration enhances the functionality and performance of optical sensors. Transparent RRAM devices could be integrated with optical sensors, enabling direct interaction between optical input data and neural network processing. This could find applications in fields such as image recognition or computer vision (Zhou et al., 2019; Kalaga et al., 2020).

A graphene-based memristive device (GMD) has been proposed by Qian et al. (2014) and presented a comparative analysis of output performance with a Pt-based memristive device (PtmD). The schematic structure for PtMD and GMDs is shown in Figure 15. The graphene electrode is integrated into TiO_x by the CVD fabrication method to obtain ultra-low switching power and non-linearity. Unlike Yao et al. (2012), they have used graphene as the bottom electrode, whereas Ti/Pt is used as the top electrode. The GMD is fabricated on polyethylene naphthalate (PEN) and offers excellent retention against mechanical bending. They discovered that GMDs have less switching power compared to PtMDs, which helps to protect the device from any thermal damage. Tunable, ultralow-power switching in memristive devices are enabled by a heterogeneous graphene oxide interface. The summary of RRAM devices graphene as top and bottom electrode along with typical characteristics are listed in Table 2.

Similar to Qian et al. (2014), Lee et al. (2015) fabricated a graphene SET electrode-RRAM (GS-RRAM) memory device and

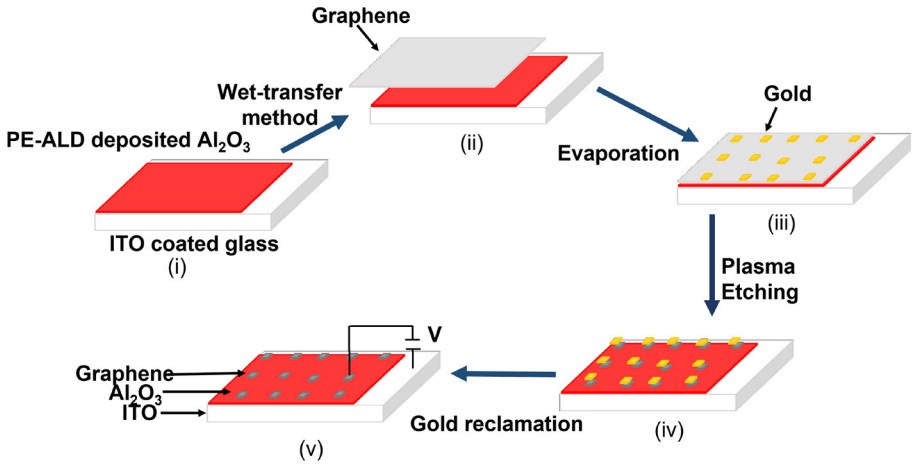

FIGURE 14
Schematic structure of the Ti/ZrO_2/Pt RRAM device (Dugu et al., 2018).

compared it with a Pt-RRAM memory device. In this study, a thin monolayer graphene that serves as a SET electrode is considered to make a thin memory cell structure. The graphene SET electrode helps to store (SET) and restore (RESET) oxygen ions during the programming process. They revealed that the proposed model with a graphene edge electrode has a lower SET compliance current, low RESET current, and low programming voltages, where the Pt-RRAM device cannot deal with low programming voltage or current due to degradation issues of the memory window. The efficient ion-storing capability of graphene helps reduce the power consumption 300 times more in Pt-RRAM. Metal oxide-resistive memory using graphene-edge electrodes (Chakrabarti et al., 2014) explored the performance of RRAM, where graphene is used as top and bottom electrodes. The $TiO_x/Al_2O_3/TiO_2$ dielectric layer is sandwiched between the top and bottom electrodes. The device exhibits forming-free switching characteristics where the device transitions between different resistance states (HRS/LRS) without requiring a separate "forming" process.The forming-free behavior reduces the device complexity and faster the switching process. The proposed device has increases the non-linearity of the current-voltage characteristic with a reduced value of current compliance. When the device exhibits increased non-linearity, the relationship between voltage and current is not linear and more complex and may involve various mechanisms, such as threshold effects, hysteresis, or other non-linear behaviors. This non-linearity can be influenced by factors such as the material properties of the dielectric layer and the electrodes as well as the specific design and operating conditions of the device. A stable retention time of 10^4s, a switching ratio of 10^4, and a greater endurance value ($>$ 200 cycles) have been obtained for the graphene-insulator-graphene (G-I-G) based RRAM configuration. Sohn *et al.* reported a graphene-based 3D RRAM structure where the oxygen ions originating from HfO_x migrate toward the graphene layer, where they aggregate to create a conductive filament (Sohn et al., 2015). This filamentary layer exhibits exceptional thinness, primarily attributed to the atomic-thick nature of graphene. This aligns with the switching mechanism observed in HfO_2 RRAM devices

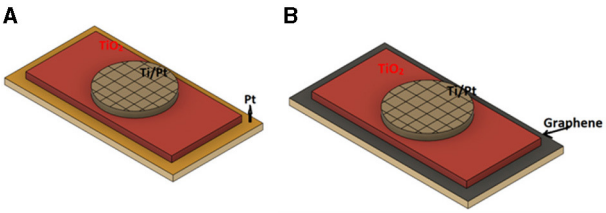

FIGURE 15
Schematic structure for **(A)** platinum-based memristors devices (PtMDs) and **(B)** graphene-based memristors devices (GMDs).

utilizing a top electrode composed of TiN in conjunction with a passive bottom electrode (Yu et al., 2012).

4.2. Graphene as the middle layer in RRAM

Other than electrodes, graphene can also be used as a middle layer in GRRAM for optimizing the switching properties. The incorporation of graphene in the middle layer helps the filament growth by generating a local internal field and acts as a trapping site in the RRAM. The graphene middle layer is usually used for multilevel switching. It is reported that graphene flakes when used as a middle layer help trap charge and act as a storage medium.

Doh and Yi (2010) proposed few-layer graphene (FLG) as an active layer in field-effect devices/ferroelectric devices. They studied the effect of the graphene thickness variation to observe the electrical performance. They discovered that the device has bistable resistance characteristics with long retention time. The resistance difference ratio has decreased with the increased value of graphene film thickness. They also demonstrated that power consumption is high due to the high value of operational voltage ($V_G > 30V$). He et al. (2012) proposed nanographene (NG) which acted as an active layer fabricated on a SiO_2 substrate. Various

TABLE 2 Graphene as the top and bottom electrode.

References	Bottom electrode	Top electrode	Active layer	Substrate	Switching ratio	Endurance	Retention ratio
Yu et al. (2011b)	Graphene	Graphene	SWCNT	PET	10^3	-	10^2
Ji et al. (2011)	Al	Graphene	polyimide and 6-phenyl-C61 butyric acid methyl ester (PI:PCBM)	PET	10^6	-	10^4
Park et al. (2012)	Graphene	Pt	SiO_2	Si	10^2	80	-
Yao et al. (2012)	ITO	Graphene	SiO_x	Glass	10^5	300	-
Dugu et al. (2018)	ITO	Graphene	Alumina	Glass	$> 10^3$	-	-
Chakrabarti et al. (2014)	Graphene	Graphene	TiO-x/Al_2O_3/TiO_2	-	10^4	> 200	10^4
Ji et al. (2011)	Graphene	Graphene	SWCNT	PET	10^3	10^2	10^3
Ji et al. (2011)	Graphene	Graphene	ZnO	Si	10^3	50	-
Chakrabarti et al. (2014)	Graphene	Graphene	TiO-x/Al_2O_3/TiO_2	-	10^4	10^2	10^4
Yao et al. (2012)	Graphene	Graphene	SiO_x	Plastic	10^6	10^2	
Park et al. (2012)	Graphene	SiO_x	Pt	Si	10^2	80	10^4
Ying-Chih Lai et al. (2013)	Graphene	Al	PMMA:P3BT	PET	10^5	10^7	10^4

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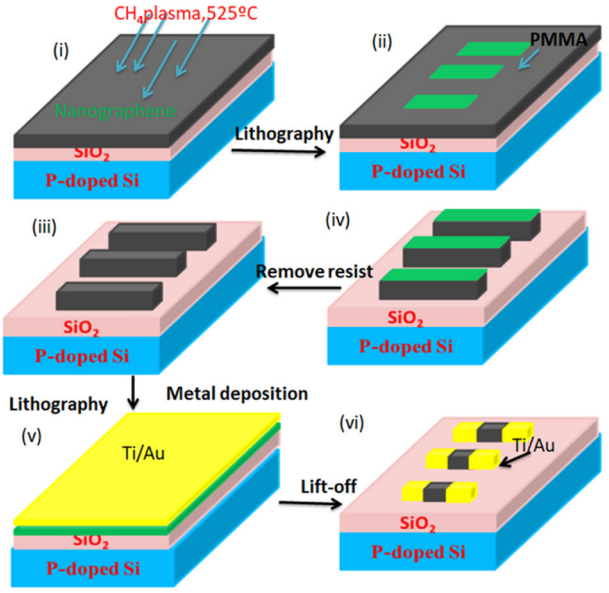

FIGURE 16
Fabrication flowchart for nanographene (NG).

multi-level switching mechanisms have been observed, such as unipolar, bipolar, and non-polar characteristics. Nanographene as an active layer in RRAM has several advantages, such as tunable conductivity and an easy fabrication process, unlike other materials. This research has shown a better endurance value of 10^4 cycles, a faster-switching speed of 500 ns, and a longer retention time of 10^5 cycles. The fabrication flow chart is shown in Figure 16.

Shindome et al. (2013) experimented with single and multi-layer graphene nanoribbon RRAM device characteristics. The drain current performance has been obtained for changing metal electrodes. They revealed that drain current is more for multi-layer graphene RRAM devices than single-layer graphene RRAM. The research also exhibits lower switching energy with a decreased value of channel width, which increases the packing density of the device. Graphene nanoribbon RRAM can possibly scale down to 30nm. Shin et al. (2010) proposed the charging and discharging effect (CDE) to study the bistable switching effects in graphene devices. They also demonstrate bandgap engineering to improve the switching ratio of the device. Two different charge carriers, p-type and n-type, have been considered for this study. The proposed study revealed that the current hysteresis of p-type graphene is inverted into n-type graphene, which increases the stability of the device. The summary of RRAM devices with graphene as an active layer along with typical characteristics are listed in Table 3.

5. Graphene oxide (GO)/reduced graphene oxide (rGO) RRAM

Graphene as a two-dimensional crystal has received more attention from researchers in the semiconductor industry due to its ultrahigh mobility, high thermal conductivity, and transparency characteristics. Graphene oxide is a layered structure consisting of a monolayer of graphene bound to oxygen in carboxyl, hydroxyl, or epoxy groups. Having a high energy band-gap of graphene oxide is possible to reduce the energy band-gap by removing the C-O bonds and offers high solubility. Graphene oxide and reduced graphene oxide are the two important carbon materials mainly used in bioelectrochemical systems (BESs). Graphene oxide offers a large hydrophilic surface area with oxygen-containing functional groups, facilitating microbial attachment and tailored electrochemical reactions on its electrode surface (Singh et al., 2018). On the other hand, rGO, obtained from GO through reduction processes, provides enhanced electrical conductivity, improved biocompatibility, and potential catalytic activity, making it an ideal candidate for efficient electron transfer and biofilm formation in BES systems (Wu et al., 2019). Graphene oxide can be deposited on any substrate due to its flexible nature. Nowadays, GO is a good insulating and semiconductor material compared to other materials and is highly used for RRAM devices. Graphene oxide-based RRAM devices have various pros compared to other materials. The RRAM device with GO can be scaled down in nano-regime and increases the packing density due to the easy fabrication process. Hu *et al.* studied graphene oxide (GO) based RRAM device flexible non-volatile memory. For the purpose of this study, aluminum (Al) has been chosen as the top and bottom electrodes, while GO functions as the active layer. When a negative voltage is applied, it induces an electric field that prompts the migration of oxygen ions within the GO layer. This migration leads to the formation of localized conductive filaments (CFs), consequently causing the device to switch to a LRS. Notably, at the LRS, ohmic conduction is not observed due to the transformation of the GO film into a sp3-bonded state in the absence of CFs (Jeong et al., 2010). During the forming process, a positive voltage bias applied to the Al layer initiates the creation of a highly resistive region in proximity to the tunneling electrode (TE). In the presence of an external electric field, oxygen ions present in the dielectric layer migrate toward the electrode. This migration fosters the continuous development of an sp^3 hybridization layer between the Al electrode and the GO layers that have undergone structural modifications, leading to the high-resistance state (HRS). Subsequently, when a negative voltage bias is applied to the TE Al layer, the reverse diffusion of oxygen ions occurs, resulting in the formation of CFs that lead to the low-resistance state (LRS) near the contact interface, driven by the influence of a negative electric field (Panin et al., 2011). In 2009, He et al. (2009) first explored the RRAM device with graphene oxide (GO) thin films, which are processed by the vacuum filtration method. They found that the device has a low switching voltage and offers a low switching ratio, which is improved later by many researchers (Kim et al., 2011; Yi et al., 2014). Jeong et al. (2010) fabricated a GO-based RRAM device prepared by the spin casting method at room temperature and found to be more reliable and flexible. This study has increased the retention and endurance of the device, which would be helpful for memory applications.

Graphene oxide (GO) can be used for non-volatile and bistable memory devices for its high optical transparency and flexibility. Vasu et al. (2011) studied the unipolar switching effect

TABLE 3 Graphene as an active layer.

Reference	Bottom electrode	Top electrode	Active layer	Substrate	Switch ing ratio	Endurance	Retention time
He et al. (2012)	Ti/Tu	SiO_2	NanoGraphene	p-doped Si	-	10^4	10^5
Shin et al. (2010)	Cr/Au	Al	Graphene	SiO_2	-	10^2	-
Shindome et al. (2013)	Ti/Au	Ti/Au	Graphene	SiO_2	10^3	10^4	10^5
Wu et al. (2012)	ITO	ITO	Graphene	Glass	10^6	-	10^4
He et al. (2013)	Ti/Au	Ti/Au	Graphene	Si/ SiO_2	10^5	-	-
Shindome et al. (2013)	Ti/Cr/Au	Ti/Cr/Au	Graphene nanoribbon	Si/ SiO_2	10^6	10^2	10^3

on reduced graphene oxide (rGO) with the glass substrate to obtain a high switching ratio and switching speed. The obtained results exhibit a switching ratio of 10^5 and switching speed of 10 μs.

Rani et al. (2012) implemented a cost-effective non-volatile memory behavior in rGO memory devices for extracting better endurance and retention time. It is found that the rGO memory device exhibited an endurance value of 10^2 and a retention time of 10^5. Ho et al. (2014) demonstrated a comparative analysis between rGO and GO RRAM devices for impedance spectroscopy and current-voltage analysis. The impedance spectroscopy and current-voltage analysis have been studied to determine the possible physical mechanism for resistive switching behavior. It is observed that switching behavior can be noticed in rGO-based RRAM devices due to its oxidation and reduction at the top electrode. The obtained results for rGO were better with the retention time of 10^6s. However, the rGO memory device provides a large value of the operating voltage of 4V, which increases the power consumption.

Pradhan et al. (2016) proposed a non-volatile rGO-based RRAM memory device to reduce the threshold voltage, which solves the power losses problem of the device more than Ho et al. (2014). Pradhan et al. (2016) proposed an rGO RRAM device which exhibits a threshold value of less than 1V where 4V was achieved by Ho et al. (2014). They also checked the variability of device size, film thickness, and scan votlage.

Kim et al. (2014) demonstrated a transparent memory cell, where reduced graphene is placed between two ITO electrodes to observe the multi-level resistive switching purpose. This memory device offers 80% optical transmittance where the amplitude of applied pulse voltage was varied from 2 to 7V.

Lin et al. (2015) developed a ZnO RRAM device with a capping rGO layer to study the resistive switching behavior. They concluded that introducing the rGO layer increases the stability of the ZnO memory device with a switching ratio of 10^5. The rGO layer acts as an oxygen reservoir in the ZnO memory device where ions are transit easily. On the other hand, oxygen vacancies of the rGO layer oppose reacting with Al electrodes. They also mentioned that ZnO RRAM device offers a great value of endurance of 10^8. The summary of RRAM devices with graphene oxide and reduced graphene oxide as an active layer is listed in Table 4.

6. Comparison of the properties of graphene-based materials with other 2D materials

In sections 4 and 5, the details of graphene, graphene oxide, and reduced graphene oxide base RRAM and its characteristics are discussed. There are other 2D materials such as transition metal dichalcogenides (TMDs) (molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2) etc.), which offer a diverse range of electronic properties as discussed in section 3. TMDS based RRAM is an emerging technology in the field of non-volatile memory and nanoelectronics (Zhu et al., 2019). In TMD-based RRAM, a thin layer of TMD material is used as the switching medium between two electrodes. The resistance of this TMD layer can be altered by applying an electric field, which changes the oxidation state or defects in the TMD material (Zhang et al., 2018; Jian et al., 2022). However, there are also challenges to overcome, such as ensuring stable and reliable switching behavior, understanding the underlying mechanisms that control resistance switching, and developing scalable manufacturing processes (Zhang et al., 2018). Table 5 presents the comparative study of different properties of graphene and TMDs based RRAM. TMDs can form stable heterostructures with graphene, combining the strengths of both materials for various functionalities.

Metal oxides such as hafnium oxide (HfO_2) and titanium dioxide (TiO_2) provide unique electronic properties suitable for different device applications (Meyer et al., 2012). Along with memory, they are used in optoelectronic devices, catalysis, and sensing applications. Metal oxides exhibit resistive switching behavior, which makes them suitable for RRAM applications, where the metal oxide layer acts as the switching medium (Sawa, 2008). When a voltage is applied across the electrodes, localized changes in the metal oxide's resistance state occur due to various mechanisms, such as the formation and dissolution of conductive filaments or changes in oxygen vacancy concentration (Kumar et al., 2017). One advantage of metal oxide-based RRAM is the potential for high memory cell density, HfO_2 based systems provide multilevel cell storage capabilities (Qi

TABLE 4 Graphene oxide and reduced graphene oxide as an active layer.

Reference	Bottom electrode	Top electrode	Active layer	Substrate	Switching ratio	Endurance	Retention time
Wu et al. (2014)	Pt	Cu	GO	$Ti/SiO_2/Si$	20	10^2	10^4
Hong et al. (2010)	ITO	Al	GO	Glass	10^3	10^2	10^9
Jeong et al. (2010)	Al	Al	GO	PET	10^2	10^2	10^5
Wang et al. (2012a)	ITO	Al	GO	Glass		10^3	10^2
Hu et al. (2012a)	Pt	Pt	GO	SiO_2 /Si	10^4	10^2	10^5
Liu et al. (2013)	GO	GO	GO	PET	10^2	10^3	10^3
Wang et al. (2012b)	Pt	Al	GO	Si	10^4	10^2	10^3
Venugopal and Kim (2012)	Ag	Ag	GO	SiO_2	10	-	10^3
Wang et al. (2012a)	ITO	Al	GO	PET	10^2	10^2	10^4
Pradhan et al. (2016)	Al	Al	GO	Glass	10^2	10^2	10^4
Banerjee et al. (2015)	ITO	Au	GO	Glass	10	10^2	-
Wu et al. (2015a)	ITO	ITO	GO	PES	10	-	10^5
Nagareddy et al. (2017)	Ti/Pt	Ti/Pt	GO	Si/ SiO_2	10^3	10^4	10^5
Kim et al. (2018)	Pt	Pt	rGO	Si/SiO_2	10^5	-	-
Saini et al. (2018)	ITO	Al/Au	GO	Glass	10^5	-	–
Han et al. (2014)	Ag	Au	rGO	PET	10^4	10^2	10^5
Kim et al. (2014)	ITO	ITO	rGO	Glass	10^3	10^5	10^7

et al., 2018; Milo et al., 2019). Achieving stable and repeatable resistive switching behavior is crucial for reliable memory operation. Uniformity of switching characteristics across large arrays of memory cells is also important for commercial viability (Guan et al., 2012). Table 6 presents the comparative study of different properties of graphene and metal oxide-based RRAM devices.

7. RRAM for multi-level cell storage

Multilevel cell storage in RRAM helps to increase the storage density of the memory cell without reducing its size of. In the normal method, the cell size needs to be reduced to increase the density, which requires complex patterning techniques. In the case of multilevel cell storage, the number of bits stored per cell can be increased to n (any integer above 2), increasing the density to n times with 2^n number of available states in the cell. Among the different memory devices such as Spin Transfer Torque RAM (STTRAM) and phase change memory. RRAM shows excellent scalability beyond the 10 nm technology node. The resistive switching mechanism in RRAM helps to attain different intermediate levels by varying the programming current. The size of the conducting filament in an RRAM device depends directly on the applied current. Thus, by adjusting the value of the current, different resistance states can be attained in the system.

The multilevel cell storage can be attained via different methods such as (i) varying compliance current, (ii) adjusting reset voltage, and (iii) changing the pulse width of program/erase operation (Prakash and Hwang, 2016). The most common method among these is the controlling of compliance current to obtain multi-level cell storage. The effect of compliance current on the switching mechanism of the $Ti/ZrO_2/Pt$ is studied by Lei et al. (2014), and the device structure is as shown in Figure 17. In the $Ti/ZrO_2/Pt$ device architecture, the multilevel cell storage is achieved by controlling the magnitude of the compliance current. The observed multilevel cell storage is explained using the voltage divider rule in a series circuit model. By varying the compliance current, the number of traps in the device is controlled; hence, the conductance is varied. A low voltage four-level cell storage is attained in Ta_2O_5/TiO_2 system by controlling the R_L and R_S state of the device (Terai et al., 2010). They found that multilevel cell storage can be achieved by varying the reset voltage as well. In this study, Ru et al. is used as the top and bottom electrode, and the combination of Ta_2O_5/TiO_2 is used as the middle layer. This device achieved a 2-bit/cell storage by multi R_H level operation. In another study of the HfO_2-based RRAM system, the multilevel cell storage is achieved by controlling either I_{set} or V_{stop} (Lee et al., 2008a).

In order to obtain the stable states in the multilevel cell storage system, it is important to distinguish the reference states from one another. The factors affecting the stability of resistance states are cycle-to-cycle variability, device-to-device variability,

TABLE 5 Comparative analysis of graphene-based RRAM and 2D TMDC materials-based RRAM devices.

Device name	Reference	Bottom electrode	Top electrode	Active layer material	Substrate	Switching speed	Endurance	Retention time
Graphene oxide based RRAM	Wu et al. (2014)	Pt	Cu	GO	Ti/SiO_2 /Si	20	10^2	10^4
	Liu et al. (2013)	ITO	GO	GO	PET	10^2	10^3	10^3
	Nagareddy et al. (2017)	Ti/Pt	Ti/Pt	GO	Si/SiO_2	10^3	10^4	10^5
	Wang et al. (2012b)	Pt	Al	GO	Si	10^2	10^2	10^3
	Sun et al. (2015)	FTO	Ag	MoS_2	Glass	10^3	-	10^2
2D TMDs based RRAM (MoS_2, WS_2, $MoSe_2$ based)	Zhou et al. (2017)	ITO	Ag	MoS_2	Glass	10^4	10^2	10^3
	Das et al. (2019)	ITO	Al	MoS_2	Glass	10^2	10^4	10^7
	Kumar et al. (2018)	Ni-Mn-In	Cu	MoS_2	Si	10^2	10^2	10^3
	Rehman et al. (2017)	Ag	Ag	Ws_2	PET	10^3	10^2	10^5
	Zhou et al. (2016)	Ag	Ag	MoS_2	SiO_2	10^2	10^2	10^3

TABLE 6 Comparative analysis of graphene-based RRAM and metal-based RRAM devices.

Device name	Reference	Bottom electrode	Top electrode	Active layer material	Switching speed	Endurance	Retention time
Graphene Oxide based RRAM	Wang et al. (2012b)	Pt	Al	GO	10^4	10^2	10^3
	Pradhan et al. (2016)	Al	Al	GO	10^2	10^2	10^3
	Wang et al. (2012a)	ITO	Al	GO	10^2	10^2	10^4
Metal oxide-based RRAM	Park et al. (2012)	Graphene	Pt	SiOx	10^2	80	10^3
	Yao et al. (2012)	ITO	Graphene	SiO_x	10^5	10^2	10^5
	Tsigkourakos et al. (2017)	TiN/Ti	Au	TiO_{2-x}	-	>50 cycles	10^5
	Wu et al. (2018)	Pd	TiN	HfO_x /Ag/NPs	-	-	10^4
	Chen et al. (2017)	Al	Al	HfO_x	10^4	-	-

operation temperature, random telegraph noise, and interstate switching variability. The study of the retention characteristics and endurance of the device will help to understand the reliability of the multiple resistance levels. It is observed that the retention time for the low resistance state highly depends on the operating current of the device (Ninomiya et al., 2013). With the incorporation of graphene, it is expected to obtain multiple states in the RRAM system. The property of this multi-level cell storage will enable the graphene-based systems to act as a synapse for neuromorphic computing and many other applications.

8. Commercially available RRAM models and its fabrication

For several years, researchers have demonstrated the potential of memristive devices in laboratory experiments. As a result, there

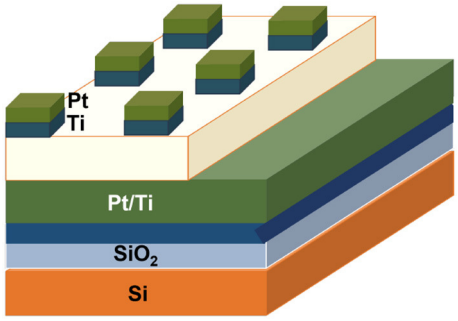

FIGURE 17
Schematic structure of the Ti/ZrO_2/Pt RRAM device (Lei et al., 2014).

have been successful demonstrations of these devices in commercial applications, with RRAM devices being particularly noteworthy in solid-state drives (SSDs) and Internet of Things (IoT) devices. Li et al. (2017) proposed a memory-centric computing approach based on RRAM that leverages on-chip non-volatile memories to perform local information processing in a highly energy-efficient manner. Three in-memory operation schemes using 3D RRAM has been developed and experimented to ensure their effectiveness and reliability, allowing for enhanced local information processing that is highly efficient and optimized for memory-centric computing systems. Wang et al. (2018) demonstrated the integration of 1-transistor/1-resistor (1T1R) memory cells using monolayer MoS_2 transistors and few-layer hBN RRAMs, creating a two-level stacked 3D monolithic structure. The fabrication process was conducted at temperatures below 150 °C. It is observed that this configuration exhibits forming-free (at $< 1V$) gradual set and reset, where the filament formation process in RRAM is not required for achieving the resistance states and which is particularly advantageous for linear weight updating in neuromorphic computing. However, some renowned company has developed various kind of RRAM devices. Adesto Technologies has recently launched a new chip family called Moneta, which utilizes CBRAM (Conductive Bridging Random Access Memory) technology. The Moneta family offers ultra-low power memory solutions that are designed to significantly reduce the overall energy consumption of connected devices. The chips demonstrate read and write operations at 50-100 times lower power compared to competitive solutions. The company has already begun shipping samples of the Moneta family in four different densities, including 32 Kbit, 64 Kbit, 128 Kbit, and 256 Kbit. Fujitsu recently developed RRAM product which offers 1.5 times higher memory density compared to the existing 8 Mbit RRAM. Other renowned foundries such as Intel, Panasonic, and Samsung have been developing RRAM technology. These companies have been investing heavily in RRAM research and development to improve the performance, reliability, and scalability of this promising memory technology.

9. Graphene-based RRAM applications

The researchers are investigating using graphene or graphene oxide (GO) as electrodes or switching material of RRAM targeting in-memory computing for neuromorphic behavior (Izam et al., 2016; Liu et al., 2018; Yan et al., 2018; Abunahla et al., 2020a). The control of resistance for multiple states by memorizing the previous state enables to mimic of biological synapses in the human brain neural network (Sparvoli and Marma, 2018; Xu et al., 2019b; Schranghamer et al., 2020; Kireev et al., 2022). With the large development in memristive materials, an excessive amount of work is being conducted in 2D materials-based memristors for neuromorphic computing (Abunahla et al., 2020a,b; Alimkhanuly et al., 2021). The graphene crossbar variability can be used to build a unique physical unclonable function (PUF), which can be used for various applications. Table 7 presents the review on graphene/GO RRAM for neuromorphic computing.

9.1. Memory

The characteristic features of RRAM such as simple structure, non-volatile, scalability, low power, and fast operation speed makes it a prominent place for future memory devices. In comparison with other materials, the 2D materials-based RRAM devices offer better transparency and flexibility. The incorporation of graphene will provide more feasible and effective methods to increase the capacity of storage devices. The SET current/voltage, I_{set}/ V_{set}, RESET current/voltage, I_{reset}/ V_{reset}, resistance ratio R_{OFF}/ R_{ON}, programming speed, power, and retention time are the parameters for the evaluation of memory devices. Table 8 shows the list of RRAM architecture in the literature with the evaluation parameters.

Zhao et al. (2014a) experimentally demonstrated that the graphene electrode layer provides high built-in series resistance to exhibit good device-to-device uniformity. This exhibits narrow resistance/voltage variations in both ON and OFF states. The switching characteristics of ITO/Al_2O_3/Graphene RRAM is compared with ITO/Al_2O_3/Pt RRAM devices in Dugu et al. (2018). The results in Dugu et al. (2018) show that graphene shows a low SET/RESET current/voltage in comparison with conventional RRAM electrodes such as Pt. A perceptron model is experimentally in Sparvoli and Marma (2018).

Lu et al. (2022) have developed a two-terminal memristor synapse based on a silicon-argon composite film. In the case of the biological synapse, the weight is varied by the release of neurotransmitters from the preneuron induced by spikes. Thus, similar to that, this memristive synapse varies its conductance by the migration of the ions upon an external electrical signal or stimuli.

9.2. Neural networks

The RRAM crossbar in-memory computing is considered to be a potential solution for implementing power-efficient neural network architectures (Li et al., 2018; Mehonic et al., 2020). The analog/digital feature of RRAM, with the ability to memorize, can be used to build artificial neural networks for neuromorphic computation (Mehonic et al., 2020). Figure 18 shows crossbar architecture using RRAM devices for realizing the

TABLE 7 A review on graphene RRAM for neuromorphic computing.

Sl no.	Reference	Graphene application	No. of conductance states	Target application
1	Abunahla et al. (2020a,b)	Au/ partially redued graphene oxide (prGO)/Au	7	ANN of size 5 × 4 and 4 × 4
2	Alimkhanuly et al. (2021)	electrode of 3D vertical RRAM	64	XNOR
3	Sparvoli and Marma (2018)	RRAM fabrication with doped graphene oxide with silver	2	RRAM bridge synapse
4	Schranghamer et al. (2020)	Graphene field effect transistor	16	RRAM synapse
5	Xu et al. (2019b)	Al_2O_3/graphene quantum dots/Al_2O_3	2	Synapse
6	Kireev et al. (2022)	Bilayer Graphene-based Artificial Synaptic Transistors (BLAST)	100	Synapse transistor

TABLE 8 Different RRAM architectures.

RRAM structure	I_{set}/ V_{set}	I_{reset}/ V_{reset}	R_{OFF}/R_{ON} Ratio	SET/R ESET speed	Power
MLG/Dy_2O_3/ITO (Zhao et al., 2014a) Unipolar	1 μA/0.4V	20 μA /0.2V	$> 10^5$	60 ns	4.4 μW
ITO/Al_2O_3/ Graphene (Dugu et al., 2018) Bipolar	2.1 μA/0.8V	1.55 mA/-0.65V	$\sim 3.5 \times 10^3$	NA	$\sim 1mW$
Al_2O_3/GQD/Al_2O_3 (Xu et al., 2019b)	$< 5nA$/1.2V	$< 5nA$/-1.2V	NA	NA	NA
ITO/GO+0.1 % Ag/Al (Sparvoli and Marma, 2018) Unipolar	$< 4.78mA$/0.8V	2 pA/0.25V	7.5×10^8	$10\mu s$	NA
G/SiO_x/ITO (Yao et al., 2012) Unipolar	2 μA/4.26V	2 mA/10V	10^4	$50ns$	20 mW
Au/prGO/Au (Abunahla et al., 2020a,b) Unipolar	25 mA/3V	10 mA/-6.5V	10	10s	NA
TiN/HfO_x/ Graphene (Alimkhanuly et al., 2021) bipolar	$< 1\mu$ A/1.27V	$< 10\mu$A/ -1.37V	$> 10X$	500 ns	NA

MLG, multi-layer graphene; ITO, indium tinoOxide; GQD, graphene quantum dots; NA, not available.

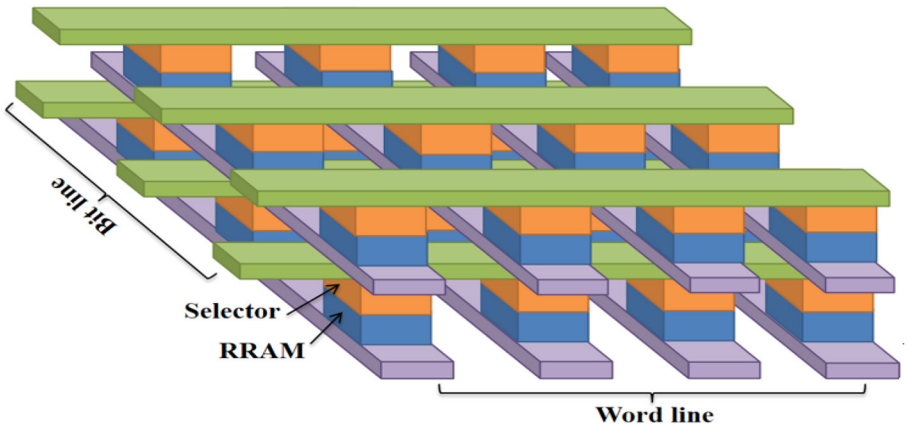

FIGURE 18
3D RRAM crossbar array.

neuromorphic computations. The weights of neural computations are programmed onto the RRAM devices during the write mode. Only a few studies have been reported in the literature using graphene/GO-based RRAM for neuromorphic computing (Abunahla et al., 2020a,b; Alimkhanuly et al., 2021). Both 2D and 3D crossbar architecture with RRAM have been discussed in the literature for neuromorphic computing. HebaAbunahla et al. presented a novel planar analog memristor crossbar with partially reduced graphene oxide (prGO) thin film (Abunahla et al., 2020a,b). In Abunahla et al. (2020a,b), the crossbar array has been fabricated and tested using the Iris dataset with an accuracy of 96.67%. 5 × 4 and 4 × 4 crossbar arrays have been fabricated, which is then used to classify the iris flower based on its petal and sepal length and width into different classes.

Alimkhanuly et al. (2021) demonstrated a 3D vertical RRAM (VRRAM) by replacing the metal-based interconnects with graphene due to the remarkable electronic and thermal conductivities. In Alimkhanuly et al. (2021), the authors fabricated a 416 × 224 × 8 size 3D array system. The recognition performance of the fabricated 3D graphene RRAM (Gr-RRAM) has been tested for the MNIST dataset. The network size is 400 input, 200 hidden, and 10 output neurons. The performance accuracy of Gr-RRAM is compared with platinum RRAM (Pt-RRAM), and the results show that the overall accuracy levels degrade for Pt-RRAM due to high read inaccuracy.

9.3. Logic gates

The logic computing is yet another application of memristor crossbar structure. The XOR operation-focused 3D VRRAM array architecture is demonstrated in Alimkhanuly et al. (2021). The XOR architecture using graphene-based VRRAM arrays have the potential of a highly stackable nature for parallel processing of multiple layers (Alimkhanuly et al., 2021). An XNOR logic-inspired architecture is designed to integrate 1-bit ternary precision synaptic weights into graphene-based VRRAM is presented in Alimkhanuly et al. (2021). However, robustness to device variability by using graphene-based RRAM in logic computing is not yet investigated in the literature and still remains an open problem.

9.4. Cryptography

The memristor crossbar arrays is also applied for cryptography applications (Cai et al., 2022; Yu et al., 2023). An in-memory hyperdimensional encryption using a memristor crossbar array is presented in Cai et al. (2022). The robustness of binary hypervectors against memristor crossbar non-ideality helps to control the impact of noise generated by the memristor crossbar for encryption. A 4D memristive hopfield neural network (MHNN) is proposed in Yu et al. (2023) for image encryption applications. The majority of memory-based cryptographic techniques for hardware security are based on physical unclonable functions (PUFs) (James, 2019). A large number of memory-crossbar-based PUFs have been proposed in the literature, for example, metal-oxide memristor-based or RRAM (Rose and Meade, 2015; Yansong et al., 2015; Uddin et al., 2017; Khan et al., 2021; Kim et al., 2021) etc. The PUF methods use variations in device parameters such as resistance state, switching time, and threshold voltages. These unpredictable probabilistic characteristics of memristor crossbars form the basis for PUF applications. The variations in device parameters and process variations affect the current flow through the device. Any temporal or spatial variations affect all aspects of resistive switching. The variation in PUF characteristics with the properties of graphene has not been explored yet in the literature.

The stochasticity in graphene-RRAM device response has not been extensively studied in the existing literature. The repeatability of fabricated Gr-RRAM devices are experimentally evaluated in the literature. The SET voltage varies for cycle-cycle variations for Gr-RRAM was found to be 6.4% in Alimkhanuly et al. (2021). As discussed in Kim et al. (2021), the SET voltage variations in Gr-RRAM crossbar array can also be used for PUF generation in cryptographic applications. The other device variations such as resistance state, switching time, and threshold voltages have not been considered for analysis with device-to-device and cycle-to-cycle variations. The stochasticity in graphene-RRAM variation for cryptography or PUF characteristics has not been explored yet in the literature and is an open problem.

10. CMOS compatibility

CMOS technology faces various unwanted problems due to the scaling of device attributes. The semiconductor industry is planning to replace the silicon material with graphene material. Since graphene is a conducting material and no energy band gap is present in it, it is very difficult to use graphene for digital device applications due to high-off state leakage and non-saturating drive currents. However, graphene-based devices are more acceptable for low-noise amplifiers and radio-frequency (RF) in analog device applications (Banerjee et al., 2010). Rodriguez et al. (2012) compared the RF behavior between graphene-based field effect transistor (GFET) and Si-based metal oxide field effect transistor (MOSFET). It is observed that the GFET device is more acceptable for the narrow range of drain voltage and drain current compared to Si-MOSFET. Cisneros-Fernández et al. (2019) proposed frequency domain multiplexing of liquid-gate GFET sensor for micro electrocorticogram (ECoG) recording purpose. The proposed work also allows hybrid integration.

Nowadays, graphene with Si CMOS circuits can also be constructed together for making heterogeneous devices. The demonstration of graphene and Si CMOS hybrid circuits has reduced barriers to entry of graphene in electronics. Huang et al. (2014) constructed a low-temperature hybrid integrated circuit where graphene devices and Si-CMOS circuits integrated together. Gilardi et al. (2019) designed relaxation oscillators using a GFET, Si CMOS D latch, and timing RC circuit. It is observed that the introduction of graphene material in the Si-CMOS logic circuit has improved the circuit complexity and also added other device functionality. One of the truly unique electronic properties of graphene not exhibited by conventional

semiconductors is ambipolarity. The ambipolarity of graphene helps to simplify the circuit and provide additional functionality. Graphene's ambipolarity eliminates the need for separate electron and hole transistors, reducing the overall transistor count and circuit complexity (Jabeur et al., 2010). The integration of graphene into Si CMOS logic circuits could offer a feasible approach for both simplification and enhanced functionality. Zhang et al. (2014b) proposed CMOS-compatible all-metal-nitride RRAM based on aluminum nitride (AlN). It is observed that the proposed device provides a lower operation current of 100 A, retention time $3x10^5$, and endurance value of 10^5 Hz. AlN has high thermal stability, allowing it to withstand the elevated temperatures used in CMOS processes. This makes it possible to integrate AlN-based RRAM fabrication steps into standard CMOS processes without causing significant damage to the underlying circuitry (Jackson et al., 2013). AlN can be deposited using various techniques that are already employed in CMOS manufacturing, such as PVD and CVD (Perez-Campos et al., 2015). PVD and CVD methods allow for conformal deposition of thin AlN films over complex three-dimensional structures, including the intricate features found in modern CMOS circuits (Cansizoglu et al., 2015). This conformal deposition capability is crucial for integrating RRAM cells within the existing CMOS architecture. The temperature requirements and chemical interactions during AlN deposition are generally more manageable compared to some graphene synthesis methods. Graphene-based RRAM, on the other hand, could face more integration challenges due to the specialized processes required for graphene synthesis and transfer. Graphene synthesis and transfer techniques involve high-temperature processes and chemical treatments that could affect the performance of the graphene itself (Choi et al., 2022). Achieving high-quality, defect-free graphene layers on a large scale while maintaining CMOS compatibility remains a significant hurdle (Moon and Gaskill, 2011). Yeh and Wong (2015) proposed a cost-competitive One-Transistor-N-RRAM (1TNR) array architecture for advanced CMOS technology where one committed transistor controls the access of one RRAM. It is observed that the 1TNR array architecture provides less leakage current than the cross-point array. Therefore, there is the possibility that graphene-based RRAM memory devices can be considered in CMOS technology soon.

11. Challenges and future scope

Due to its unique and interesting features, graphene has surpassed all other nanomaterials in terms of its use in electronic devices. Additionally, it was shown that graphene's greater mobility, less light absorption, and excellent mechanical qualities enhance the functionality of transparent flexible electronic devices. The difficulty is that the cost of manufacturing graphene will increase the overall price of the device. The transfer of graphene from one substrate to another without causing any damage is a tedious process, which requires the need of sophisticated instruments. Efficient methods need to be implemented to overcome these drawbacks.

The past several years have seen a substantial increase in research into new memory technologies, and numerous prototype RRAM products have been created to show the potential for high-speed and low-power applications. The CMOS compatibility and ability to fabricate in smaller dimensions make the RRAM a suitable candidate for device applications. A high endurance is reported in graphene-based RRAM devices. To date, in a single RRAM device, no technology has reported fast switching, low power, and stable operation simultaneously. In a graphene-based RRAM device, the properties need to be enhanced for better performance of the device.

12. Conclusion

This review article offers an insightful look into the topic of developing graphene-based RRAM devices in terms of neural computing by giving a concise overview of the development of memory architecture, the current trends, and the constraints. The importance of graphene based RRAM, as well as its structure, operation, and classification, have all been highlighted in a thorough discussion. The methodology and a detailed investigation on the MLC capabilities of RRAM have been presented. It is proposed that the graphene-based RRAM can be used for multilevel cell storage. This modified memory device, with 2D material can be used as a synapse. Along with this, the implementation of graphene based RRAM for various important applications such as hardware security and neuromorphic computing have been highlighted.

Author contributions

RTR, RD, and CR: Conducted literature review, prepared a part of the draft copy of the manuscript, and revision of the manuscript. AJ: Contributed to the theoretical framework development, provided critical insights during data analysis and interpretation, manuscript correction and writing, funding acquisition and supervision.

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

References

Abunahla, H., Halawani, Y., Alazzam, A., and Mohammad, B. (2020a). Neuromem: Analog graphene-based resistive memory for artificial neural networks. *Sci. Rep*. 10, 1–11. doi: 10.1038/s41598-020-66413-y

Abunahla, H., Halawani, Y., Mohammad, B., and Alazzam, A. (2020b). "Tunable non-volatile analog resistive memory and its application in AI," in *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 464–467.

Adam, K., Smagulova, K., and James, A. P. (2018). "Memristive lstm network hardware architecture for time-series predictive modeling problems," in *2018 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 459–462.

Alimkhanuly, B., Sohn, J., Chang, I. J., and Lee, S. (2021). Graphene-based 3d xnor-vrram with ternary precision for neuromorphic computing. *NPJ 2D Mater. Applicat*. 5, 55. doi: 10.1038/s41699-021-00236-x

Ambriz-Vargas, F., Kolhatkar, G., Broyer, M., Hadj-Youssef, A., Nouar, R., Sarkissian, A., et al. (2017). A complementary metal oxide semiconductor process-compatible ferroelectric tunnel junction. *ACS Appl. Mater. Interfaces*. 9, 13262–13268. doi: 10.1021/acsami.6b16173

Banerjee, I., Harris, P., Salimian, A., and Ray, A. K. (2015). Graphene oxide thin films for resistive memory switches. *IET Circuits Devices Syst*. 9, 428–433. doi: 10.1049/iet-cds.2015.0170

Banerjee, S. K., Register, L. F., Tutuc, E., Basu, D., Kim, S., Reddy, D., et al. (2010). Graphene for cmos and beyond cmos applications. *Proc. IEEE* 98, 2032–2046. doi: 10.1109/JPROC.2010.2064151

Bill, J., and Legenstein, R. (2014). A compound memristive synapse model for statistical learning through STDP in spiking neural networks. *Front. Neurosci*. 8, 120754. doi: 10.3389/fnins.2014.00412

Bousoulas, P., Stathopoulos, S., Tsialoukis, D., and Tsoukalas, D. (2016). Low-power and highly uniform 3-b multilevel switching in forming free TiO2-x-based RRAM with embedded Pt nanocrystals. *IEEE Electron Device Lett*. 37, 874–877. doi: 10.1109/LED.2016.2575065

Boybat, I., Le Gallo, M., Nandakumar, S. R., Moraitis, T., Parnell, T., Tuma, T., et al. (2018). Neuromorphic computing with multi-memristive synapses. *Nat. Commun*. 9, 1–12. doi: 10.1038/s41467-018-04933-y

Brivio, S., Ly, D. R., Vianello, E., and Spiga, S. (2021). Non-linear memristive synaptic dynamics for efficient unsupervised learning in spiking neural networks. *Front. Neurosci*. 15, 580909. doi: 10.3389/fnins.2021.580909

Cai, J., Amirsoleimani, A., and Genov, R. (2022). "Hyperlock: In-memory hyperdimensional encryption in memristor crossbar array," in *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, 960–964.

Cansizoglu, H., Yurukcu, M., Cansizoglu, M. F., and Karabacak, T. (2015). Investigation of physical vapor deposition techniques of conformal shell coating for core/shell structures by Monte Carlo simulations. *Thin Solid Films* 583, 122–128. doi: 10.1016/j.tsf.2015.03.071

Cao, G., Meng, P., Chen, J., Liu, H., Bian, R., Zhu, C., et al. (2021). 2D material based synaptic devices for neuromorphic computing. *Adv. Funct. Mater*. 31, 2005443. doi: 10.1002/adfm.202005443

Chakrabarti, B., Roy, T., and Vogel, E. M. (2014). Nonlinear switching with ultralow reset power in graphene-insulator graphene forming-free resistive memories. *IEEE Electron Device Letters* 35, 750–752. doi: 10.1109/LED.2014.2321328

Chen, D., Wang, F., Li, Y., Wang, W.-W., Huang, T.-X., Li, J.-F., et al. (2019). Programmed electrochemical exfoliation of graphite to high quality graphene. *Chem. Commun*. 55, 3379–3382. doi: 10.1039/C9CC00393B

Chen, Y.-C., Chang, Y.-F., Wu, X., Zhou, F., Guo, M., Lin, C.-Y., et al. (2017). Dynamic conductance characteristics in hfo x-based resistive random access memory. *RSC Adv*. 7, 12984–12989. doi: 10.1039/C7RA00567A

Chithra, R., Aswani, A. R., and James, A. (2022). "Memristive cnn for wafer defect detection," in *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, 3284–3288. Austin, TX: IEEE.

Chiu, F. C., Li, P. W., and Chang, W. Y. (2012). Reliability characteristics and conduction mechanisms in resistive switching memory devices using ZnO thin films. *Nanoscale Res. Lett*. 7:1–9. doi: 10.1186/1556-276X-7-178

Choi, S. H., Yun, S. J., Won, Y. S., Oh, C. S., Kim, S. M., Kim, K. K., et al. (2022). Large-scale synthesis of graphene and other 2D materials towards industrialization. *Nat. Commun*. 13, 1–5. doi: 10.1038/s41467-022-29182-y

Chua, L., and Yang, L. (1988a). Cellular neural networks: applications. *IEEE Trans. Circuits Syst*.35, 1273–1290. doi: 10.1109/31.7601

Chua, L., and Yang, L. (1988b). Cellular neural networks: theory. *IEEE Trans. Circuits Syst*. 35, 1257–1272. doi: 10.1109/31.7600

Cisneros-Fernández, J., Dei, M., Terés, L., and Serra-Graells, F. (2019). "Switch-less frequency-domain multiplexing of GFET sensors and low-power CMOS frontend for 1024-channel μECoG," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)* (Sapporo: IEEE), 1–5.

Das, U., Bhattacharjee, S., Sarkar, P. K., and Roy, A. (2019). A multi-level bipolar memristive device based on visible light sensing mos2 thin film. *Mater. Res. Express* 6, 075037. doi: 10.1088/2053-1591/ab154d

Doh, Y.-J., and Yi, G.-C. (2010). Nonvolatile memory devices based on few-layer graphene films. *Nanotechnology* 21, 105204. doi: 10.1088/0957-4484/21/10/105204

Duan, S., Hu, X., Dong, Z., Wang, L., and Mazumder, P. (2015). Memristor-based cellular nonlinear/neural network: design, analysis, and applications. *IEEE Trans. Neural Netw. Learn. Syst*. 26, 1202–1213. doi: 10.1109/TNNLS.2014.2334701

Dugu, S., Pavunny, S. P., Limbu, T. B., Weiner, B. R., Morell, G., and Katiyar, R. S. (2018). A graphene integrated highly transparent resistive switching memory device. *APL Mater*. 6, 058503. doi: 10.1063/1.5021099

Ejigu, A., Le Fevre, L. W., Fujisawa, K., Terrones, M., Forsyth, A. J., and Dryfe, R. A. W. (2019). Electrochemically exfoliated graphene electrode for high-performance rechargeable chloroaluminate and dual-ion batteries. *ACS Appl. Mater. Interf*. 11, 23261–23270. doi: 10.1021/acsami.9b06528

Farajian, A. A., Mortezaee, R., Osborn, T. H., Pupysheva, O. V., Wang, M., Zhamu, A., et al. (2019). Multiscale molecular thermodynamics of graphene-oxide liquid-phase exfoliation. *Phys. Chem. Chem. Phys*. 21, 1761–1772. doi: 10.1039/C8CP07115B

Feng, W., Shima, H., Ohmori, K., and Akinaga, H. (2016). Investigation of switching mechanism in HfOx-ReRAM under low power and conventional operation modes. *Scientific Rep*. 6, 1–8. doi: 10.1038/srep39510

Fujita, J. I., Hiyama, T., Hirukawa, A., Kondo, T., Nakamura, J., Ito, S. I., et al. (2017). Near room temperature chemical vapor deposition of graphene with diluted methane and molten gallium catalyst. *Scient. Rep*. 7, 1–10. doi: 10.1038/s41598-017-12380-w

Galashev, A. E., and Rakhmanova, O. R. (2014). Mechanical and thermal stability of graphene and graphene-based materials. *Physics-Uspekhi* 57, 970–989. doi: 10.3367/UFNe.0184.201410c.1045

Gilardi, C., Pedrinazzi, P., Patel, K. A., Anzi, L., Luo, B., Booth, T. J., et al. (2019). Graphene-si cmos oscillators. *Nanoscale* 11, 3619–3625. doi: 10.1039/C8NR07862A

Guan, X., Yu, S., and Wong, H. S. (2012). On the switching parameter variation of metal-oxide RRAM - Part I: Physical modeling and simulation methodology. *IEEE Trans. Electron Devices* 59, 1172–1182. doi: 10.1109/TED.2012.2184545

Han, S. T., Zhou, Y., Yang, Q. D., Zhou, L., Huang, L. B., Yan, Y., et al. (2014). Energy-band engineering for tunable memory characteristics through controlled doping of reduced graphene oxide. *ACS Nano* 8, 1923–1931. doi: 10.1021/nn406505t

He, C., Li, J., Wu, X., Chen, P., Zhao, J., Yin, K., et al. (2013). Tunable electroluminescence in planar graphene/SiO2 memristors. *Adv. Mater*. 25, 5593–5598. doi: 10.1002/adma.201302447

He, C., Shi, Z., Zhang, L., Yang, W., Yang, R., Shi, D., et al. (2012). Multilevel resistive switching in planar graphene/sio2 nanogap structures. *ACS Nano* 6, 4214–4221. doi: 10.1021/nn300735s

He, C., Zhuge, F., Zhou, X., Li, M., Zhou, G., Liu, Y., et al. (2009). Nonvolatile resistive switching in graphene oxide thin films. *Appl. Phys. Lett*. 95, 232101. doi: 10.1063/1.3271177

Ho, N. T., Senthilkumar, V., and Kim, Y. S. (2014). Impedance spectroscopy analysis of the switching mechanism of reduced graphene oxide resistive switching memory. *Solid State Electron*. 94, 61–65. doi: 10.1016/j.sse.2014.02.002

Hong, S. K., Kim, J. E., Kim, S. O., and Cho, B. J. (2010). "Non-volatile memory using graphene oxide for flexible electronics," in *2010 10th IEEE Conference on Nanotechnology, NANO 2010*, 604–606.

Hu, B., Quhe, R., Chen, C., Zhuge, F., Zhu, X., Peng, S., et al. (2012a). Electrically controlled electron transfer and resistance switching in reduced graphene oxide noncovalently functionalized with thionine. *J. Mater. Chem*. 22, 16422–16430. doi: 10.1039/c2jm32121a

Hu, X., Chen, G., and Duan, S. (2016). A novel memristive cellular neural network with time-variant templates. *Perspect. Sci*. 7, 126–132. doi: 10.1016/j.pisc.2015.11.021

Hu, X., Duan, S., Wang, L., and Liao, X. (2012b). Memristive crossbar array with applications in image processing. *Sci. China Informat. Sci*. 55, 461–472. doi: 10.1007/s11432-011-4410-9

Huang, H.-M., Wang, Z., Wang, T., Xiao, Y., and Guo, X. (2020). Artificial neural networks based on memristive devices: from device to system. *Adv. Intell. Syst*. 2, 2000149. doi: 10.1002/aisy.202000149

Huang, L., Xu, H., Zhang, Z., Chen, C., Jiang, J., Ma, X., et al. (2014). Graphene/si cmos hybrid hall integrated circuits. *Sci. Rep*. 4, 1–6. doi: 10.1038/srep05548

Huang, Y., Gu, Y., Wu, X., Ge, R., Chang, Y.-F., Wang, X., et al. (2021). Rese2-based rram and circuit-level model for neuromorphic computing. *Front. Nanotechnol*. 3, 782836. doi: 10.3389/fnano.2021.782836

Huang, Y., Shen, Z., Wu, Y., Wang, X., Zhang, S., Shi, X., et al. (2016). Amorphous ZnO based resistive random access memory. *RSC Adv*. 6, 17867–17872. doi: 10.1039/C5RA22728C

Im, I. H., Kim, S. J., and Jang, H. W. (2020). Memristive devices for new computing paradigms. *Adv. Intell. Syst*. 2, 2000105. doi: 10.1002/aisy.202000105

Izam, N. I. B., Aziz, T. N. T. A., Rahman, R. A., Malek, M. F., Herman, S. H., and Zulkifli, Z. (2016). *2016 IEEE Student Conference on Research and Development (SCOReD)*. Kuala Lumpur. 1–6.

Jabeur, K., Navarro, D., O'Connor, I., Gaillardon, P. E., Ben Jamaa, M. H., and Clermidy, F. (2010). *Proceedings of the 2010 IEEE/ACM International Symposium on Nanoscale Architectures*. Anaheim, CA. 47–52.

Jackson, N., Keeney, L., and Mathewson, A. (2013). Flexible-CMOS and biocompatible piezoelectric AlN material for MEMS applications. *Smart Mater. Struct*. 22, 115033. doi: 10.1088/0964-1726/22/11/115033

James, A. P. (2019). An overview of memristive cryptography. *Eur. Phys. J. Spec. Top*. 228, 2301–2312. doi: 10.1140/epjst/e2019-900044-x

Jeong, H. Y., Kim, J. Y., Kim, J. W., Hwang, J. O., Kim, J. E., Lee, J. Y., et al. (2010). Graphene oxide thin films for flexible nonvolatile memory applications. *Nano Lett*. 10, 4381–4386. doi: 10.1021/nl101902k

Ji, Y., Lee, S., Cho, B., Song, S., and Lee, T. (2011). Flexible organic memory devices with multilayer graphene electrodes. *ACS Nano* 5, 5995–6000. doi: 10.1021/nn201770s

Jian, J., Dong, P., Jian, Z., Zhao, T., Miao, C., Chang, H., et al. (2022). Ultralow-power rram with a high switching ratio based on the large van der waals interstice radius of TMDs. *ACS Nano* 16, 20445–20456. doi: 10.1021/acsnano.2c06728

Jung, J., Shin, D., Lee, Y., and Pak, J. J. (2021). Fabrication of solution-processed SnO2–Based flexible ReRAM using laser-induced graphene transferred onto PDMS. *Curr. Appl. Phys*. 25, 70–74. doi: 10.1016/j.cap.2021.02.009

Kalaga, P. S., Kumar, D., Ang, D. S., and Tsakadze, Z. (2020). Highly transparent ITO/HfO2/ITO device for visible-light sensing. *IEEE Access* 8, 91648–91652. doi: 10.1109/ACCESS.2020.2994383

Khan, M. I., Ali, S., Ikram, A. A., and Bermak, A. (2021). Optimization of memristive crossbar array for physical unclonable function applications. *IEEE Access* 9, 84480–84489. doi: 10.1109/ACCESS.2021.3087810

Kim, D., Kim, T.-H., Choi, Y., Lee, G. H., Lee, J., Sun, W., et al. (2021). Selected bit-line current puf: implementation of hardware security primitive based on a memristor crossbar array. *IEEE Access* 9, 120901–120910. doi: 10.1109/ACCESS.2021.3108534

Kim, H., Lee, S., and Kim, H. (2019). Electrical heating performance of electro-conductive para-aramid knit manufactured by dip-coating in a graphene/waterborne polyurethane composite. *Sci. Rep*. 9, 1511. doi: 10.1038/s41598-018-37455-0

Kim, H.-D., Yun, M. J., Lee, J. H., Kim, K. H., and Kim, T. G. (2014). Transparent multi-level resistive switching phenomena observed in ito/rgo/ito memory cells by the sol-gel dip-coating method. *Sci. Rep*. 4, 1–6. doi: 10.1038/srep04614

Kim, I., Siddik, M., Shin, J., Biju, K. P., Jung, S., and Hwang, H. (2011). Low temperature solution-processed graphene oxide/pr0. 7ca0. 3mno3 based resistive-memory device. *Appl. Phys. Lett*. 99, 042101. doi: 10.1063/1.3617426

Kim, K. H., Gaba, S., Wheeler, D., Cruz-Albrecht, J. M., Hussain, T., Srinivasa, N., et al. (2012). A functional hybrid memristor crossbar-array/CMOS system for data storage and neuromorphic applications. *Nano Lett*. 12, 389–395. doi: 10.1021/nl203687n

Kim, S., Jung, H. J., Kim, J. C., Lee, K. S., Park, S. S., Dravid, V. P., et al. (2018). *In situ* observation of resistive switching in an asymmetric graphene oxide bilayer structure. *ACS Nano* 12, 7335–7342. doi: 10.1021/acsnano.8b03806

Kireev, D., Liu, S., Jin, H., Patrick Xiao, T., Bennett, C. H., Akinwande, D., et al. (2022). Metaplastic and energy-efficient biocompatible graphene artificial synaptic transistors for enhanced accuracy neuromorphic computing. *Nat. Commun*. 13, 1–11. doi: 10.1038/s41467-022-32078-6

Ko, T. J., Li, H., Mofid, S. A., Yoo, C., Okogbue, E., Han, S. S., et al. (2020). Two-dimensional near-atom-thickness materials for emerging neuromorphic devices and applications. *iScience* 23, 101676. doi: 10.1016/j.isci.2020.101676

Krestinskaya, O., James, A. P., and Chua, L. O. (2020). Neuromemristive circuits for edge computing: a review. *IEEE Trans. Neural Netw. Learn. Syst*. 31, 4–23. doi: 10.1109/TNNLS.2019.2899262

Krishnaprasad, A., Choudhary, N., Das, S., Dev, D., Kalita, H., Chung, H. S., et al. (2019). Electronic synapses with near-linear weight update using MoS2/graphene memristors. *Appl. Phys. Lett*. 115, 10. doi: 10.1063/1.5108899

Kumar, A., Pawar, S., Sharma, S., and Kaur, D. (2018). Bipolar resistive switching behavior in mos2 nanosheets fabricated on ferromagnetic shape memory alloy. *Appl. Phys. Lett*. 112, 26. doi: 10.1063/1.5037139

Kumar, D., Aluguri, R., Chand, U., and Tseng, T. Y. (2017). Metal oxide resistive switching memory: Materials, properties and switching mechanisms. *Ceramics Int*. 43, S547–S556. doi: 10.1016/j.ceramint.2017.05.289

Kumar, M., Ban, D. K., Kim, S. M., Kim, J., and Wong, C. P. (2019). Vertically aligned WS2 layers for high-performing memristors and artificial synapses. *Adv. Electr. Mater*. 5, 1900467. doi: 10.1002/aelm.201900467

Kurian, M. (2021). Recent progress in the chemical reduction of graphene oxide by green reductants–a mini review. *Carbon Trends* 5, 100120. doi: 10.1016/j.cartre.2021.100120

Lee, H. Y., Chen, P. S., Wu, T. Y., Chen, Y. S., Wang, C. C., Tzeng, P. J., et al. (2008a). *Low Power and High Speed Bipolar Switching With a Thin Reactive ti Buffer Layer in Robust HfO2 Based RRAM*. Washington, DC: Technical Digest - International Electron Devices Meeting, IEDM.

Lee, S., Sohn, J., Jiang, Z., Chen, H.-Y., and Philip Wong, H.-S. (2015). Metal oxide-resistive memory using graphene-edge electrodes. *Nat. Commun*. 6, 1–7. doi: 10.1038/ncomms9407

Lee, S. B., Chae, S. C., Chang, S. H., Lee, J. S., Seo, S., Kahng, B., et al. (2008b). Scaling behaviors of reset voltages and currents in unipolar resistance switching. *Appl. Phys. Lett*. 93, 212105. doi: 10.1063/1.3036532

Lee, S. W., Lee, H. J., Choi, J. H., Koh, W. G., Myoung, J. M., Hur, J. H., et al. (2010). Periodic array of polyelectrolyte-gated organic transistors from electrospun poly (3-hexylthiophene) nanofibers. *Nano Lett*. 10, 347–351. doi: 10.1021/nl903722z

Lei, X.-Y., Liu, H.-X., Gao, H.-X., Yang, H.-N., Wang, G.-M., Long, S.-B., et al. (2014). Resistive switching characteristics of Ti/ZrO2/Pt RRAM device. *Chinese Phys. B*. 23, 117305. doi: 10.1088/1674-1056/23/11/117305

Li, H., Wang, S., Zhang, X., Wang, W., Yang, R., Sun, Z., et al. (2021). Memristive crossbar arrays for storage and computing applications. *Adv. Intell. Syst*. 3, 2100017. doi: 10.1002/aisy.202100017

Li, H., Wu, T. F., Mitra, S., and Wong, H.-S. P. (2017). Resistive ram-centric computing: Design and modeling methodology. *IEEE TCAS-I*. 64, 2263–2273. doi: 10.1109/TCSI.2017.2709812

Li, N., Wang, Z., and Shi, Z. (2011). "Synthesis of graphenes with arc-discharge method," in *Physics and Applications of Graphene - Experiments*.

Li, Y., Wang, Z., Midya, R., Xia, Q., and Yang, J. J. (2018). Review of memristor devices in neuromorphic computing: materials sciences and device challenges. *J. Phys. D Appl. Phys*. 51, 503002. doi: 10.1088/1361-6463/aade3f

Li, Y.-T., Zhao, H.-M., Tian, H., Wang, X.-F., Mi, W.-T., Yang, Y., et al. (2016). "Novel graphene-based resistive random access memory," in *2016 13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)* (Hangzhou), 462–465.

Lin, C.-L., Chang, W.-Y., Huang, Y.-L., Juan, P.-C., Wang, T.-W., Hung, K.-Y., et al. (2015). Resistance switching behavior of zno resistive random access memory with a reduced graphene oxide capping layer. *Jpn. J. Appl. Phys*. 54, 04DJ08. doi: 10.7567/JJAP.54.04DJ08

Lin, C. Y., Wu, C. Y., Wu, C. Y. Y., Lee, T. C., Yang, F. L., Hu, C., et al. (2007). Effect of top electrode material on resistive switching properties of ZrO2 film memory devices. *IEEE Electron Device Letters* 28:366–368. doi: 10.1109/LED.2007.894652

Lin, Z., McCreary, A., Briggs, N., Subramanian, S., Zhang, K., Sun, Y., et al. (2016). 2D materials advances: from large scale synthesis and controlled heterostructures to improved characterization techniques, defects and applications. *2D Materials* 3, 042001. doi: 10.1088/2053-1583/3/4/042001

Liu, B., Liu, Z., Chiu, I.-S., Di, M., Wu, Y., Wang, J.-C., et al. (2018). Programmable synaptic metaplasticity and below femtojoule spiking energy realized in graphene-based neuromorphic memristor. *ACS Appl. Mater. Interf*. 10, 20237–20243. doi: 10.1021/acsami.8b04685

Liu, J., Yin, Z., Cao, X., Zhao, F., Wang, L., Huang, W., et al. (2013). Fabrication of flexible, all-reduced graphene oxide non-volatile memory devices. *Adv. Mater*. 25, 233–238. doi: 10.1002/adma.201203349

Liu, J., Zeng, Z., Cao, X., Lu, G., Wang, L. H., Fan, Q. L., et al. (2012). Preparation of MoS2-polyvinylpyrrolidone nanocomposites for flexible nonvolatile rewritable memory devices with reduced graphene oxide electrodes. *Small* 8, 3517–3522. doi: 10.1002/smll.201200999

Long, S., Lian, X., Ye, T., Cagli, C., Perniola, L., Miranda, E., et al. (2013). Cycle-to-cycle intrinsic RESET statistics in HfO2-based unipolar RRAM devices. *IEEE Electron Device Lett*. 34, 623–625. doi: 10.1109/LED.2013.2251314

Long, Y., Wu, L., Pan, F., Zhang, Z., Yang, M., Tang, A., et al. (2019). A graphene spin coatings for cost-effective corrosion protection for the magnesium alloy az31. *J. Nanosci. Nanotechnol*. 19, 105–111. doi: 10.1166/jnn.2019.16436

Lu, Q.., Zhao, Y.., Huang, L.., An, J.., Zheng, Y.., Yap, E. H., et al. (2023). Low-dimensional-materials-based flexible artificial synapse: materials, devices, and systems. *Nanomaterials* 13, 373. doi: 10.3390/nano13030373

Lu, W., Bao, N., Zheng, T., Zhang, X., and Song, Y. (2022). Memristor-based read/write circuit with stable continuous read operation. *Electronics* 11, 2018. doi: 10.3390/electronics11132018

Ma, W., Zidan, M. A., and Lu, W. D. (2018). Neuromorphic computing with memristive devices. *Sci. China Informat. Sci*. 61, 1–9. doi: 10.1007/s11432-017-9424-y

Meena, J. S., Sze, S. M., Chand, U., and Tseng, T. Y. (2014). Overview of emerging nonvolatile memory technologies. *Nanoscale Res. Lett*. 9, 1–33. doi: 10.1186/1556-276X-9-526

Mehonic, A., Sebastian, A., Rajendran, B., Simeone, O., Vasilaki, E., and Kenyon, A. J. (2020). Memristors from in-memory computing, deep learning acceleration, and spiking neural networks to the future of neuromorphic and bio-inspired computing. *Adv. Intellig. Syst.* 2:2000085. doi: 10.1002/aisy.202000085

Meyer, J., Hamwi, S., Kröger, M., Kowalsky, W., Riedl, T., and Kahn, A. (2012). Transition metal oxides for organic electronics: energetics, device physics and applications. *Adv. Mater.* 24, 5408–5427. doi: 10.1002/adma.201201630

Milo, V., Zambelli, C., Olivo, P., Pérez, E., K., Mahadevaiah, M., et al. (2019). Multilevel HfO2-based RRAM devices for low-power neuromorphic networks. *APL Mater.* 7, 81120. doi: 10.1063/1.5108650

Moon, J. S., and Gaskill, D. K. (2011). Graphene: its fundamentals to future applications. *IEEE Trans. Microw. Theory Tech.* 59, 2702–2708. doi: 10.1109/TMTT.2011.2164617

Mueller, N. S., Morfa, A. J., Abou-Ras, D., Oddone, V., Ciuk, T., and Giersig, M. (2014). Growing graphene on polycrystalline copper foils by ultra-high vacuum chemical vapor deposition. *Carbon N. Y.* 78, 347–355. doi: 10.1016/j.carbon.2014.07.011

Nagareddy, V. K., Barnes, M. D., Zipoli, F., Lai, K. T., Alexeev, A. M., Craciun, M. F., et al. (2017). Multilevel ultrafast flexible nanoscale nonvolatile hybrid graphene oxide-titanium oxide memories. *ACS Nano* 11, 3010–3021. doi: 10.1021/acsnano.6b08668

Nicolosi, V., Chhowalla, M., Kanatzidis, M. G., Strano, M. S., and Coleman, J. N. (2013). Liquid exfoliation of layered materials. *Science* 340, 1226419. doi: 10.1126/science.1226419

Ninomiya, T., Wei, Z., Muraoka, S., Yasuhara, R., Katayama, K., and Takagi, T. (2013). Conductive filament scaling of TaOx bipolar ReRAM for improving data retention under low operation current. *IEEE Trans. Electron Devices* 60, 1384–1389. doi: 10.1109/TED.2013.2248157

Novoselov, K. S., Geim, A. K., Morozov, S. V., Jiang, D., Zhang, Y., Dubonos, S. V., et al. (2004). Electric field in atomically thin carbon films. *Science* 306, 666–669. doi: 10.1126/science.1102896

Novoselov, K. S., Jiang, D., Schedin, F., Booth, T. J., Khotkevich, V. V., Morozov, S. V., et al. (2005). Two-dimensional atomic crystals. *Proc. Natl. Acad. Sci. USA*. 102, 10451–10453. doi: 10.1073/pnas.0502848102

Pan, C., Miranda, E., Villena, M. A., Xiao, N., Jing, X., Xie, X., et al. (2017). Model for multi-filamentary conduction in graphene/hexagonal-boron-nitride/graphene based resistive switching devices. *2D Materials* 4, 025099. doi: 10.1088/2053-1583/aa7129

Panin, G. N., Kapitanova, O. O., Lee, S. W., Baranov, A. N., and Kang, T. W. (2011). Resistive switching in al/graphene oxide/al structure. *Jpn. J. Appl. Phys.* 50, 070110. doi: 10.1143/JJAP.50.070110

Papageorgiou, D. G., Kinloch, I. A., and Young, R. J. (2017). Mechanical properties of graphene and graphene-based nanocomposites. *Prog. Mater. Sci.* 90, 75–127. doi: 10.1016/j.pmatsci.2017.07.004

Park, W. I., Yoon, J. M., Park, M., Lee, J., Kim, S. K., Jeong, J. W., et al. (2012). Self-assembly-induced formation of high-density silicon oxide memristor nanostructures on graphene and metal electrodes. *Nano Lett.* 12, 1235–1240. doi: 10.1021/nl203597d

Perez-Campos, A., Iriarte, F., Hernando-Garcia, J., and Calle, F. (2015). Post-CMOS compatible high-throughput fabrication of AlN-based piezoelectric microcantilevers. *J. Micromech. Microeng.* 25, 025003. doi: 10.1088/0960-1317/25/2/025003

Pradhan, S. K., Xiao, B., Mishra, S., Killam, A., and Pradhan, A. K. (2016). Resistive switching behavior of reduced graphene oxide memory cells for low power nonvolatile device application. *Sci. Rep.* 6, 1–9. doi: 10.1038/srep26763

Prakash, A., Deleruyelle, D., Song, J., Bocquet, M., and Hwang, H. (2015). Resistance controllability and variability improvement in a TaOx-based resistive memory for multilevel storage application. *Appl. Phys. Lett.* 106, 23. doi: 10.1063/1.4922446

Prakash, A., and Hwang, H. (2016). Multilevel cell storage and resistance variability in resistive random access memory. *Nano Devic. Sens.* 4, 49–72. doi: 10.1515/9781501501531-004

Prakash, A., and Hwang, H. (2019). Multilevel cell storage and resistance variability in resistive random access memory. *Phys. Sci. Rev.* 1, 6. doi: 10.1515/psr-2016-0010

Prodromakis, T., and Toumazou, C. (2010). "A review on memristive devices and applications," in *2010 17th IEEE International Conference on Electronics, Circuits and Systems*, 934–937. Athens: IEEE.

Puah, P. Y., Yusoff, U. H., Lee, P. C., MOH, P. Y., and How, S. E. (2020). Surface characterization, biocompatibility and osteogenic differentiation of drop-casted multilayer graphene oxide film towards human wharton's jelly derived mesenchymal stem cells. *Mater. Technol.* 35, 238–247. doi: 10.1080/10667857.2019.1674506

Qi, M., Tao, Y., Wang, Z., Xu, H., Zhao, X., Liu, W., et al. (2018). Highly uniform switching of HfO2–x based RRAM achieved through Ar plasma treatment for low power and multilevel storage. *Appl. Surf. Sci.* 458, 216–221. doi: 10.1016/j.apsusc.2018.07.095

Qian, K., Tay, R. Y., Nguyen, V. C., Wang, J., Cai, G., Chen, T., et al. (2016). Hexagonal boron nitride thin film for flexible resistive memory applications. *Adv. Funct. Mater.* 26, 2176–2184. doi: 10.1002/adfm.201504771

Qian, M., Pan, Y., Liu, F., Wang, M., Shen, H., He, D., et al. (2014). Tunable, ultralow-power switching in memristive devices enabled by a heterogeneous graphene-oxide interface. *Adv. Mater.* 26, 3275–3281. doi: 10.1002/adma.201306028

Rani, A., Song, J.-M., Jung Lee, M., and Lee, J.-S. (2012). Reduced graphene oxide based flexible organic charge trap memory devices. *Appl. Phys. Lett.* 101, 233308. doi: 10.1063/1.4769990

Rehman, M. M., Rehman, H. M. M. U., Gul, J. Z., Kim, W. Y., Karimov, K. S., and Ahmed, N. (2020). Decade of 2d-materials-based rram devices: a review. *Sci. Technol. Adv. Mater.* 21, 147–186. doi: 10.1080/14686996.2020.1730236

Rehman, M. M., Siddiqui, G. U., Doh, Y. H., and Choi, K. H. (2017). Highly flexible and electroforming free resistive switching behavior of tungsten disulfide flakes fabricated through advanced printing technology. *Semicond. Sci. Technol.* 32, 095001. doi: 10.1088/1361-6641/aa77db

Rodriguez, S., Vaziri, S., Ostling, M., Rusu, A., Alarcon, E., and Lemme, M. C. (2012). Rf performance projections of graphene fets vs. silicon mosfets. *ECS Solid State Lett.* 1, Q39. doi: 10.1149/2.001205ssl

Rose, G. S., and Meade, C. A. (2015). "Performance analysis of a memristive crossbar puf design," in *2015 52nd ACM/EDAC/IEEE Design Automation Conference (DAC)*. San Francisco, CA: IEEE, 1–6. doi: 10.1145/2744769.2744892

Saini, P., Singh, M., Thakur, J., Patil, R., Ma, Y. R., Tandon, R. P., et al. (2018). Probing the mechanism for bipolar resistive switching in annealed graphene oxide thin films. *ACS Appl. Mater. Interfaces*. 10:6521–6530. doi: 10.1021/acsami.7b09447

Sano, K., Hatsuda, Y., and Yamamoto, S. (2013). Multi-fpga accelerator for scalable stencil computation with constant memory bandwidth. *IEEE Trans. Parallel Distrib. Syst.* 25, 695–705. doi: 10.1109/TPDS.2013.51

Sawa, A. (2008). Resistive switching in transition metal oxides. *Mater. Today* 11, 28–36. doi: 10.1016/S1369-7021(08)70119-6

Schranghamer, T. F., Oberoi, A., and Das, S. (2020). Graphene memristive synapses for high precision neuromorphic computing. *Nat. Commun.* 11, 1–11. doi: 10.1038/s41467-020-19203-z

Sharma, I., Papanai, G. S., Paul, S. J., and Gupta, B. K. (2020). Partial pressure assisted growth of single-layer graphene grown by low-pressure chemical vapor deposition: implications for high-performance graphene FET devices. *ACS Omega* 5, 22109–22118. doi: 10.1021/acsomega.0c02132

Shehab, M., Abualigah, L., Omari, M., Shambour, M. K. Y., Alshinwan, M., Abuaddous, H. Y., et al. (2022). "Artificial neural networks for engineering applications: a review," in *Artificial Neural Networks for Renewable Energy Systems and Real-World Applications*. Cambridge, MA: Academic Press, 189–206.

Shin, Y. J., Kwon, J. H., Kalon, G., Lam, K.-T., Bhatia, C. S., Liang, G., et al. (2010). Ambipolar bistable switching effect of graphene. *Appl. Phys. Lett.* 97, 262105. doi: 10.1063/1.3532849

Shindome, A., Doioka, Y., Beppu, N., Oda, S., and Uchida, K. (2013). Experimental study of two-terminal resistive random access memory realized in mono- and multilayer exfoliated graphene nanoribbons. *Jpn. J. Appl. Phys.* 52, :04CN05. doi: 10.7567/JJAP.52.04CN05

Singh, D. P., Herrera, C. E., Singh, B., Singh, S., Singh, R. K., and Kumar, R. (2018). Graphene oxide: an efficient material and recent approach for biotechnological and biomedical applications. *Mater. Sci. Eng. C* 86, 173–197. doi: 10.1016/j.msec.2018.01.004

Sohn, J., Lee, S., Jiang, Z., Chen, H. Y., and Wong, H. S. (2015). *Atomically Thin Graphene Plane Electrode for 3D RRAM*. Washington, DC: Technical Digest - International Electron Devices Meeting, IEDM, 1–5.

Sparvoli, M., and Marma, J. S. (2018). "Development of resistive memories based on silver doped graphene oxide for neuron simulation," in *2018 International Joint Conference on Neural Networks*, Rio de Janeiro, Brazil: IEEE, 1–6.

Starzyk, J. A., and Basawaraj. (2014). Memristor crossbar architecture for synchronous neural networks. *IEEE Trans. Circuits Syst. I: Regul. Pap.* 61, 2390–2401. doi: 10.1109/TCSI.2014.2304653

Strukov, D. B., Snider, G. S., Stewart, D. R., and Williams, R. S. (2008). The missing memristor found. *Nature* 453, 80–83. doi: 10.1038/nature06932

Sun, B., Zhao, W., Liu, Y., and Chen, P. (2015). Resistive switching effect of ag/mos 2/fto device. *Function. Mater. Lett.* 8, 1550010. doi: 10.1142/S1793604715500101

Sung, S. H., Kim, T. J., Shin, H., Im, T. H., and Lee, K. J. (2022). Simultaneous emulation of synaptic and intrinsic plasticity using a memristive synapse. *Nat. Commun.* 13, 1. doi: 10.1038/s41467-022-30432-2

Terai, M., Sakotsubo, Y., Kotsuji, S., and Hada, H. (2010). Resistance controllability of Ta2O5/TiO2 stack ReRAM for low-voltage and multilevel operation. *IEEE Electron. Device Lett.* 31, 204–206. doi: 10.1109/LED.2009.2039021

Tsigkourakos, M., Bousoulas, P., Aslanidis, V., Skotadis, E., and Tsoukalas, D. (2017). Ultra-low power multilevel switching with enhanced uniformity in forming free tio2- x-based rram with embedded pt nanocrystals. *Physica Status Solidi* 214, 1700570. doi: 10.1002/pssa.201700570

Uddin, M., Majumder, M. B., and Rose, G. S. (2017). Robustness analysis of a memristive crossbar puf against modeling attacks. *IEEE Trans. Nanotechnol.* 16, 396–405. doi: 10.1109/TNANO.2017.2677882

Vasu, K., Sampath, S., and Sood, A. (2011). Nonvolatile unipolar resistive switching in ultrathin films of graphene and carbon nanotubes. *Solid State Commun.* 151, 1084–1087. doi: 10.1016/j.ssc.2011.05.018

Venugopal, G., and Kim, S. J. (2012). Observation of nonvolatile resistive memory switching characteristics in Ag/graphene-oxide/Ag devices. *J. Nanosci. Nanotechnol.* 12, 8522–8525. doi: 10.1166/jnn.2012.6675

Vourkas, I., Stathis, D., Sirakoulis, G. C., and Hamdioui, S. (2016). Alternative architectures toward reliable memristive crossbar memories. *IEEE Transact. Very Large Scale Integrat. (VLSI) Syst.* 24, 206–217. doi: 10.1109/TVLSI.2015.2388587

Wang, C.-H., McClellan, C., Shi, Y., Zheng, X., Chen, V., Lanza, M., et al. (2018). "3d monolithic stacked 1t1r cells using monolayer mos 2 fet and hbn rram fabricated at low (150c) temperature," in *2018 IEEE International Electron Devices Meeting (IEDM)*, 22–5. San Francisco, CA: IEEE.

Wang, L.-H., Yang, W., Sun, Q.-Q., Zhou, P., Lu, H.-L., Ding, S.-J., et al. (2012a). The mechanism of the asymmetric set and reset speed of graphene oxide based flexible resistive switching memories. *Appl. Phys. Lett.* 100, 063509. doi: 10.1063/1.3681366

Wang, S. Y., Lee, D. Y., Tseng, T. Y., and Lin, C. Y. (2009). Effects of Ti top electrode thickness on the resistive switching behaviors of rf-sputtered ZrO2 memory films. *Appl. Phys. Lett.* 95, 112904. doi: 10.1063/1.3231872

Wang, Z., Tjoa, V., Wu, L., Liu, W., Fang, Z., Tran, X. A., et al. (2012b). Mechanism of different switching directions in graphene oxide based rram. *J. Electrochem. Soc.* 159, K177. doi: 10.1149/2.068206jes

Wu, C., Li, F., Zhang, Y., and Guo, T. (2012). Recoverable electrical transition in a single graphene sheet for application in nonvolatile memories. *Appl. Phys. Lett.* 100, 042105. doi: 10.1063/1.3680093

Wu, C., Li, F., and Guo, T. (2014). Efficient tristable resistive memory based on single layer graphene/insulating polymer multi-stacking layer. *Appl. Phys. Lett.* 104, 183105. doi: 10.1063/1.4875596

Wu, H. Y., Lin, C. C., and Lin, C. H. (2015a). Characteristics of graphene-oxide-based flexible and transparent resistive switching memory. *Ceramics Int.* 41, S823–S828. doi: 10.1016/j.ceramint.2015.03.129

Wu, Q., Banerjee, W., Cao, J., Ji, Z., Li, L., and Liu, M. (2018). Improvement of durability and switching speed by incorporating nanocrystals in the hfox based resistive random access memory devices. *Appl. Phys. Lett.* 113, 5030780. doi: 10.1063/1.5030780

Wu, X., Saxena, V., and Zhu, K. (2015b). Homogeneous spiking neuromorphic system for real-world pattern recognition. *IEEE J. Emerg. Select. Top. Circ. Syst.* 5, 254–266. doi: 10.1109/JETCAS.2015.2433552

Wu, Y., Lee, B., and Wong, H. S. (2010). Al2O3-based RRAM using atomic layer deposition (ALD) with 1-μa RESET current. *IEEE Electron Devi. Lett.* 31, 1449–1451. doi: 10.1109/LED.2010.2074177

Wu, Y., Wang, L., Jin, M., Kong, F., Qi, H., and Nan, J. (2019). Reduced graphene oxide and biofilms as cathode catalysts to enhance energy and metal recovery in microbial fuel cell. *Bioresour. Technol.* 283, 129–137. doi: 10.1016/j.biortech.2019.03.080

Xia, Q., and Yang, J. J. (2019). Memristive crossbar arrays for brain-inspired computing. *Nature Mater.* 18, 309–323. doi: 10.1038/s41563-019-0291-x

Xie, J., Afshari, S., and Sanchez Esqueda, I. (2022). Hexagonal boron nitride (h-BN) memristor arrays for analog-based machine learning hardware. *NPJ 2D Mater. Appl.* 6, 1–7. doi: 10.1038/s41699-022-00328-2

Xu, R., Jang, H., Lee, M. H., Amanov, D., Cho, Y., Kim, H., et al. (2019a). Vertical MoS2 double-layer memristor with electrochemical metallization as an atomic-scale synapse with switching thresholds approaching 100 mV. *Nano Lett.* 19, 2411–2417. doi: 10.1021/acs.nanolett.8b05140

Xu, W., Wang, J., and Yan, X. (2021). Advances in memristor-based neural networks. *Front. Nanotechnol.* 3, 20. doi: 10.3389/fnano.2021.645995

Xu, Z., Li, F., Wu, C., Ma, F., Zheng, Y., Yang, K., et al. (2019b). Ultrathin electronic synapse having high temporal/spatial uniformity and an al2o3/graphene quantum dots/al2o3 sandwich structure for neuromorphic computing. *NPG Asia Mater.* 11, 1–11. doi: 10.1038/s41427-019-0118-x

Xue, C. J., Zhang, Y., Chen, Y., Sun, G., Yang, J. J., and Li, H. (2011). "*Emerging non-volatile memories: Opportunities and challenges*," in *Proceedings of the Seventh IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis* (New York, NY), 325–334.

Yakopcic, C., Fernando, B. R., and Taha, T. M. (2019). "Design space evaluation of a memristor crossbar based multilayer perceptron for image processing," in *2019 International Joint Conference on Neural Networks (IJCNN)*, 1–8. Budapest: IEEE. doi: 10.1109/IJCNN.2019.8852005

Yan, X., Zhang, L., Chen, H., Li, X., Wang, J., Liu, Q., et al. (2018). Graphene oxide quantum dots based memristors with progressive conduction tuning for artificial synaptic learning. *Adv. Funct. Mater.* 28, 1803728. doi: 10.1002/adfm.201803728

Yang, J. J., and Williams, R. S. (2013). Memristive devices in computing system: promises and challenges. *ACM J. Emerg. Technol. Comput. Syst. (JETC)* 9, 1–20. doi: 10.1145/2463585.2463587

Yang, L., Kuegeler, C., Szot, K., Ruediger, A., and Waser, R. (2009). The influence of copper top electrodes on the resistive switching effect in TiO2 thin films studied by conductive atomic force microscopy. *Appl. Phys. Lett.* 95, 013109. doi: 10.1063/1.3167810

Yansong, G., C., R. D., Said, A.-S., Kavehei, O., and Abbott, D. (2015). Memristive crypto primitive for building highly secure physical unclonable functions. *Sci. Rep.* 5, 12785. doi: 10.1038/srep12785

Yao, J., Lin, J., Dai, Y., Ruan, G., Yan, Z., Li, L., et al. (2012). Highly transparent nonvolatile resistive memory devices from silicon oxide and graphene. *Nat. Commun.* 3, 1101. doi: 10.1038/ncomms2110

Yeh, C.-W. S., and Wong, S. S. (2015). Compact one-transistor-n-rram array architecture for advanced cmos technology. *IEEE J. Solid-State Circ.* 50, 1299–1309. doi: 10.1109/JSSC.2015.2402217

Yi, M., Cao, Y., Ling, H., Du, Z., Wang, L., Yang, T., et al. (2014). Temperature dependence of resistive switching behaviors in resistive random access memory based on graphene oxide film. *Nanotechnology* 25, 185202. doi: 10.1088/0957-4484/25/18/185202

Ying-Chih Lai, C., Hsu, F.-C., Chen, J.-Y., He, J.-H., Chang, T.-C., Hsieh, Y.-P., et al. (2013). Transferable and flexible label-like macromolecular memory on arbitrary substrates with high performance and a facile methodology. *Adv. Mater.* 25, 2733–2739. doi: 10.1002/adma.201205280

Yu, F., Kong, X., Mokbel, A. A. M., Yao, W., and Cai, S. (2023). Complex dynamics, hardware implementation and image encryption application of multiscroll memeristive hopfield neural network with a novel local active memeristor. *IEEE Trans. Circuits Syst II: Express Briefs* 70, 326–330. doi: 10.1109/TCSII.2022.3218468

Yu, J., Du Nguyen, H. A., Xie, L., Taouil, M., and Hamdioui, S. (2018). "Memristive devices for computation-in-memory," in *2018 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. Dresden: IEEE, 1646–1651.

Yu, J., Sun, W., Lai, J., Zheng, X., Dong, D., Luo, Q., et al. (2022). Performance improvement of memristor-based echo state networks by optimized programming scheme. *IEEE Electron Devi. Lett.* 43, 866–869. doi: 10.1109/LED.2022.3165831

Yu, S., Guan, X., and Wong, H. S. (2012). On the switching parameter variation of metal oxide RRAM - part II: model corroboration and device design strategy. *IEEE Trans. Electron Devices* 59, 1183–1188. doi: 10.1109/TED.2012.2184544

Yu, S., Jeyasingh, R., Wu, Y., and Philip Wong, H. S. (2011a). *Understanding the Conduction and Switching Mechanism of Metal Oxide RRAM Through low Frequency Noise and AC Conductance Measurement and Analysis*. Washington, DC: Technical Digest - International Electron Devices Meeting, IEDM.

Yu, W. J., Chae, S. H., Lee, S. Y., Duong, D. L., and Lee, Y. H. (2011b). Ultra-transparent, flexible single-walled carbon nanotube non-volatile memory device with an oxygen-decorated graphene electrode. *Adv. Mater.* 23, 1889–1893. doi: 10.1002/adma.201004444

Yung, K. C., Wu, W. M., Pierpoint, M. P., and Kusmartsev, F. V. (2013). Introduction to graphene electronics a new era of digital transistors and devices. *Contemporary Physics.* 54, 233–251. doi: 10.1080/00107514.2013.833701

Zahoor, F., Azni Zulkifli, T. Z., and Khanday, F. A. (2020). Resistive random access memory (RRAM): an overview of materials, switching mechanism, performance, multilevel cell (mlc) storage, modeling, and applications. *Nanoscale Res. Lett.* 15, 1–26. doi: 10.1186/s11671-020-03299-9

Zhang, F., Krylyuk, S., Zhang, H., Milligan, C. A., Zemlyanov, D. Y., Bendersky, L. A., et al. (2018). Electric field induced phase transition in vertical MoTe2 and Mo1-xWxTe2 based RRAM devices. *Nat. Mater.* 18, 55–61. doi: 10.1038/s41563-018-0234-y

Zhang, F., Li, C., Li, Z., Dong, L., and Zhao, J. (2023). Recent progress in three-terminal artificial synapses based on 2D materials: from mechanisms to applications. *Microsyst. Nanoeng.* 9, 1–17. doi: 10.1038/s41378-023-00487-2

Zhang, H. (2015). Ultrathin two-dimensional nanomaterials. *ACS Nano* 9, 9451–9469. doi: 10.1021/acsnano.5b05040

Zhang, S., Long, S., Guan, W., Liu, Q., Wang, Q., and Liu, M. (2009). Resistive switching characteristics of MnOx-based ReRAM. *J. Phys. D Appl. Phys.* 42, 055112. doi: 10.1088/0022-3727/42/5/055112

Zhang, Y., Ren, W., Jiang, Z., Yang, S., Jing, W., Shi, P., et al. (2014a). Low-temperature remote plasma-enhanced atomic layer deposition of graphene and characterization of its atomic-level structure. *J. Mater. Chem. C* 2, 7570–7574. doi: 10.1039/C4TC00849A

Zhang, Z., Gao, B., Fang, Z., Wang, X., Tang, Y., Sohn, J., et al. (2014b). All-metal-nitride rram devices. *IEEE Electron Dev. Lett.* 36, 29–31. doi: 10.1109/LED.2014.2367542

Zhang, Z., Yang, D., Li, H., Li, C., Wang, Z., Sun, L., et al. (2022). 2d materials and van der waals heterojunctions for neuromorphic computing. *Neuromorphic Comput. Eng.* 2, 032004. doi: 10.1088/2634-4386/ac8a6a

Zhao, H., Tu, H., Wei, F., and Du, J. (2014a). Highly transparent dysprosium oxide-based rram with multilayer graphene electrode for low-power nonvolatile memory application. *IEEE Trans. Electron Dev.* 61, 1388–1393. doi: 10.1109/TED.2014.2312611

Zhao, L., Chen, H. Y., Wu, S. C., Jiang, Z., Yu, S., Hou, T. H., et al. (2014b). Multi-level control of conductive nano-filament evolution in HfO2 ReRAM by pulse-train operations. *Nanoscale* 6, 5698–5702. doi: 10.1039/C4NR00500G

Zhong, Y. L., Tian, Z., Simon, G. P., and Li, D. (2015). Scalable production of graphene via wet chemistry: progress and challenges. *Mater. Today* 18 73–78. doi: 10.1016/j.mattod.2014.08.019

Zhou, F., Chen, J., Tao, X., Wang, X., and Chai, Y. (2019). 2D materials based optoelectronic memory: convergence of electronic memory and optical sensor. *Research*. 2019, :9490413. doi: 10.34133/2019/9490413

Zhou, G., Lu, Z., Yao, Y., Wang, G., Yang, X., Zhou, A., et al. (2017). Mechanism for bipolar resistive switching memory behaviors of a self-assembled three-dimensional mos2 microsphere composed active layer. *J. Appl. Phys.* 121, 15. doi: 10.1063/1.4980173

Zhou, G., Sun, B., Yao, Y., Zhang, H., Zhou, A., Alameh, K., et al. (2016). Investigation of the behaviour of electronic resistive switching memory based on mose2-doped ultralong se microwires. *Appl. Phys. Lett*. 109, 14. doi: 10.1063/1.4962655

Zhu, L., Zhou, J., Guo, Z., and Sun, Z. (2015). An overview of materials issues in resistive random access memory. *J. Materiom.* 1, 285–295. doi: 10.1016/j.jmat.2015.07.009

Zhu, W., Low, T., Wang, H., Ye, P., and Duan, X. (2019). Nanoscale electronic devices based on transition metal dichalcogenides. *2D Materials* 6, 032004. doi: 10.1088/2053-1583/ab1ed9