



Low-Cutoff Frequency Reduction in Neural Amplifiers: Analysis and Implementation in CMOS 65 nm

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Specialty section:

This article was submitted to
Neural Technology,
a section of the journal
Frontiers in Neuroscience

Received: 14 February 2021

Accepted: 04 May 2021

Published: 02 June 2021

Citation:

Hashemi Noshahr F, Nabavi M,
Gosselin B and Sawan M (2021)
Low-Cutoff Frequency Reduction in
Neural Amplifiers: Analysis and
Implementation in CMOS 65 nm.
Front. Neurosci. 15:667846.
doi: 10.3389/fnins.2021.667846

Scaling down technology demotes the parameters of AC-coupled neural amplifiers, such as increasing the low-cutoff frequency due to the short-channel effects. To improve the low-cutoff frequency, one solution is to increase the feedback capacitors' value. This solution is not desirable, as the input capacitors have to be increased to maintain the same gain, which increases the area and decreases the input impedance of the neural amplifier. We analytically analyze the small-signal behavior of the neural amplifier and prove that the main reason for the increase of the low-cutoff frequency in advanced CMOS technologies is the reduction of the input resistance of the operational transconductance amplifier (OTA). We also show that the reduction of the input resistance of the OTA is due to the increase in the gate oxide leakage in the input transistors. In this paper, we explore this fact and propose two solutions to reduce the low-cutoff frequency without increasing the value of the feedback capacitor. The first solution is performed by only simulation and is called cross-coupled positive feedback that uses pseudo-resistors to provide a negative resistance to increase the input resistance of the OTA. As an advantage, only standard CMOS transistors are used in this method. Simulation results show that a low-cutoff frequency of 1.5 Hz is achieved while the midband gain is 30.4 dB at 1 V. In addition, the power consumption is 0.6 μ W. In the second method, we utilize thick-oxide MOS transistors in the input differential pair of the OTA. We designed and fabricated the second method in the 65 nm TSMC CMOS process. Measured results are obtained by *in vitro* recordings on slices of mouse brainstem. The measurement results show that the bandwidth is between 2 Hz and 5.6 kHz. The neural amplifier has 34.3 dB voltage gain in midband and consumes 3.63 μ W at 1 V power supply. The measurement results show an input-referred noise of 6.1 μ V_{rms} and occupy 0.04 mm² silicon area.

Keywords: neural amplifier, low noise, low-power, low-cutoff frequency, compact

1. INTRODUCTION

Neural signal acquisition has a crucial role in understanding the function of the different parts of the brain as well as exploring and treating its various disorders (Stevenson and Kording, 2011). In addition, this data is used in developing the neural prostheses (Sun et al., 2008) and brain machine interfaces (BMI) (Fifer et al., 2012). This is why the demand for new techniques that enable

monitoring brain activity wirelessly through implantable devices is increasing every day (Schwartz et al., 2006; Mollazadeh et al., 2009; Cook et al., 2013). A complete review on neural recording is given in Hashemi Noshahr et al. (2020) and Luan et al. (2020).

Brain signals are very small and have very low bandwidth. For instance, the maximum amplitude of local field potentials (LFP) is typically 1 mV and the frequency range is <1 Hz up to 300 Hz (Van Rijn et al., 1991). On the other hand, the amplitude of the spikes or the neural action potentials (AP) are typically as high as 500 μ V and their operational frequency is up to 7 kHz (Najafi and Wise, 1986).

Increasing the number of the neural recording sites, which are called channels, is required in some applications, as the spatial resolution of the capturing signals increases. As an example, the total number of channels reported in Musk (2019) is 3072. The electrochemical reaction at the electrode-tissue interface in each channel generates different DC offset voltages across the various electrodes. These voltages vary typically between 1 and 10 mV and in some cases up to 50 mV (Bagheri et al., 2017). As the offset voltages of the channels have high value, they can saturate the neural amplifier. Therefore, they should be eliminated. The most common approach to block this DC input offset is to utilize large AC-coupling capacitors (Harrison and Charles, 2003; Ng and Xu, 2012). On the other hand, there is an alternative method that blocks these DC offset voltages by using a low-pass filter in the feedback path, which is called DC-coupled input offset rejection. The authors in Enz et al. (1995), Yazicioglu et al. (2008), Muller et al. (2012), Biederman et al. (2013), Lee et al. (2019), Jomehei and Sheikhaei (2019), Cabrera et al. (2020), and Farouk et al. (2020) use this method, however, it requires a huge capacitor or high power consumption amplifier in the feedback path.

To design multichannel neural amplifiers, the following factors should be considered and diminished as much as possible.

1. Power consumption: the brain tissues that are surrounded by implantable neuro-amplifiers must be protected from heat damage. For this purpose, the power dissipation of these amplifiers must be lowered.
2. Chip area: The neural amplifiers are generally huge. This is because they usually utilize large AC-coupled input capacitors. Also, to decrease the flicker-noise power of amplifiers, the size of the MOS transistors is designed to be very large especially in the differential pairs. Therefore, for a specific chip area, to maximize the number of the channels, the amplifiers should be designed in their minimum area.
3. Noise: the neural signals have very low amplitude and bandwidth. The flicker and thermal noise of the neural amplifier circuit is the main source of the noise, which can decrease the signal to noise ratio (SNR) in the output of the amplifiers. This is why they are designed as a low noise amplifier (LNA). In the low frequency, the power of the flicker noise is dominant. To decrease the flicker-noise power, in addition to increasing the size of the transistors and utilizing a PMOS differential pair, the chopper-stabilization technique is used (Denison et al., 2007; Verma et al., 2010; Xu et al., 2011; Yazicioglu et al., 2011; Luo et al., 2019; Samiei and Hashemi, 2019). The chopper-stabilization technique modulates the

low-frequency noise of the OTA (flicker noise), as well as the offset voltage to a higher frequency by the chopper switches. These higher frequencies are eliminated with a low pass filter (LPF).

The 65 nm CMOS and finer technologies introduce new challenges as a result of the short channel effects for analog circuits. One of these challenges is decreasing the transconductance (g_m) of MOS transistors, which diminishes the voltage gain of the whole amplifier. This can be resolved by designing the neural amplifier in 2 or 3 gain stages (Zou et al., 2009; Rezaee-Dehsorkh et al., 2011). The other destructive effect of short channel effects is increasing the low-cutoff frequency (f_L) of the AC-coupled neural amplifiers. In this paper, we analyze the parameters that affect the low-cutoff frequency and propose two solutions. The first solution utilizes a standard CMOS

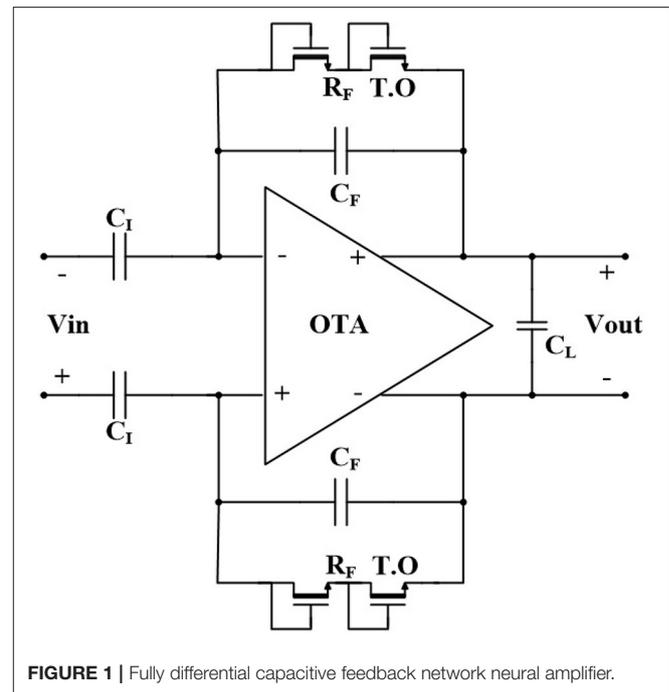


FIGURE 1 | Fully differential capacitive feedback network neural amplifier.

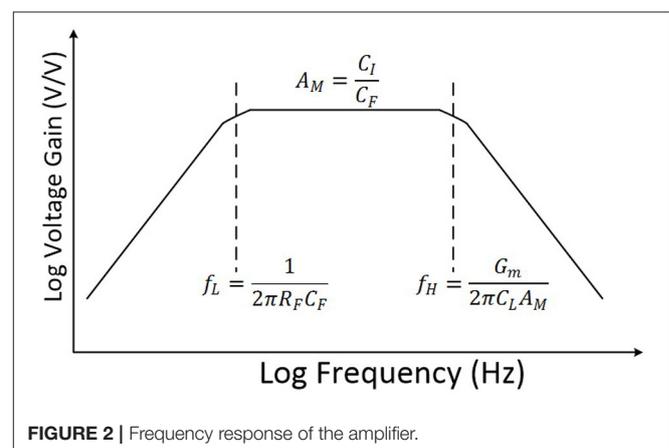


FIGURE 2 | Frequency response of the amplifier.

and improves the low-cutoff frequency by increasing the input resistance. The second method utilizes thick-oxide transistors to increase the input resistance.

The rest of the paper is organized as follows. Section II analyzes the low-cutoff frequency in neural amplifiers. Section III presents the two proposed solutions. The experimental results are provided in Section IV and the paper concludes in section V.

2. LOW-CUTOFF FREQUENCY ANALYSIS

Figure 1 shows the schematic of a fully differential neural amplifier with conventional capacitive feedback network (CFN) architecture. As explained in Harrison and Charles (2003), this architecture is one of the most popular architectures of AC-coupled neural amplifiers in terms of low power consumption, low noise, and compact area. Also, utilizing thick-oxide NMOS pseudoresistors instead of PMOS pseudoresistors, provides a better total harmonic distortion (THD) (Kassiri et al., 2013).

Figure 2 shows the frequency response of this CFN neural amplifier as a bandpass amplifier. Assuming that the voltage

gain of the operational transconductance amplifier (OTA) is significantly high, the voltage gain of the amplifier in the midband (A_M) can be approximately calculated by

$$A_M = \frac{C_I}{C_F} \tag{1}$$

where C_I and C_F are input and feedback capacitance of the amplifier, respectively. Also, the low-cutoff frequency (f_L) of the amplifier can be approximated as

$$f_L = \frac{1}{2\pi R_F C_F} \tag{2}$$

where R_F is the dynamic resistance of NMOS pseudoresistors of the amplifier.

As presented in Equation 2, in order to reduce f_L , C_F and R_F should be increased. However, by increasing C_F , it is required to increase C_I to maintain the same gain which results in huge area loss for each channel of a multi channel device. In addition,

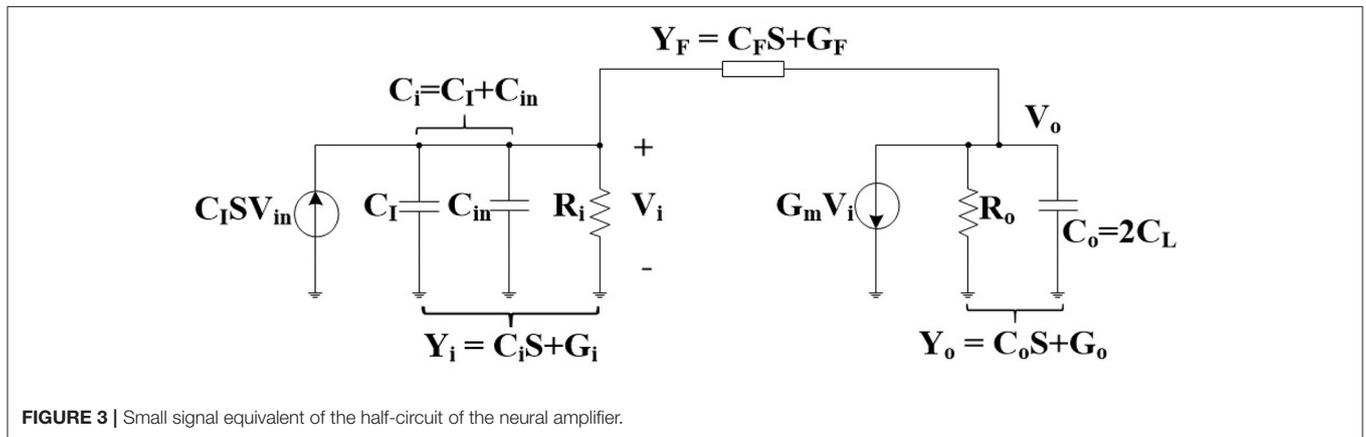


FIGURE 3 | Small signal equivalent of the half-circuit of the neural amplifier.

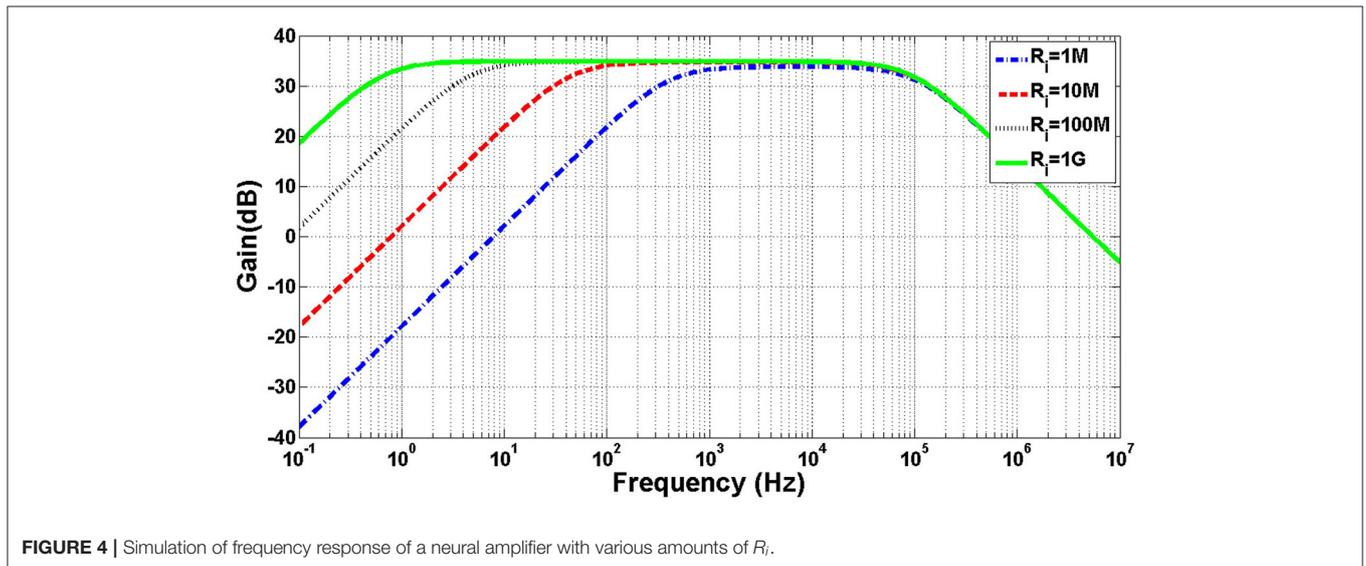


FIGURE 4 | Simulation of frequency response of a neural amplifier with various amounts of R_i .

this results in the reduction of the input impedance of the neural amplifier.

MOS pseudoresistors can be utilized as a feedback resistance (R_F) for their compactness and high resistance. However, the drawback of this technique is that the MOS pseudoresistors provide much less resistance in advanced technology. For example, in an old technology such as $1.5 \mu\text{m}$ CMOS technology, by utilizing a MOS pseudoresistor for the R_F , a C_F of only 200 fF is enough to achieve a f_L of 0.025 Hz (Harrison and Charles, 2003). However, with the same technique and the same value for C_F , a f_L of 39 Hz is reported in the 180 nm CMOS technology (Shoaran et al., 2014). Moreover, in the 130 nm CMOS technology (Abdelhalim et al., 2013), a higher C_F of 300 fF is used to compensate for the low R_F to provide a f_L of 0.1 Hz. Moreover, in the 65 nm CMOS technology, our simulation results show that when a C_F of 200 fF is used, the f_L is achieved at 472 Hz. To better understand the effects that increase the f_L value in the

advanced CMOS technologies, we provide a small signal analysis of the amplifier in the following.

The equivalent small signal half-circuit of a neural amplifier of **Figure 1** is depicted in **Figure 3**. The OTA can be modeled as a single pole amplifier with a pole at the output node. In this figure, G_m is the transconductance of the OTA and C_{in} , R_i , and R_o are OTA's input terminal capacitance, resistance, and the output terminal resistance, respectively. We extract the time constant of the first pole as

$$\tau_1 = \frac{1}{p_1} = \tag{3}$$

$$= \frac{C_F(G_o + G_m) + C_oG_F + C_i(G_o + G_F) + G_i(C_o + C_F)}{G_F(G_m + G_o) + G_i(G_F + G_o)}$$

Reduction of the oxide thickness in advanced technologies translates to lower input resistance (i.e., higher G_i) due to higher gate leakage current. By increasing G_i , the denominator in Equation (3) grows much faster than the numerator. Therefore, the time constant (τ_1) increases resulting in lower f_L .

However, for older technologies, we can simplify Equations (3) to (4) with the assumption that OTA's input resistance (R_i) is infinity (i.e., G_i is approximately zero) (Hashemi Noshahr and Sawan, 2017).

$$\tau_1 = \frac{1}{p_1} = R_F C_F + \frac{C_o R_o}{1 + G_m R_o} + \frac{C_i (R_F + R_o)}{1 + G_m R_o} \tag{4}$$

If the gain of the OTA ($G_m R_o$) is high, the second and third terms of this equation can be considered negligible resulting in Equation (5) where the corresponding frequency to τ_1 is the same as Equation (2). In other words, Equation (5) is a special case of Equation (3) where the gain of the OTA is high and the input resistance of the OTA is infinity.

$$\tau_1 = \frac{1}{p_1} = R_F C_F \tag{5}$$

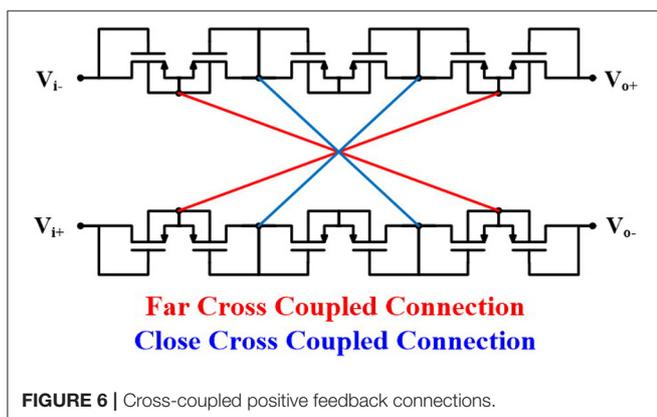
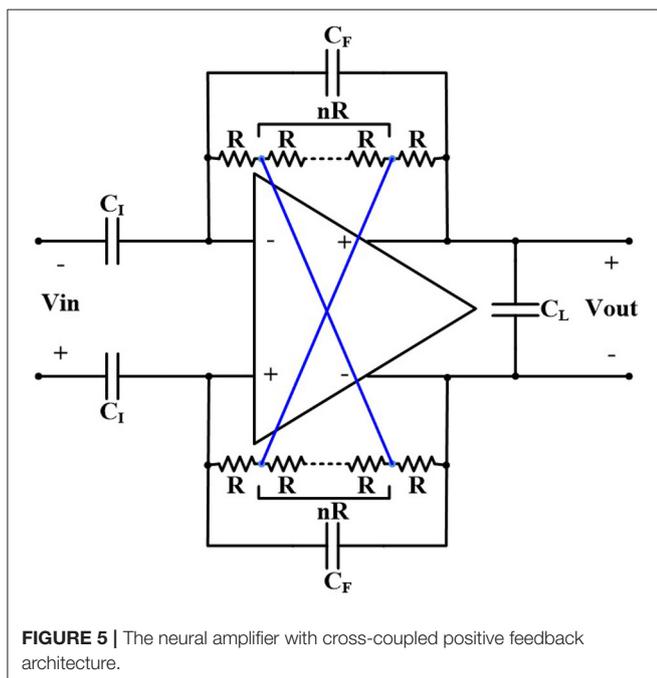
Figure 4 illustrates the frequency response of the small signal model of the amplifier shown in **Figure 3** for different values of R_i . The DC voltage of the outputs is biased at 0.5 V and thick-oxide NMOS pseudoresistors are utilized for feedback resistors. The values of G_m , R_o , C_I , C_F , C_{in} , and C_o are chosen as $22.4 \mu\text{S}$, $157 \text{ M}\Omega$, 11.5 pF , 200 fF , 3 pF , and 200 fF , respectively. As shown in this figure, f_L decreases by increasing R_i .

3. PROPOSED SOLUTIONS

In this section, we propose two solutions to decrease the low-cutoff frequency down to 1 Hz of OTA's in advanced CMOS technologies without increasing the feedback capacitance (C_F).

3.1. Cross-Coupled Positive Feedback

Figure 5 shows the architecture of the neural amplifier with cross-coupled positive feedback (CCPF) connections



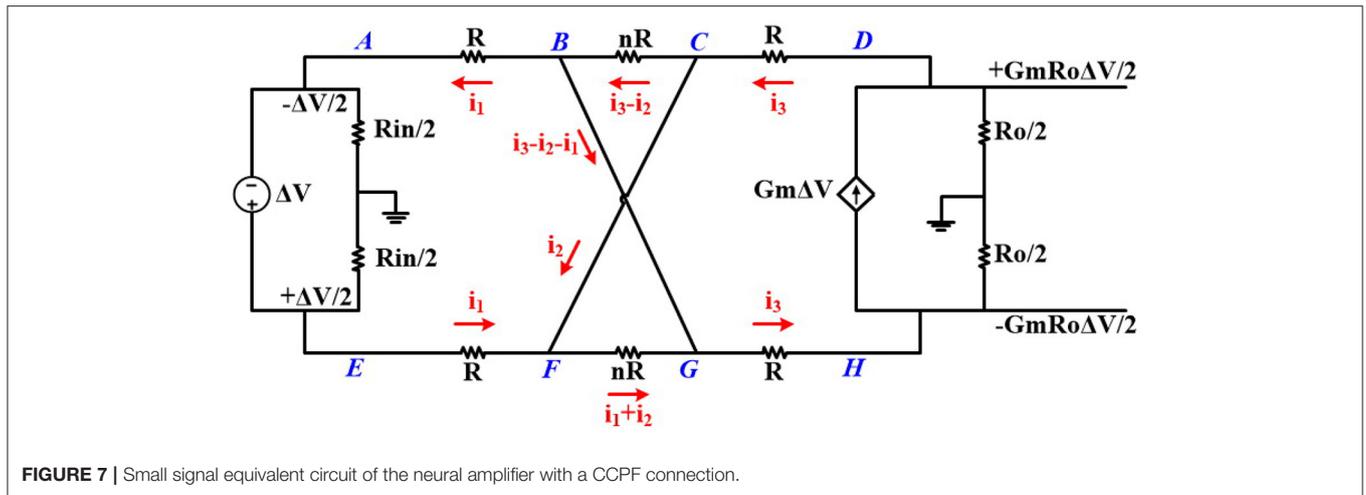


FIGURE 7 | Small signal equivalent circuit of the neural amplifier with a CCPF connection.

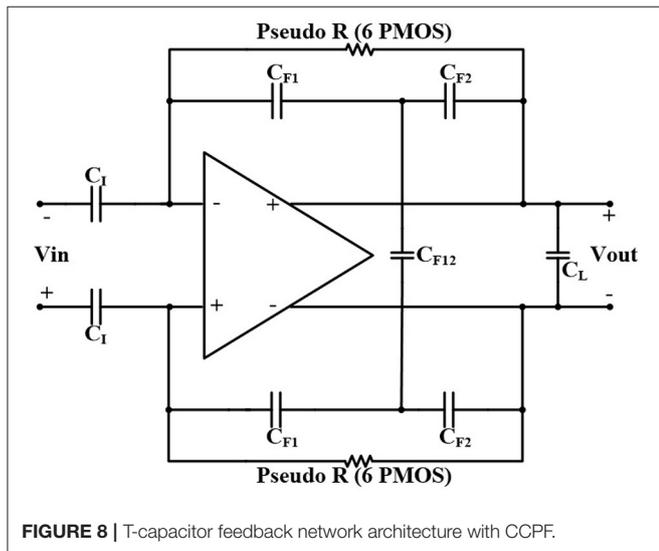


FIGURE 8 | T-capacitor feedback network architecture with CCPF.

in which multiple $(n+2)$ numbers of pseudoresistors are utilized. **Figure 6** shows two implementations of the CCPF connections (far and close connections) in which each pseudoresistor is implemented with a standard PMOS transistor. By knowing the fact that the CCPF provides a negative resistance $(-|R_N|)$, the equivalent input resistance of the OTA can be presented by

$$R_{ieq} = R_i \parallel (-|R_N|) = \frac{R_i |R_N|}{|R_N| - R_i} \quad (6)$$

As presented in Equation (6), to maximize R_{ieq} , $(|R_N| - R_i)$ must be minimized. In other words, to achieve a very high positive equivalent input resistance, the amount of $|R_N|$ must be slightly higher than R_i , and $(|R_N| - R_i)$ should approach zero. However, since this negative resistance is created by positive feedback, the stability of the amplifier limits the lower bound of $(|R_N| - R_i)$.

To verify Equation (6), we calculate the negative resistance of the CCPF. **Figure 7** shows the small signal equivalent circuit of the neural amplifier with a far CCPF connections. For simplicity of calculation, we assume all the pseudoresistors are identical and have the same value.

Performing a KVL in the loops DCBGHD and DCFGHD results in

$$i_3 = i_1 + 2i_2 \quad (7)$$

Also Performing KVL on the loops of ABCFEA and DCBGHD and considering (Equation 7) results in the following two equations

$$(n + 2)Ri_1 + nRi_2 = \Delta V \quad (8)$$

$$(n + 2)Ri_1 + (n + 4)Ri_2 = G_m R_o \Delta V \quad (9)$$

After solving these equations, the value of i_1 will be

$$i_1 = \frac{(n + 4) - G_m R_o n}{4(n + 2)R} \Delta V \quad (10)$$

As shown in **Figure 7**, $R_N = \frac{\Delta V}{i_1}$ is the equivalent resistance of the whole circuit connected to input terminals of the OTA (nodes A and E), which is parallel to R_{in} . By considering (Equation 10), R_N can be presented as

$$R_N = \frac{4(n + 2)R}{(n + 4) - G_m R_o n} \quad (11)$$

By knowing that the gain of the OTA ($G_m R_o$) is very high, the dominator of R_N is negative. In practice, the values of the pseudoresistors are not equal and vary based on their currents (or their voltages). Therefore, Equation (11) is not accurate and simulation results are required to calculate the exact value of R_N .

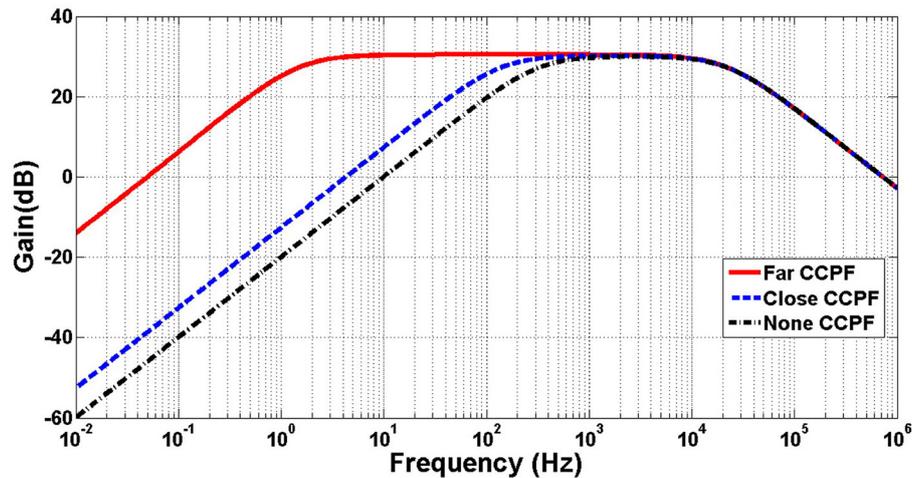


FIGURE 9 | Simulation of frequency response (gain) of the amplifier of Figure 8 with far, close and no CCPF connection.

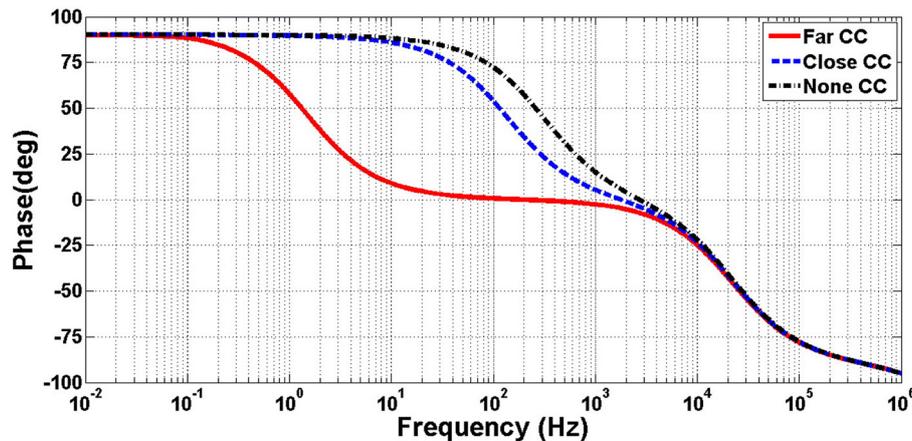


FIGURE 10 | Simulation of frequency response (phase) of the amplifier of Figure 8 with far, close and no CCPF connection.

The value of the low-cutoff frequency of the amplifier depends on the number and size (W/L) of the pseudoresistors as well as the position of the CCPF connections (far or close). For example, assuming $C_I = 10 \text{ pF}$, $C_F = 200 \text{ fF}$, $C_L = 1.7 \text{ pF}$, and $n = 4$ for a far CCPF connection in the amplifier shown in Figure 5 achieves a f_L of 0.27 Hz with the midband gain of 31.67 dB, while the total capacitance value of this amplifier is 22 pF. In order to decrease the total capacitance, we exploited a T-capacitor feedback network shown in Figure 8 (Ng and Xu, 2013). The pseudoresistors and CCPF connections in this figure are implemented similar to Figure 6 with 6 PMOS transistors.

The midband gain of the amplifier in Figure 8 is calculated as

$$A_M = \left(\frac{C_I}{C_{F1}} \right) \left(\frac{C_{F1} + C_{F2} + 2C_{F12}}{C_{F12}} \right) \quad (12)$$

We can adjust the capacitances in Equation (12) to keep the total capacitance of the OTA low while maintaining the same gain.

For example, in Figure 8, by choosing the value of the capacitors as $C_I = 1.4 \text{ pF}$, $C_{F1} = C_{F2} = 200 \text{ fF}$, $C_{F12} = 400 \text{ fF}$, and $C_L = 200 \text{ fF}$, the total capacitor value of the amplifier decreases to 4.2 pF, and the low-cutoff frequency increases from 0.27 to 1.5 Hz, which is still in the acceptable range.

Figures 9, 10 illustrates the frequency response of the amplifier in terms of gain and phase, respectively, and in far, close, and no CCPF connections. The amount of the low-cutoff frequency for far, close, and no CCPF connections are 1.5, 143, and 320 Hz, respectively.

The positive feedback in the CCPF architecture of the amplifier can result in instability. However, by carefully designing the number of pseudoresistors, transistor sizes, and the position of the CCPF connection we can make sure that the negative feedback is dominant and the whole architecture is stable and satisfies at least a 60 degree phase margin. Figure 11 shows the simulation of open loop frequency response of the amplifier of Figure 8 with 70 degree phase margin.

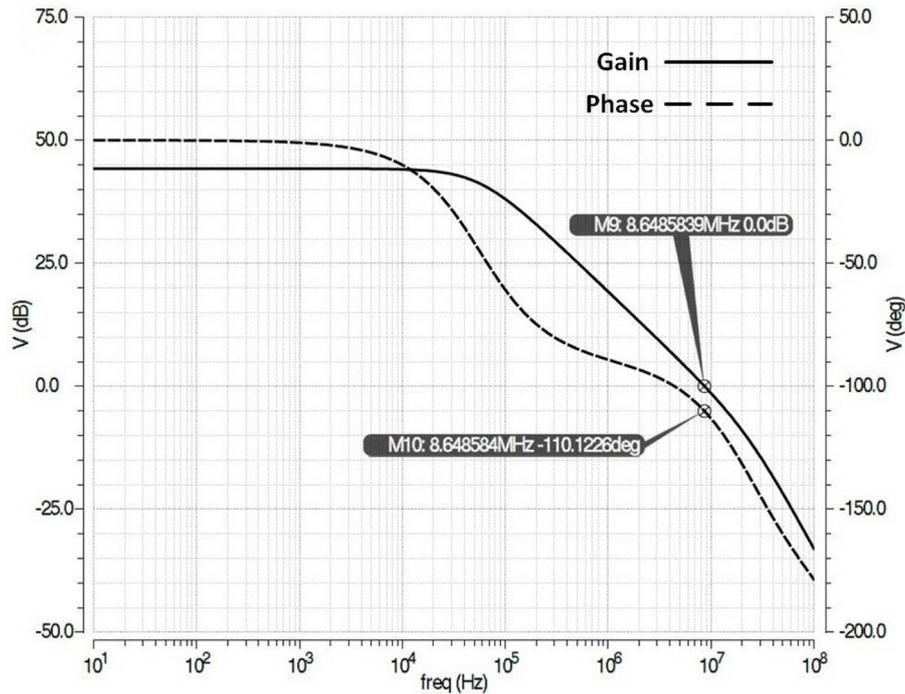


FIGURE 11 | Simulation of open loop frequency response (gain and phase) of the amplifier of Figure 8 with 70 degree phase margin.

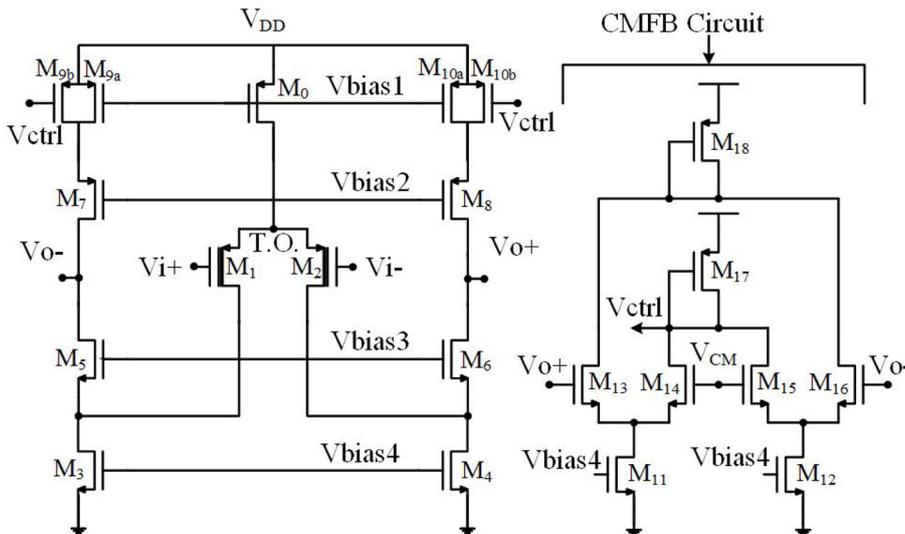


FIGURE 12 | Fully differential folded cascode OTA utilized in neural amplifier.

By adding switches to the CCPF connection we can program (i.e., turn on or off) the connections in the post-fabrication process. In case of multiple pseudoresistors (e.g., 18), the farther CCPF connections might observe instability due to process variation. Therefore, by programming the connections and choosing closer connections, we can avoid instability. In addition, programmability can also give us control over the value of f_L . The

closer connections have higher value of f_L and are more stable. On the other hand, the farther connections have lower value of f_L at the cost of less stability.

3.2. Thick Oxide Differential Pair

The second method to increase the input resistance of the OTA without increasing the feedback capacitance is to utilize

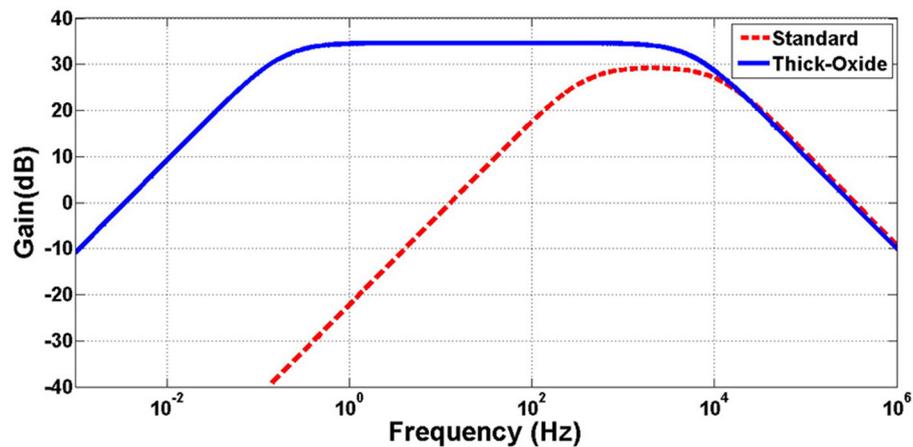


FIGURE 13 | Simulation of frequency response of neural amplifier with thick-oxide and standard PMOS differential pair.

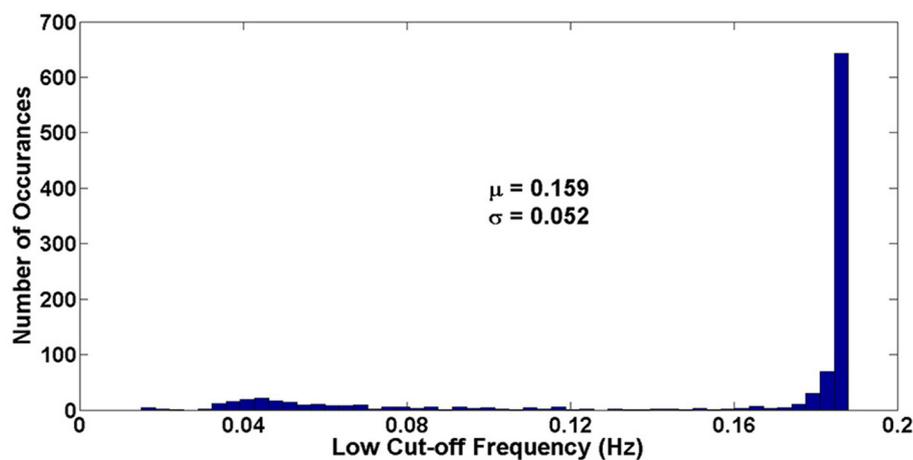


FIGURE 14 | Monte Carlo simulation of low-cutoff frequency of the neural amplifier.

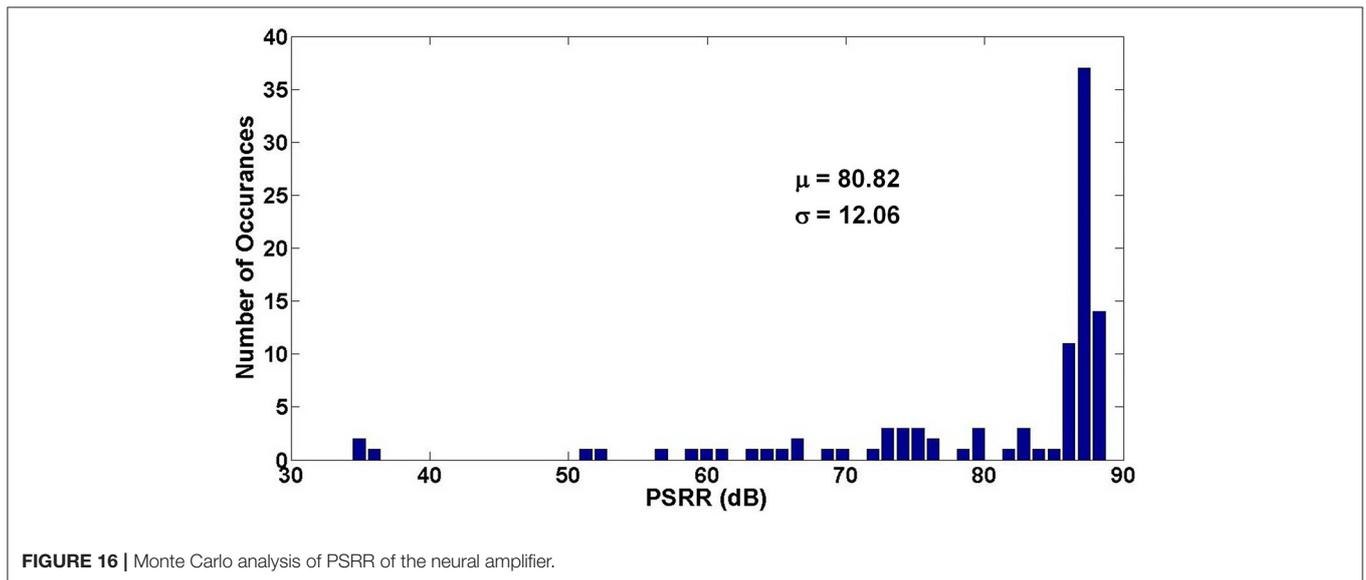
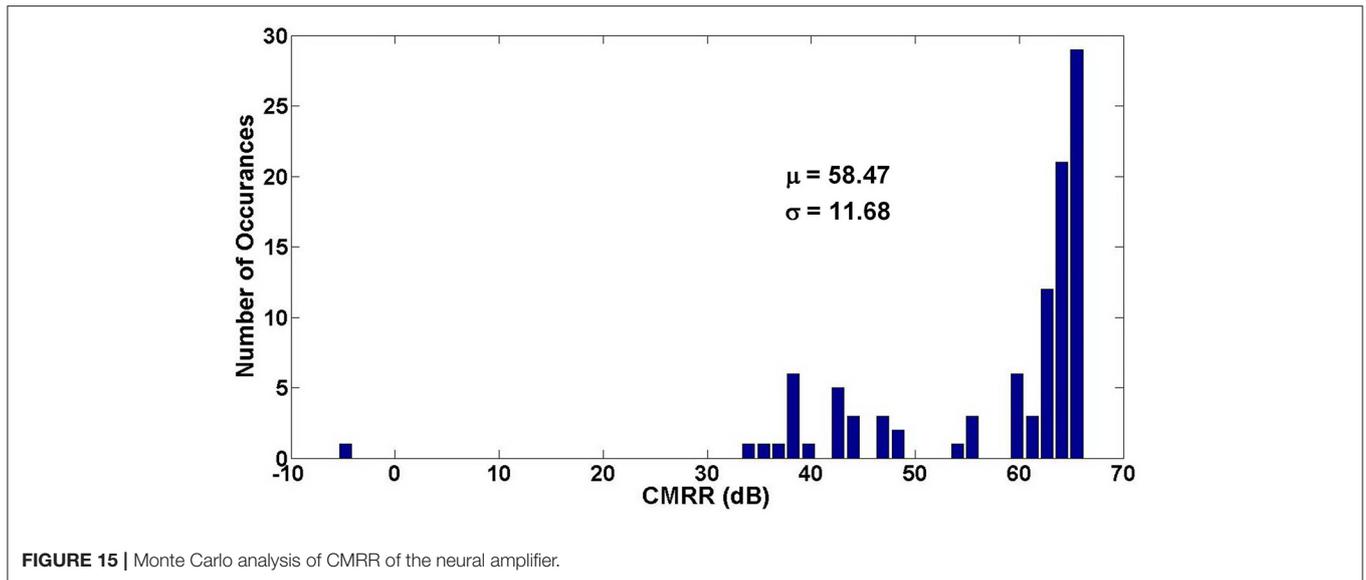
thick-oxide MOS transistors in the input differential pair. **Figure 12** shows the transistor level implementation of the OTA of **Figure 1** with thick-oxide PMOS input differential pair. In this figure, the bulks of NMOS transistors are grounded whereas the bulks of PMOS transistors are connected to their sources. The size of each transistor is shown in **Table 1** and the bias currents are tabulated in **Table 2**.

Figure 13 shows the simulation results of the designed neural amplifier utilizing the OTA of **Figure 12** and the OTA with standard PMOS input differential pair. The gain of the OTA and the whole neural amplifier are 68.2 and 34.6 dB, respectively. As shown in this figure, applying a thick-oxide PMOS in the input differential pair improved the low-cutoff frequency from 360 to 0.19 Hz. These simulation results confirm that increasing the input resistance of the OTA by utilizing thick-oxide PMOS in the differential pair decreases the low-cutoff frequency dramatically.

In order to increase the SNR of the neural amplifier, the first stage of a neural amplifier is designed as an LNA. To reduce the

flicker noise of the OTA of **Figure 12**, we optimize the size of the PMOS transistors in the input differential pair (i.e., M_1 and M_2). Also, as mentioned in Harrison and Charles (2003), to minimize the thermal noise, the transistors M_1 and M_2 are biased in the sub-threshold region to maximize their transconductance over drain current called transconductance efficiency (g_m/I_D), and the transistors M_3 , M_4 , M_{9a} , M_{9b} , M_{10a} , and M_{10b} are biased in the saturation region to minimize their g_m/I_D .

As mentioned earlier, the bandwidth and operating frequency of neural amplifiers are very low, therefore the dominant noise power is the flicker noise. Also, in the OTA of **Figure 12**, the differential pair transistors are the main source of the flicker noise in comparison with other transistors (Razavi, 2005). Therefore, to analyze the noise of the proposed neural amplifier, we only investigate the effect of the thick-oxide PMOS differential pair. Utilizing thick-oxide PMOS transistors in the differential pair of the OTA decreases the gate-oxide capacitance per unit area (C_{ox}) due to the increased gate oxide thickness (t_{ox}). Utilizing



the thick-oxide PMOS in the input differential pair increases the flicker noise power due to decreasing C_{ox} . The relation between the input-referred noise of the whole neural amplifier ($\overline{V_{ni,amp}^2}$) and the OTA input-referred noise ($\overline{V_{ni}^2}$) is presented as

$$\overline{V_{ni,amp}^2} = \left(\frac{C_I + C_F + C_{in}}{C_I} \right)^2 \cdot \overline{V_{ni}^2} \quad (13)$$

Decreasing the C_{ox} due to utilizing the thick-oxide PMOS differential pair, increases $\overline{V_{ni}^2}$ and decreases the C_{in} in Equation (13). Since the increase in $\overline{V_{ni}^2}$ is much higher than the reduction of its coefficient, the $\overline{V_{ni,amp}^2}$ increases by decreasing the C_{ox} . To compensate this drawback, we can increase the gain of the LNA

(C_I/C_F) by increasing C_I to reduce the $\overline{V_{ni,amp}^2}$ in Equation (13). Simulation results show that the minimum input-referred noise voltage of the neural amplifier is $5.9 \mu V_{rms}$ in the frequency range between 1 Hz and 5.6 kHz (bandwidth).

Note that to further reduce the noise of the OTA, it is required to apply noise reduction techniques such as the chopper stabilization technique, which is out of the scope of this paper.

Figure 14 shows the Monte Carlo simulation results ($N = 1,000$) of the low-cutoff frequency. As shown in this figure, the μ is equal to 0.159 Hz and the σ is equal to 0.052, resulting $\frac{3\sigma}{\mu}$ of 0.983.

Figures 15, 16 show the Monte Carlo analysis of CMRR and PSRR of the Neural amplifier. Applying thick-oxide MOS transistors in the input differential pair decreases the gate leakage current significantly and increases the input

impedance of the OTA and consequently the CMRR and PSRR improve.

4. MEASUREMENT AND *IN VITRO* RESULTS

4.1. Measured Performance

The prototype is implemented in the TSMC 65 nm CMOS process. The C_I and C_F are set to 11.5 pF and 208 fF, respectively, in the layout to achieve a gain of 55 V/V (or 34.3 dB) ($A_M = \frac{C_I}{C_F}$). The prototype uses 0.04 mm^2 ($270 \mu\text{m} \times 150 \mu\text{m}$) of silicon area. The micrograph of the die containing the amplifier is shown in **Figure 17**.

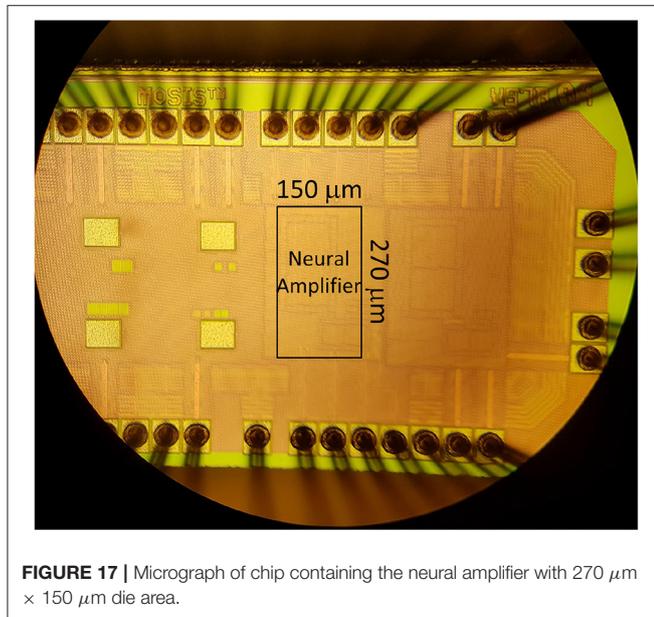


FIGURE 17 | Micrograph of chip containing the neural amplifier with $270 \mu\text{m} \times 150 \mu\text{m}$ die area.

The measured frequency response from 0.1 Hz to 1 MHz is performed through saline medium to mimic the brain environment as well as the simulation result are illustrated in **Figure 18**. The midband gain is 34.3 dB and the low and high-cutoff frequencies are 2 Hz and 5.6 kHz, respectively. The simulated low-cutoff frequency is 0.19 Hz which is less than that achieved in the measurement result. This deviation is expected as the MOS pseudoresistors are nonlinear and significantly sensitive to their operating point (Harrison and Charles, 2003).

Figure 19 shows the measured input-referred noise voltage spectral density of the neural amplifier. The RMS value of the input referred noise is achieved as $6.1 \mu\text{V}_{\text{rms}}$ by integrating the area under the curve from 1 Hz to 5.6 kHz (amplifier bandwidth) in **Figure 19**. This value is slightly higher than the simulated result ($5.9 \mu\text{V}_{\text{rms}}$).

Table 3 shows a summary of the simulated and measured parameters of the prototype. A comparison of our work and the other published works is presented in **Table 4**. All of the chosen neural amplifiers are AC-coupled. To fairly compare these amplifiers with different gain values, number of stages and technology, we only consider the first stage of each amplifiers.

Measurement results show that the achieved gain is the highest among all in **Table 4**. Note that the gain for Xiao et al. (2010) is reported for two stages. Also, the area of the fabricated chip is less than others. However, we should note that comparing the chip area itself without considering the midband gain is not a fair comparison. The midband gain (A_m) of the amplifier is equal to $\frac{C_I}{C_F}$. The low-cutoff frequency (f_L) is determined by C_F , and C_I is determined by the gain and C_F . Also, note that the main contributor to the chip area is C_I . In other words, for a normalized gain, lower C_F results in less chip area. Therefore, comparing C_F is a better figure of merit for comparing the chip area while the amplifiers have different gains. In this case, the values of C_F of the proposed amplifier and Ng and Xu (2016) are 208 fF and 350 fF, respectively. Note that the gain reported in our work is 34.3 dB, while the gain in Ng and Xu (2016) is 26.4 dB.

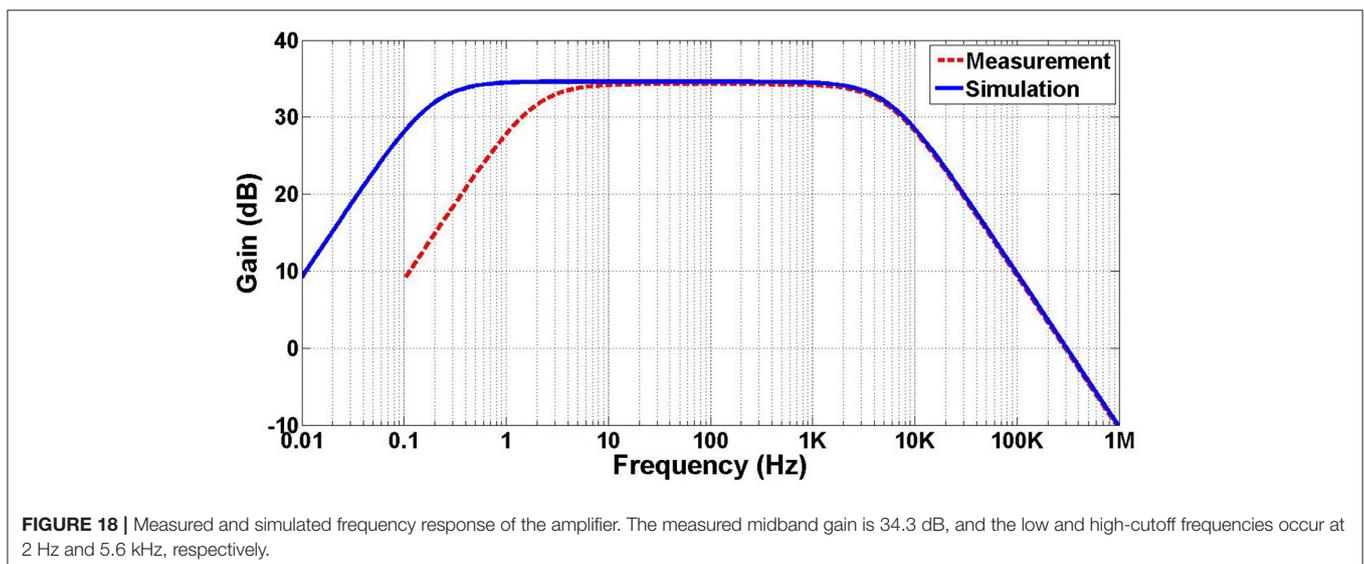


FIGURE 18 | Measured and simulated frequency response of the amplifier. The measured midband gain is 34.3 dB, and the low and high-cutoff frequencies occur at 2 Hz and 5.6 kHz, respectively.

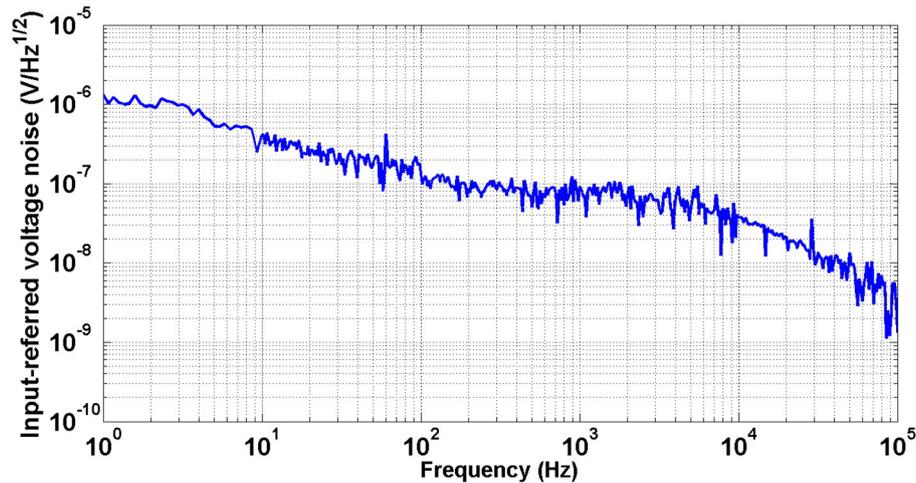


FIGURE 19 | Measured input-referred noise voltage spectrum.

TABLE 1 | Transistor sizes of the neural amplifier.

Transistor	$W/L(\mu m)$	Transistor	$W/L(\mu m)$	Transistor	$W/L(\mu m)$
M_0	$5 \frac{4}{10}$	M_5	$2 \frac{0.8}{2}$	M_{9b}	$4 \frac{1}{20}$
M_1	$24 \frac{4}{4}$	M_6	$2 \frac{0.8}{2}$	M_{10a}	$4 \frac{1}{20}$
M_2	$24 \frac{4}{4}$	M_7	$2 \frac{0.8}{2}$	M_{10b}	$4 \frac{1}{20}$
M_3	$3 \frac{1}{20}$	M_8	$2 \frac{0.8}{2}$	M_{11}	$2 \frac{0.5}{20}$
M_4	$3 \frac{1}{20}$	M_{9a}	$4 \frac{1}{20}$	M_{12}	$2 \frac{0.5}{20}$
M_{13}	$1 \frac{1}{1}$	M_{14}	$1 \frac{1}{1}$	M_{15}	$1 \frac{1}{1}$
M_{16}	$1 \frac{1}{1}$	M_{17}	$4 \frac{1}{20}$	M_{18}	$4 \frac{1}{20}$

TABLE 2 | Bias currents of the neural amplifier.

I_{M0}	$I_{M3,4}$	$I_{M9a,10a}$	$I_{M11,12}$
$1.83 \mu A$	$1.276 \mu A$	$175 nA$	$390 nA$

This is why the total area of our work is almost the same as that of Ng and Xu (2016).

The amplifier of Song et al. (2013) has been implemented in the $0.18 \mu m$ technology with a gain of 26 dB. Its high pass pole is 80 Hz. The value of C_F is not reported, however, the total area of the amplifier is $0.16 mm^2$ which is significantly large. In Abdelhalim et al. (2013), neural amplifiers with a gain of 54–60 dB in two gain stages have been implemented in the $0.13 \mu m$ process. The first stage (LNA) with the estimated gain of 31.8 dB has 300 fF feedback capacitors with 0.1 Hz low-cutoff frequency. Our analysis shows that the C_F in Abdelhalim et al. (2013) could be reduced to 200 fF if the thick-oxide differential pair is used.

The neural amplifier of Xiao et al. (2010) has employed two gain stages to obtain 49 dB in the $0.13 \mu m$ process. The value of the C_F is not reported. However, the estimated amplifier area and f_L are $0.4 mm^2$ and 100 Hz, respectively. This amplifier occupies a very large area and has a high low-cutoff frequency. The designs

TABLE 3 | Experimental and simulation characteristics of neural amplifier.

Parameter	Simulation	Measured
Supply voltage [V]	1	1
Supply current [μA]	3.63	3.63
Gain [dB]	34.6	34.3
Band width [kHz]	5.8	5.6
Low-cutoff frequency [Hz]	0.19	2
Input-Referred Noise [μV_{rms}]	5.9	6.1
Noise efficiency factor	5.8	6.1
THD (2 mV_{pp} at 1 kHz) [%]	0.18	< 1

in Biederman et al. (2015) utilize LNA with a gain of 26 dB fabricated in the 65 nm CMOS Technology. It employs a 500 fF feedback capacitor parallel to a pseudoresistor in a conventional CFN architecture similar to our work. The low-cutoff frequency f_L is adjustable, with the minimum value of 10 Hz. The neural amplifier consists of a variable gain amplifier (VGA) and buffer to achieve a gain of 45–60 dB. The amplifier in Ng and Xu (2016) has been implemented with two gain stages with 52.1 dB midband gain in the 65 nm technology. The gain in the first stage, LNA, is 26.4 dB and the f_L is reported as 1 Hz. The LNA exploits a CMOS-inverter-based OTA with 360 fF as C_F . The amplifier designed in Kim and Ko (2019) utilizes relatively small transistors in the OTA. In addition to small transistors, an older process of $0.18 \mu m$ is used which they both help decreasing the gate leakage and increase the input resistance of the OTA. This results in a low f_L of 6.4 Hz. However, this comes at the cost of high input-referred noise voltage ($10.68 \mu V_{rms}$). CMRR and PSRR in the typical corner simulation are 66.3 and 88 dB, respectively. As mentioned earlier, when thick-oxide CMOS is used, the CMRR and PSRR increase compared to the case when standard CMOS is used. This increase is due to the increased input impedance

TABLE 4 | Comparison of fully integrated neural amplifiers.

Parameter	Song et al. (2013)	Abdelhalim et al. (2013)	Xiao et al. (2010)	Biederman et al. (2015)	Ng and Xu (2016)	Kim and Ko (2019)	This work
Technology [CMOS]	0.18 μm	0.13 μm	0.13 μm	65 nm	65 nm	0.18 μm	65 nm
Area [mm^2]	0.16	N/A	0.4*	N/A	0.042	N/A	0.04
Supply [V]	1.2	1.2	0.8	1	1	0.6	1
Power consumption [μW]	0.43	4.5	0.64	1.2	3.28	0.27	3.63
Gain [dB]	26	31.8	49**	26	26.4	14-28***	34.3
BW [Hz]	80-15k	0.1-5k	100* - 6.2k	10-8k	1-8.2k	6.4-4.46k	2-5.6k
C_F [fF]	N/A	300	N/A	500	350	100	208
Input-referred noise [μV_{rms}]	8.1	6.5	14	7.5	4.13	10.68	6.1
Noise BW [Hz]	80-15k	10-5k	100* - 6.2k	100-10k	1-8.2k	1-10k	1-5.6k
NEF	1.52	7.2	6.5	3.6	3.19	1.79***	6.1
CMRR [dB]	>60	75	59	N/A	>90 @100Hz	61.3	66.3****
PSRR [dB]	>80	N/A	71	N/A	78 @1kHz	77.2	88****
THD	0.05% @10 mV_{pp}	-51dB @1KHz 0.7 V_{opp}	@1 mV_{pp} < 0.4%	N/A	1% 0.7 mV_p	0.5% @ 200 mV_{opp}	< 1% @1KHz 2 mV_{pp}

*Estimated. **This gain is reported for two stages. All other gains are reported for the first stage. ***Single CCIA. ****Simulation result.

of the OTA. Also, because of less short channel effects in thick-oxide MOS transistors, the linearity and THD of the amplifier are improved.

4.2. *In vitro* Neural Recording

We used this neural amplifier for neural recordings in an *in vitro* experiment on the slices of a mouse brain at the faculty of Dentistry at University of Montreal. A micropipette is used to capture the electrical activity of the brain. The micropipette is filled with NaCl (0.5 mol) without bubbles. This micropipette contains a metal electrode of AgCl which records the extracellular APs of the brainstem of the mouse brain slice. The brain slice is inserted and fixed in a chamber which contains artificial cerebrospinal fluid (ACSF) which is continuously oxygenated and kept humid to mimic a real brain environment and to keep the neurons alive for a few hours. The micropipette is gradually penetrated into the brainstem tissue by means of a microscope and its peripheral tools.

To complete the test setup, the AgCl electrode of the micropipette is connected to the non-inverting input of the prototype amplifier. The connection of the chamber, including the ACSF, is connected to the inverting port of the amplifier as a V_{ref} . It should be noted that shielded wires are utilized to perform these connections. A commercial setup of a neural recording system containing an instrumentation amplifier (A-M systems, Inc.), rack mounted data acquisition equipment and a PC with a spike2 Windows-based software (version 5.19, Cambridge Electronic design) was utilized. The output of the proposed amplifier is connected to the commercial amplifier. The commercial amplifier is a band pass amplifier with a midband gain of 100 (V/V) and with low and high cutoff frequencies of 300 Hz and 5 kHz, respectively. Setting the low-cutoff frequency at 300 Hz allows us to eliminate the LFP and extract the extra

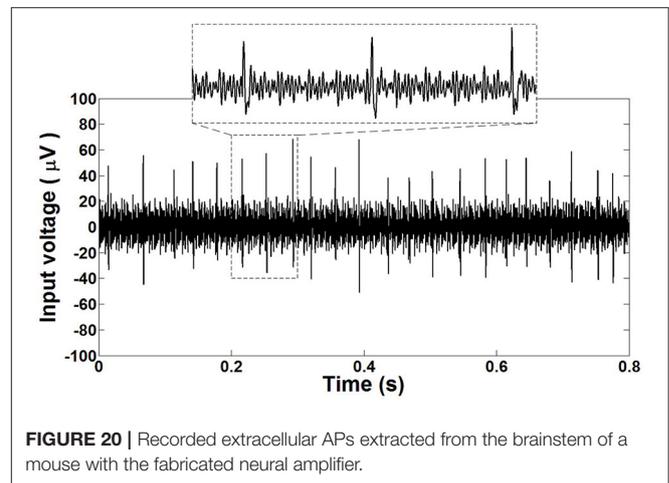


FIGURE 20 | Recorded extracellular APs extracted from the brainstem of a mouse with the fabricated neural amplifier.

cellular APs from the output signal. By using the commercial amplifier as the second stage amplifier, the total gain is achieved at 5,300 V/V. During the test procedure, the amplified signal is sampled with a frequency of 10 kS/s and digitized by the mentioned data acquisition equipment and transferred to the PC. Spike2 was used to observe the captured data in the PC. **Figure 20** illustrates the recorded spontaneous extra cellular APs from the brainstem of the mouse with the proposed neural amplifier.

5. CONCLUSION

Scaling down technology introduces new challenges in neural amplifier design. One main challenge is the increased low-cutoff frequency (f_L) of the AC-coupled amplifiers, assuming the same feedback capacitance value is used. The simplest

solution is to increase the feedback capacitors. However, this comes at the cost of increased input capacitors for the same gain of the amplifier, which increases the silicon area and decreases the input impedance of the amplifier. Assuming a neural recording implant requires a large array of these amplifiers, the total consumption of the silicon area increases dramatically.

In this paper, we focus on this challenge, find its roots, and propose solutions to improve it. Scaling down the technology increases the leakage current of the differential pair of the OTA due to decreasing the gate oxide thickness (short channel effects). This is translated to decreasing the input resistance (R_i) of OTA. We show, through simulations backed by an analytical analysis, that decreasing R_i is the fundamental reason for the increase in f_L . Two different solutions are presented in this paper to increase R_i : applying a cross-coupled positive feedback architecture and utilizing thick-oxide PMOS transistors in a differential pair of the

OTA. The simulations confirm that both of the solutions decrease the f_L . We designed and fabricated the latter solution in the 65 nm TSMC process. The experimental results show that the low-cutoff frequency decreases to 2 Hz with 208 fF feedback capacitor (C_F). The neural amplifier is verified by *in vitro* experiment on mouse brainstem slices.

DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author/s.

AUTHOR CONTRIBUTIONS

All authors listed have made a substantial, direct and intellectual contribution to the work, and approved it for publication.

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Conflict of Interest: The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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