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Self-Rectified Graphite-Based Reprogrammable One-Time Programmable (RS-OTP) Memory for Embedded Applications

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A graphite-based RRAM device with a self-rectifying characteristic named "non-linearity (NL)" is developed for a high-density crossbar array for in-memory computing with low power and high scalability. Meanwhile, the reprogrammable functions are presented in self-selected RRAM as a promising candidate for one-time programmable (OTP) in the emerging memory-embedded applications such as security, system-on-chip (SoC), and Internet of Things (IoT).

Keywords: selectorless, OTP, fuse, resistive random-access memory, self-rectify

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INTRODUCTION

In the era of computational and information technologies renovation such as artificial intelligence (AI), Internet of Things (IoT), edge computing, and in-memory computing paradigm, the emerging memory technology with high-density storage, large bandwidth, and low power consumption has been rapidly developed over decades. With the simple crossbar structure featuring $4F^2$ of footprint, resistive random-access memory (RRAM) is a promising candidate for next-generation non-volatile memory technologies for both data storage and in-memory computing, owing to its ultra-low power consumption, simple structure, and high scalability (Park et al., 2013; Liu et al., 2016; Huang and Lee, 2017; Moon et al., 2018). Despite the simple structure of RRAM being beneficial for the high-density memory application, sneak-path currents (SPCs) in the crossbar array resulting in crosstalk have attracted considerable attention. The interference currents from neighboring cells caused the read error and false programming and are usually resolved by integration of a selection device, for example, transistor, diode, and selector, called "1T-1R" or "1S-1R" configurations (Sungho Kim et al., 2014; Sharma et al., 2015; Lim et al., 2016; Chen et al., 2017). However, this approach leads to high cost, fabrication complexity, energy overhead, and hindered scalability. Consequently, accessing a selected memory cell in the cross-point array with interference robustness and SPC immunity is the major challenge for high-density memory arrays (Sungho Kim et al., 2014; Lim et al., 2016; Doi et al., 2018). In other words, self-rectified memory is beneficial for future high-density storage and in-memory computing applications.

On the other hand, one-time programmable (OTP) memory enables the chip unit identification and circuit unit adaptation, and repair for cache (Chen et al., 2021). The OTP memory has become promising for embedded memory applications for its cost-effectiveness, feasibility for integration, and data retention. However, data can only be written once and cannot be revised, in which the users compromised with the risk of miss-programming. Polysilicon is utilized as the fuse element in prior CMOS technologies before utilizing the high-k metal gate in the front-end technology (Chen et al., 2017; Cheng et al., 2018; Doi et al., 2020; Chen et al., 2021). With high demands on computing configurations, the logic process-compatible non-volatile OTP utilizing the resistive memory is

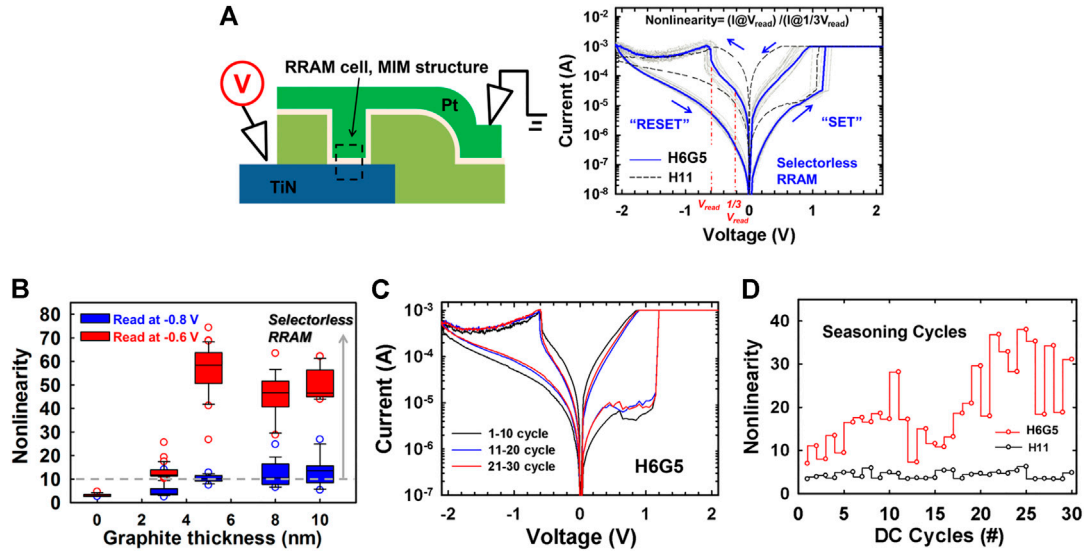

FIGURE 1 | (A) Device structure and I-V characteristics for selectorless RRAM with V/3 read scheme, **(B)** non-linearity as a function of graphite thickness (0, 3, 5, 8, and 10 nm), **(C)** seasoning cycles for a pristine device, **(D)** non-linearity as a function of seasoning cycles for as-fabricated devices (i.e., H6G5 and H11).

critical for recent applications, namely, security for data storage, security, Internet of Things, and modern system-on-chip (Kulkarni et al., 2021; Liu et al., 2018; Okuno et al., 2020; Shamsoshoara et al., 2020; Yang et al., 2020). This results in challenges, such as, increase in the fuse bit counts, overall area, large power consumption, and reliability. In this work, self-rectified graphite-based reprogrammable one-time programmable (RS-OTP) memory is presented for high-performance computing and embedded applications.

RESULTS AND DISCUSSION

Device Fabrication

The RRAM devices with a varied feature size of 400 nm, 600 nm, 800 nm, and 1 μm have been fabricated. With starting substrates of heavily doped N + Si wafers, titanium nitride (TiN) of 200 nm was deposited as the bottom electrode (BE). Then 3, 5, 8, and 10 nm of graphite, followed by 6 nm of HfO_x, were deposited as resistive switching dielectric layers for bilayer structures by radio frequency (RF) sputtering. Platinum of 165 nm was then deposited as top electrodes, followed by the lift-off process for RRAM devices. The HfO_x (11 nm) single-layer, SiO_x (6 nm)/graphite (5 nm), and HfO_x (4 nm)/SiO_x (9 nm) bilayer devices are fabricated, as in **Figure 1A**. The RRAM cell is filled in the SiO_x isolation via, which formed by SiO_x encapsulation (100 nm). Platinum is grounded while applying the voltage at TiN as the bottom electrode. The transmission electron microscopy (TEM) image of the H6G5 stacked device was analyzed in our previous work, and the graphite is examined in the crystallographic plane of (211) by X-ray diffraction (XRD) and energy dispersive X-ray spectrum (EDX) line scan results (Ki Hong et al., 2011; Chen et al., 2018a). The abbreviations for a single-layer (e.g., H11) and bilayer device structures (e.g., H6G3, H6G5, H6G8, H6G10, and H4S9) are used to simplify the notations. An Agilent B1500 and a Lakeshore probe station were used for electrical characterization of the RRAM devices.

RESULTS AND DISCUSSION

The sneak path current is the inevitable issue in the crossbar memory array while implementing high-density storage and new computing applications, for example, in-memory computing. Crosstalk occurs and the read accuracy is deteriorated by the SPC, which is mainly due to the neighboring cells. The self-rectifying behaviors, called "non-linearity (NL)," were presented in bilayer stacked RRAM to mitigate the read margin degradation, attributing to its built-in non-linear nature which suppresses the sneak path currents in the array. Note that the non-linearity (NL) is defined as the current at reading voltage divided by a current at 1/3 read voltage in this work, that is, V/3 read scheme (**Figure 1A**). The built-in NL shows both positive and negative polarities, which improves the design feasibility better than the unipolar selection devices. Like the conventional oxide-based RRAM, the electroforming process is conducted with the voltage of ~3 V and a compliance current limit (CCL) of 1 mA to form the conductive filament for a low resistance state (LRS). Then, the RESET process with negative polarity voltage sweeping was followed to rupture the conductive filament for a high resistance state (HRS). The SET process with positive polarity voltage sweeping was applied to reconnect the conductive filament for LRS. **Figure 1A** shows 30 cycles of the SET/RESET process (gray curves) in a self-rectified RRAM (H6G5) and the median of the I-V curves (blue). As a comparison, the I-V curve of the single-layer HfOx (11 nm) (H11) with no NL behavior is shown (**Figure 1A**, dash lines). **Figure 1B** shows non-linearity as a function of graphite thickness with varied read

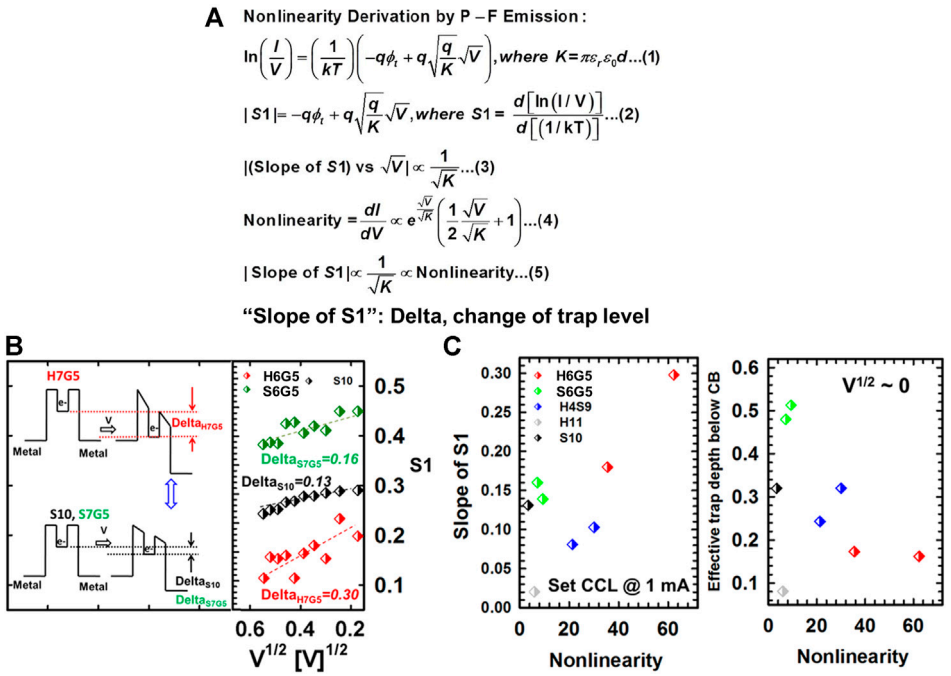

FIGURE 2 | (A) Summary of internal filament gap design by Poole–Frenkel formula in (Park et al., 2013) DC response, where B is a constant, q is the elementary charge, φt is the energy barrier that must be overcome by the electron, ε_r is the relative permittivity of the RS medium, d is dielectric thickness, k is the Boltzmann constant, and T is temperature. Huang and Lee (2017); Liu et al. (2016) derived the procedure from Poole–Frenkel formula (Moon et al., 2018). Non-linearity definition and derivate procedure (Sharma et al., 2015). The relationship between Poole–Frenkel carrier transport and non-linearity, **(B)** band diagram of the trap fluctuation under low (e.g., 0.28 V), and high voltage (e.g., 0.8 V) with the slope of S1 current fitting results in H6G5, S6G5, and H11, **(C)** slope of S1 **(left)** and trap depth **(right)** as a function of non-linearity in five device structures (SET CCL at 1 mA).

voltage (V_{read} = −0.6 V and −0.8 V) on 10 devices for each thickness condition. The higher read voltage induced read stress, leading to non-linearity degradation, which is discussed in the previous work (Lim et al., 2016). The NL increases with increasing graphite thickness from NL = 10 (graphite layer = 3 nm) to NL = 60 (graphite layer = 5 nm). However, the NL remains at ~ 60 for the devices with a graphite thickness of 5, 8, and 10 nm, which is suggested as the identical thickness of graphite oxide formation at the interface of HfO_x and BE (~3 nm) that acts as the low-k layer for the microstructure design of selectorless RRAM (Chen et al., 2018a). This depicts that the deposition thickness of graphite is required more than 3 nm for realizing the graphite-based self-rectified RRAM with an NL of ~60. The oxide-based bilayer stacked RRAM is presented to offer immunity toward sneak path currents in high-density memory integrations when implementing the future high-density storage and in-memory computing applications.

After the electroforming process, the conductive filament, that is, the percolation path, is formed in the as-deposited oxide thin film. The "seasoning cycling" is required in some bilayer systems to locate the switching gap and to stabilize the NL behaviors (Chen et al., 2018a; Chen et al., 2019a; Chen et al., 2019b). **Figure 1C** shows the three median I-V curves on H6G5 for cycles 1 to 10, 11 to 20, and 20 to 30, respectively. Generally, the LRS current in the first several cycles after electroforming is relatively higher than that in the following cycles due to the instability of the switching location and discussed (Chen et al., 2019a). As compared to the yield of efficient seasoning in self-rectified RRAMs using HfO_x/SiO_x stacks, the yield of efficient seasoning is improved in the graphite-based self-rectified RRAMs (~6%). **Figure 1D** shows the comparison of seasoning cycles on single-layer SiO_x and graphite-based stacked self-rectified devices.

The contribution of the low-k layer in stacked engineering with the gap modulation method (i.e., SET CCL) has been fully discussed in our previous work, such as, providing a low-k region to gain a high non-linearity based on the relation of NL and 1/[k]$^{0.5}$. However, the physical mechanism modeling of the bilayer structure utilized for improving non-linearity is still lacking investigation, for example, how will the thin film with a higher dielectric constant improve the non-linearity. Herein, the contribution of the high-k layer to the stacking engineering selectorless RRAMs can be investigated by the numerical current fitting, such as, the high-k/low-k structures (e.g., H6G5 and H4S9), low-k/low-k structure (e.g., S6G5), and single layer (e.g., S10), are gained with low-temperature testing and the current fitting procedure (Chen et al., 2018b). **Figure 2C**) shows the "slope of S1 (S1′, delta)" as a function of [V]$^{0.5}$, where S1′ is proportional to non-linearity (eq. 2). In other words, higher S1′ indicates the larger trap depth differences when voltage is applied, which results in higher non-linearity and preferred self-selective behaviors in selectorless RRAMs. The schematic of band

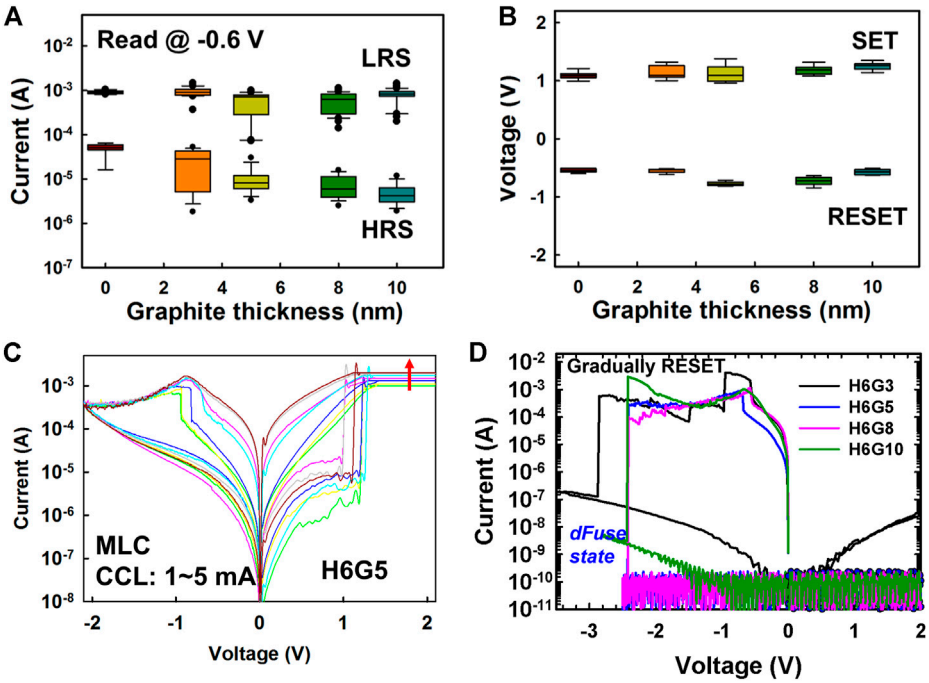

FIGURE 3 | (A) Low resistance state (LRS) and high resistance state (HRS) for various graphite thickness, **(B)** SET and RESET voltage for various graphite thickness, **(C)** I-V characteristics with SET CCL modulations on H6G5, **(D)** dielectric fuse state for varied graphite thickness.

diagrams is shown in **Figure 2** (c, left), which indicates the trap fluctuation (i.e., delta) before and after applying the voltages. **Figure 2** (c, left) shows S1 as a function of $[V]^{0.5}$ for H7G5, S7G5, and S10 devices. A stronger trap fluctuation is observed in H6G5 (delta~0.30) than in S10 (delta ~0.13) and in H6G5 (delta~0.16), which explains higher non-linearity with high-k material integration. Furthermore, the effective trap depth under the conduction band (CB) is extrapolated as voltage approach 0. The results show that shallower trap depth is observed in H6G5 than in S6G5, which results in higher NL (**Figure 2D**, right). According to the investigation of trap depth on various device structures, the device integrated with high-k materials, that is, H4S9 (blue) and H7G5 (red), shows the higher NL which is elevating the current at a full-read voltage (V_{read}) in **Figure 1A**. Shallower barrier height leads to the elevated current as the high electric field is applied, that is, V_{read}, while still maintaining a lower current at the 1/3 V_{read} for unselected cells due to the sufficient trap barriers of the bilayer dielectric thin film. The energy barrier height is shown in **Figure 2C** left panel. Note that the SET CCL at 1 mA is applied, suggesting the switching gap is firmly stabilized in the low-k layer, and the non-linearity is optimized. The non-linearity is observed to be proportional to the slope of S1 and to trap depth according to S1′ extraction of the five device structures. The high-k/low-k stacked devices, namely, H6G5 and H4S9 demonstrated higher non-linearity than S10, H11, and S6G5, which depicts the high-k materials, for example, HfO_x is desired to be integrated with the bilayer structure to obtain high non-linear nature and to realize the selectorless RRAM application.

Electric field increases and I_{Vread} increases as effective oxide thickness (EOT) decreases. Effective oxide thickness was calculated and compared between devices. The high-k integrated device, that is, H6G5, has a smaller EOT (~1.24 nm) than S6G5 (~6 nm) and higher band bending under the same applied voltage. In addition, the oxygen affinity of HfO_x is larger than that of SiO_x, that is, oxygen concentration is higher in HfO_x, which relates to the Gibbs free energy of HfO_x (ΔG^0 ~ − 266, 435) and SiOx (ΔG^0 ~ − 215,600) under the same atmospheric conditions with the spontaneous oxidation process. The high-k materials, as an oxygen exchange layer, have higher oxygen vacancy concentrations (Vo^+) than low-k materials, which leads to higher I_{Vread} and NL. It is thought to suggest that the high-k layer integration is desired in the bilayer engineering for improving the NL, especially for higher $I_{\text{at Vread}}$, as compared to the single low-k layer and low-k/low-k stacked devices.

Figure 3A,B shows the memory window and switching voltages as a function of graphite thickness, that is, 0, 3, 5, 8, and 10 nm with the identical thickness of HfO_x (6 nm) in the stacked devices. The 30 devices of each graphite thickness were measured here for device-to-device (D2D) variation. As shown in **Figure 3**A, the memory window increased with the increasing graphite thickness, where the higher HRS current reduced ~10X with thicker graphite, which is attributed to the improved thermal conductivity, that is, efficient joule heating in the RESET process. Meanwhile, the SET/RESET voltages are independent of the graphite thickness, which depicts the insulator layer that determines the switching voltages, that is, the high-k layer, as discussed in **Figure 2**. According to the

high demands of computing and data storage, the multilevel cell applications in emerging memory become beneficial for brain-inspired computing, where the memory component is utilized as mimicking the synapses and neurons for the new computational architecture. Herein, the self-rectified memory is demonstrated with the multilevel states under the SET compliance current limit (CCL) modulation from 1 to 5 mA. Both the HRS and LRS are modulated by elevating the CCL. Note that the self-rectifying characteristic is optimized with the CCL of 1–3 mA and was compromised for high-memory window under higher CCL (3–5 mA).

In addition, multi-programmable OTP is developed in this work based on the dielectric fuse breakdown (called "dFuse") with the varied thickness of graphite (**Figure 3D**). The self-rectifying operational regime (i.e., RESET at −2.1 V in **Figure 1A**) enables users to recompile and revise data before storing information permanently. This shows the feature rewritable for the user before the final write state. While the write voltage of dFuse is applied (i.e., −2 to −3 V), the dielectric breakdown occurs and completes the fuse state at the lowest current level of ~0.1 nA and cannot recover again. It is suggested that the dielectric breakdown occurs in HfOx thin-film breakdown as the electric field enhancement with the graphite layer acts as the interfacial conductive layer between the dielectric and bottom electrodes. Meanwhile, the thermal conductivity of graphite is 1,950 W/m-K (Jang et al., 2010), which is a good thermal sink for good reliability properties on the conductive filaments. The thicker graphite, for example, 5, 8, and 10 nm thickness, provides a superior thermal conduction path for the dielectric fuse breakdown, that is, "dFuse state," with reducing voltage for lower power consumption. It is worthy to note that the devices performed as the self-rectifying RRAM with gradually RESET behaviors before dFuse voltage was applied, which is favorable for the multilevel application before the permanent program step.

CONCLUSION

In summary, the graphite-based RRAM devices with a self-rectifying characteristic, that is, non-linearity have been presented and demonstrated with MLC application as well as the dFuse state, which enables an OTP with the reprogrammable data storage before the permanent written-in process. The self-rectified RRAMs were proposed for the embedded integrated application according to its CMOS compatibility, low power consumption, excellent scalability for future emerging memory, and computing applications.

DATA AVAILABILITY STATEMENT

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

AUTHOR CONTRIBUTIONS

Y-CC outlined the concepts, discussed the sections, researched the literature for this review article, and wrote the text of the article.

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Conflict of Interest: The author declares that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.