Engineering Tunneling Selector to Achieve High Non-linearity for 1S1R Integration

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Memristor devices have been extensively studied as one of the most promising technologies for next-generation non-volatile memory. However, for the memristor devices to have a real technological impact, they must be densely packed in a large crossbar array (CBA) exceeding Gigabytes in size. Devising a selector device that is CMOS compatible, 3D stackable, and has a high non-linearity (NL) and great endurance is a crucial enabling ingredient to reach this goal. Tunneling based selectors are very promising in these aspects, but the mediocre NL value limits their applications in large passive crossbar arrays. In this work, we demonstrated a trilayer tunneling selector based on the Ge/Pt/TaN$_{1+x}$/Ta$_2$O$_5$/TaN$_{1+x}$/Pd layers that could achieve a NL of 3×10^5, which is the highest NL achieved using a tunnel selector so far. The record-high tunneling NL is partially attributed to the bottom electrode's ultra-smoothness (BE) induced by a Ge/Pt layer. We further demonstrated the feasibility of 1S1R (1-selector 1-resistor) integration by vertically integrating a Pd/Ta$_2$O$_5$/Ru based memristor on top of the proposed selector.

Keywords: selectors, high non-linearity, vertically integrated 1S1R, crossbar arrays, memristor

INTRODUCTION

Originally CBA was proposed and adapted for telecommunication switching systems at the beginning of the twentieth century (Craft, 1925). A relay switch was placed at each crosspoint to automatically and efficiently route any permutation of its n input (e.g., rows) to its m output lines (e.g., column; Scudder and Reynolds, 1939). Given the CBA architecture's simplicity and extremely high-density capability, it has recently been adapted for memory applications (Kuekes et al., 2000; Kuekes and Williams, 2001; Chen et al., 2003). A memristor (also called ReRAM, resistive random access memory, when used for memory) has a simple two-terminal structure, which is highly desirable for CBA implementation (Xia and Yang, 2019). CBA makes it possible to achieve a device footprint of 4F^2. An even higher memory density (4F^2/n; n: number of the stacked-layer) is achievable by 3D stacking the memristor devices (Lin et al., 2020). In light of these advantages, memristor-based CBA has emerged as one of the most promising technologies for high-density storage (Baek et al., 2005; Lee et al., 2009; Liu et al., 2014; Sills et al., 2014; Hudec et al., 2016) as well as memory-centric computing (Mouttet, 2008; Upadhyay et al., 2016, 2019; Rao et al., 2019; Lin et al., 2020; Wang et al., 2020). Memristor based CBAs can be used for solving

linear regression, logistic regression, linear equations, matrix eigenvectors, differential equations, neural networks, etc. in one computing cycle in principle, *in-situ* within the CBA by using physical law such as Ohm's law for multiplication and Kirchhoff's law for summation (Rao et al., 2019; Sun et al., 2019, 2020; Wang et al., 2020). CBAs enable a time-saving and energy-efficient approach to solving a wide range of practical problems in the era of big data nowadays.

On the other hand, a CBA suffers from the so-called sneak path current issue (Yang et al., 2013; Xia and Yang, 2019). Sneak path current could be suppressed if we can somehow make the current-voltage relation of the "ON" state of memristor non-linear (Joshua Yang et al., 2012). This could be achieved in two ways: (1) By engineering intrinsic NL into the memristor device (Xie et al., 2006; Choi et al., 2011; Joshua Yang et al., 2012), or (2) Introducing a non-linear device, so-called selector, in series with the memristor (Upadhyay et al., 2020) at each crosspoint. In the first approach combining the non-linear mechanism and switching characteristics in one structure makes it difficult to optimize both the memory and selector performance simultaneously and independently. So far, the maximum non-linearity demonstrated by such devices falls well short of the required NL for large array implementations. Connecting a selector in series with a memristor (the 2nd approach) gives freedom of optimizing memristor and selector independently. A transistor can also be used as a select element in the so-called 1T1R (1-transistor 1-ReRAM) array (Rao et al., 2019; Wang et al., 2020). However, the 3-terminal structure and large footprint of transistors are not ideal for CBAs. The high processing temperature of the transistors makes it almost impossible to be used in 3D stacked memories. So the best approach to solve the sneak path problem is to use two-terminal thin-film-based selector devices that can be scaled laterally and stacked vertically together with a memristor (Chen, 2015; Burr et al., 2016).

In **Supplementary Figure 1**, we presented a table (extension of the table from Xia and Yang, 2019) comparing the figure of merits of all types of selector devices proposed in the literature. The tunneling selector stands out as the most promising one because of the following reasons: (1) electroforming-free operation; (2) low cycle to cycle variation; (3) high endurance (theoretically infinite); (4) in-principle low-temperature dependence; and (5) high-speed operation. In one of our recent work, we have demonstrated that such a tunneling selector even withstands the memristor's electroforming operation in a vertically integrated 1S1R cell (Upadhyay et al., 2020). This paper proposes a trilayer tunneling selector with a stack structure of Ge/Pt/TaN$_{1+x}$/Ta$_2$O$_5$/TaN$_{1+x}$/Pd. Here TaN$_{1+x}$/Ta$_2$O$_5$/TaN$_{1+x}$ layers form the trilayer tunneling barrier structure. Ge/Pt and Pt layers are BE and top electrode (TE), respectively. We engineer the Ge/Pt BE to provide an ultrasmooth surface on which a trilayer stack could be deposited. The root-mean-square (rms) roughness and peak-to-valley height distribution of the Ge/Pt layer were measured to be 185 and 700 pm, respectively.
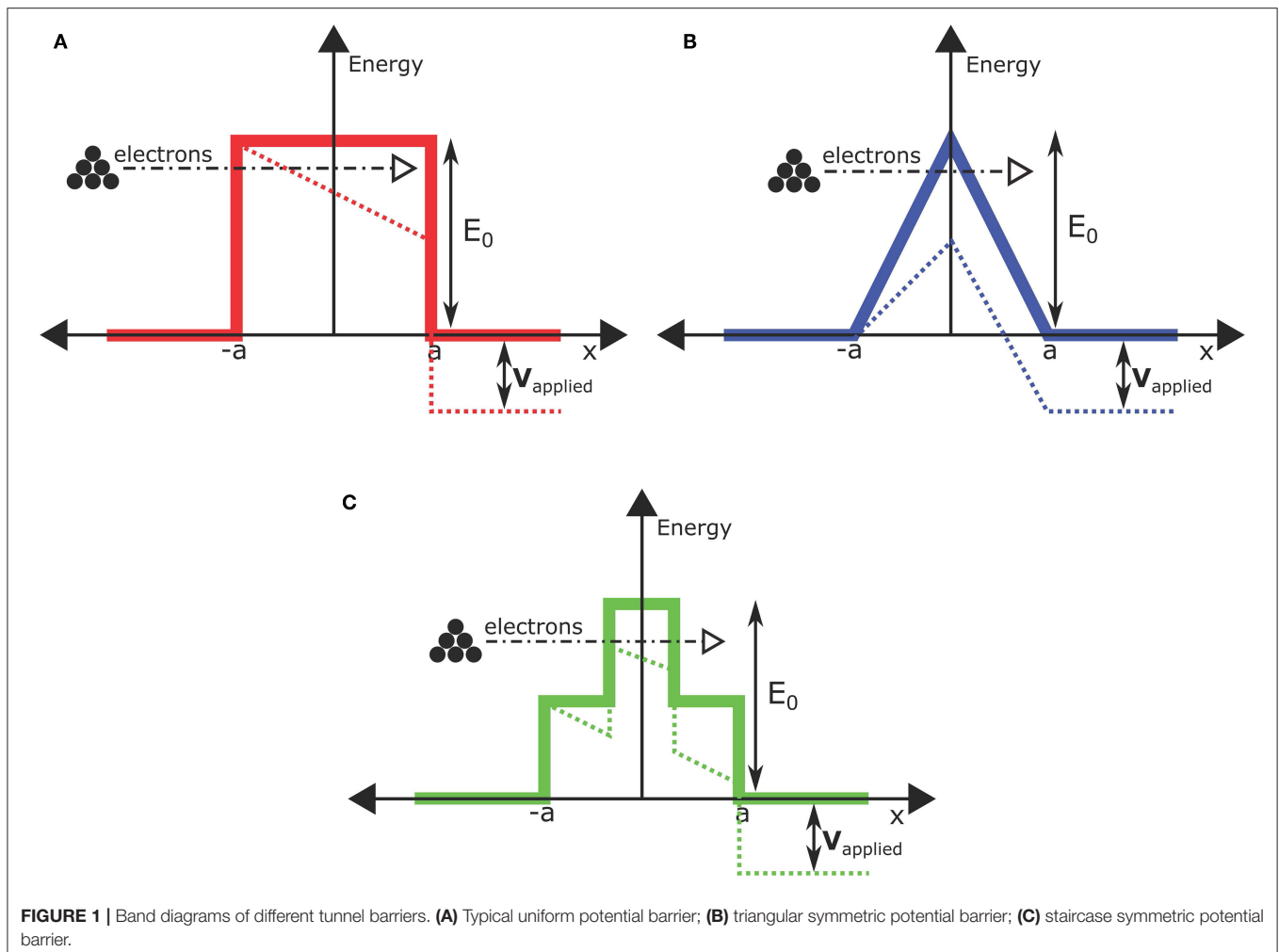
The requirements of a smooth BE surface for the tunneling selector will be discussed in detail in the next section. Using the proposed trilayer tunneling device, we have shown a record NL of 3×10^5 and 10^7 for one-half and one-third biasing

schemes, respectively. This is the highest NL among all tunneling based selectors reported so far. Furthermore, we integrated Pd/Ta$_2$O$_5$/Ru based memristor on top of the proposed selector device to realize a 1S1R cell. The 1S1R cell shows a maximum ON/OFF ratio of 100 and a NL of 10^4 and 10^6 for one-half and one-third biasing schemes, respectively. Again this is the highest NL demonstrated so far in any vertically integrated 1S1R cells to the best of our knowledge. The entire stack of the proposed 1S1R cell was deposited at room temperature, making it CMOS compatible and 3D stackable.

TUNNELING SELECTOR DESIGN

Even though tunneling selectors have many advantages over other types of selectors, their mediocre value of NL has been a shortcoming. The highest NL reported in tunneling selectors was 1.1×10^4, which we demonstrated in our previously reported work (Choi et al., 2016). We showed a trilayer tunneling barrier (TLTB) based selector could outperform the uniform barrier based selectors. As shown in **Figure 1A**, in the case of a uniform barrier device, the highest part of the barrier, closest to the electron source, is barely affected by the applied voltage. While for a "crested" barrier (**Figure 1B**) structure, the highest part of the barrier is in the middle and can be pulled down by the electric field quickly. Hence not only the barrier width but also the barrier height of such a crested barrier are much more sensitive to the applied electric field, resulting in a steeper current increase upon applied voltage and a higher non-linearity (Likharev, 1998; Jung and Cho, 2008). In other words, an applied voltage across the device only changes the barrier's width in the case of the regular rectangular barrier with a uniform barrier height. In contrast, both the barrier's width and height are reduced simultaneously upon applied voltages for the crested barrier. In practice, we can approximate a crested barrier structure with the staircase potential patterns formed in a trilayer structure, as shown in **Figure 1C**. We can achieve such a staircase energy barrier structure by sandwiching a dielectric layer with a small electron affinity between two other dielectric layers with larger electron affinities. This structure could be exploited for designing a high non-linearity selector. In this paper, we present a trilayer tunneling selector based on Ge/Pt/TaN$_{1+x}$/Ta$_2$O$_5$/TaN$_{1+x}$/Pd layers. The proposed TLTB (TaN$_{1+x}$/Ta$_2$O$_5$/TaN$_{1+x}$) layers form a staircase-like energy band structure, as shown in **Supplementary Figure 2**. This has been discussed in detail in our previous paper (Choi et al., 2016).
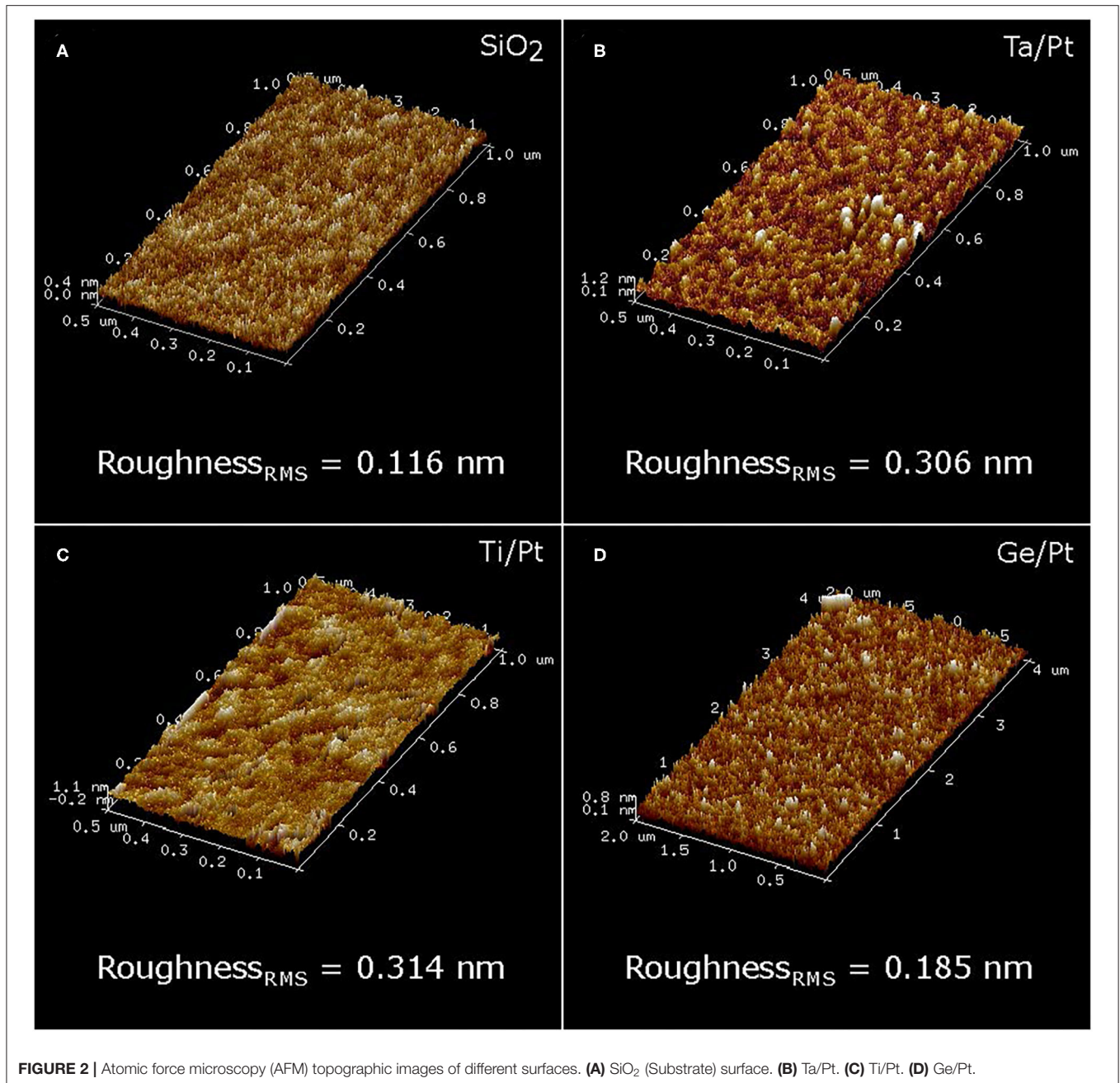
For designing a robust tunneling selector device, one needs to take care of two critical factors: (1) Depositing a high-quality dielectric layer that has minimal defects (e.g., Oxygen vacancies) and is stoichiometric and dense, which could be achieved by optimizing the deposition (sputtering in our case) recipe for the dielectric layers; (2) Having smooth surfaces and interfaces that can sustain a high electric field without breakdown. The roughness in the device stack could create hot spots due to the electric field concentration effect, resulting in an increase of the leakage current at relatively low voltage and low NL. With an increasing voltage, these hot spots can quickly

FIGURE 1 | Band diagrams of different tunnel barriers. **(A)** Typical uniform potential barrier; **(B)** triangular symmetric potential barrier; **(C)** staircase symmetric potential barrier.

cause a breakdown of the thin tunneling layers at relatively low voltages. To verify this hypothesis, we performed surface engineering for the device BE to obtain a much-smoothened surface. We found that depositing Pt on a thin Ge nucleation layer helps to achieve a smooth BE. For a comparative study, we deposited (evaporated) Ta (2 nm)/Pt (15 nm), Ti (2 nm)/Pt (15 nm), and Ge (2 nm)/Pt (15 nm) layers on a Si/SiO$_2$ substrate. **Figure 2** shows atomic force microscopy (AFM) topographic images of different surfaces. **Figure 2A** shows the rms (root mean square) roughness (R_q) of the substrate (Si/SiO$_2$) surface, which was measured to be 0.116 nm. **Figures 2B,C** present topographic images of the commonly used BE stacks Ta/Pt and Ti/Pt, with the R_q being 0.306 and 0.314 nm, respectively. **Figure 2D** presents the value of R_q for the Ge/Pt layer, which came out to be 0.185 nm. To ascertain uncertainties in the rms roughness measurement, we have done additional analysis presented in **Supplementary Figure 3**. The Ge/Pt layer not only has a significantly lower R_q but also a narrower peak-to-valley surface topological height distribution compared to those of Ta/Pt and Ti/Pt films, as shown in **Supplementary Figure 4**. The reason why a Ge nucleation layer provides smooth Pt film may

be related to the activation energy of diffusion. If the activation energy of Pt diffusion on Ge is higher than those on the Ta and Ti surfaces, in that case, it could reduce the surface diffusion and mass transportation of Pt on the Ge nucleation layer, which could result in a smoother surface topology (Logeeswaran et al., 2009). Ge/Pt layer also provides good adhesion with the substrate but maybe not as great as Ti/Pt and Ta/Pt layers.
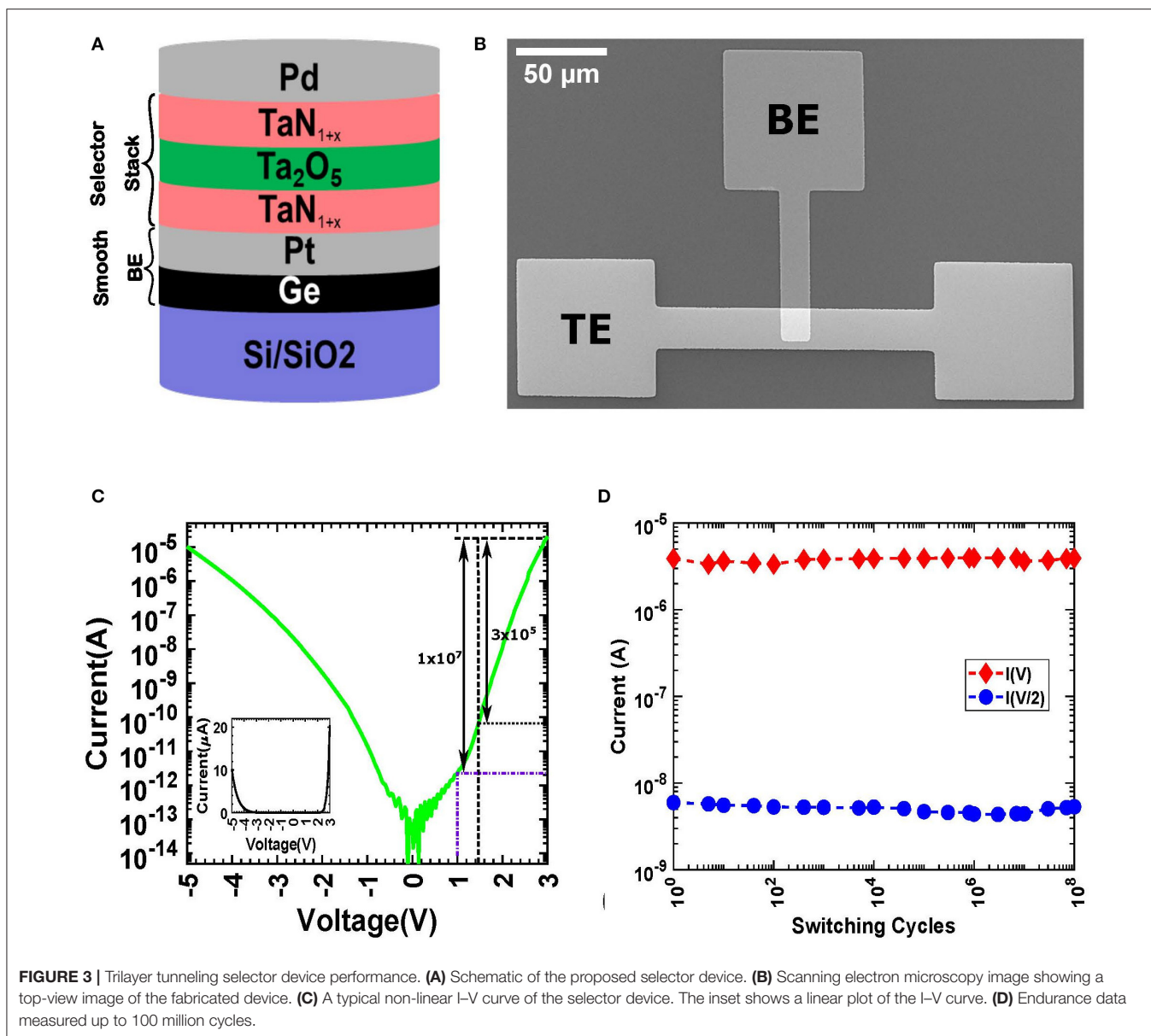
Next, we propose and demonstrate a highly non-linear TLTB selector device built upon the engineered smooth BE layers, as schematically shown in **Figure 3A**. Given that the BE smoothness is very critical to improving the performance of the TLTB selector device and the BE roughness will be affected by the surface roughness of the substrate itself, we took extensive measures to make sure the polished Si/SiO$_2$ (100 nm) substrate surface is clean and smooth. Starting with dipping the substrate in the Piranha solution [a mixture of H$_2$SO$_4$: H$_2$O$_2$ (3:1)] for 10 min, so residual organics were removed from the sample surface, followed by rinsing in the deionized water, followed by a blow-dry using compressed N$_2$ gun. Then to further smoothen out the substrate surface, CHF$_3$ + O$_2$ plasma cleaning (Turner and Chi, 2003; Ashraf et al., 2017) was performed in a Reactive

FIGURE 2 | Atomic force microscopy (AFM) topographic images of different surfaces. **(A)** SiO_2 (Substrate) surface. **(B)** Ta/Pt. **(C)** Ti/Pt. **(D)** Ge/Pt.

Ion Etching (RIE) chamber for 2 min. Finally, the substrate was cleaned with acetone in the ultrasonic bath for 10 min to remove any particle/contamination from the previous plasma cleaning step. We then rinsed it in IPA (Isopropanol) in the ultrasonic bath for 10 min to dissolve the acetone with the contaminant, followed by a blow-dry using compressed N_2. Immediately after finishing the substrate cleaning procedure, a photoresist (PR) was spin-coated on the substrate to maintain the surface cleanliness for the subsequent deposition of selector layers.

The PR coated substrate was then exposed by UV (ultraviolet) light through a mask for defining BE, then Ge (2 nm)/Pt (15 nm)

layer was deposited using the e-beam evaporator followed by the standard lift-off process. Tri-layer tunneling stack [TaN_{1+x} (4 nm)/Ta_2O_5 (3 nm)/TaN_{1+x} (4 nm)] was deposited as a blanket layer without breaking the vacuum, using RF magnetron sputtering. The TaN_{1+x} layers were deposited using a ceramic TaN (99.99%) target in Ar + N_2 medium. The TaN target has a 1:1 ratio of Ta & N, which gives it metallic characteristics. Using Ar + N2 mixture as the deposition gas medium, the deposited TaN_{1+x} film's conductivity could be tuned based on the N_2 partial pressure (Yu et al., 2002). Similarly, an Ar + O_2 medium was used for Ta_2O_5 deposition using a ceramic Ta_2O_5 (99.99%) target. The

FIGURE 3 | Trilayer tunneling selector device performance. **(A)** Schematic of the proposed selector device. **(B)** Scanning electron microscopy image showing a top-view image of the fabricated device. **(C)** A typical non-linear I–V curve of the selector device. The inset shows a linear plot of the I–V curve. **(D)** Endurance data measured up to 100 million cycles.

presence of a low oxygen partial pressure during the sputtering improves the density and the stoichiometry of the sputtered Tantalum oxide film (Duggan et al., 1993). Finally, the standard photolithography process was used to define the TE, and Pd (40 nm) was deposited using DC sputtering, followed by the lift-off process. It is worth noting that the entire selector stack was deposited at room temperature, making this proposed device CMOS compatible. The SEM (scanning electron microscope) micrograph of the $20\,\mu m \times 15\,\mu m$ crosspoint device is presented in **Figure 3B**.

Keysight B1500 device parameter analyzer was used to measure the I–V characteristics of the selector device. Bias was applied to the TE, and the BE was grounded. The I–V characteristics of the proposed TLTB selector device is plotted (semi-log) in **Figure 3C**, where the inset shows the linear plot of

the same sweep cycles. The proposed TLTB selector device shows very insulating behavior under low bias ($\approx$70 pA at +1.5 V). It becomes highly conductive at a high bias ($\approx$20.4 μA at +3 V), which results in a highly non-linear I–V characteristic of the proposed selector device. For one-half-voltage scheme NL is defined as $NL_{1/2} = I(V_{read})/I(V_{read}/2)$ and for one-third biasing scheme NL could be given as $NL_{1/3} = I(V_{read})/I(V_{read}/3)$. The measured NL of the device is around 3×10^5 (10^7) for one-half (one-third biasing) schemes, as indicated in **Figure 3C**, which is the highest NL of any tunneling selector device reported so far. **Supplementary Figure 5** shows multiple I–V sweep of the selector device. A control sample with the same TLTB structure but on different BE layers, i.e., Ti/Pt, showed a NL of about 100, as shown in **Supplementary Figure 6**, which indicates the importance of using a smooth BE for tunneling

selector devices. Endurance measurement was conducted on the proposed selector device for 100 Million cycles without any noticeable degradation, as shown in **Figure 3D**, using 5 µs wide 3 V (V_{read}) and 1.5 V ($V_{read}/2$) pulses. It should be noted here that we used B1530A Waveform Generator/Fast Measurement Unit (WGFMU) for the endurance measurement. The noise floor of WGFMU unit is limited to a few nA of current, which resulted in a smaller NL (Compare to the actual NL of the selector device), observed during the endurance test.
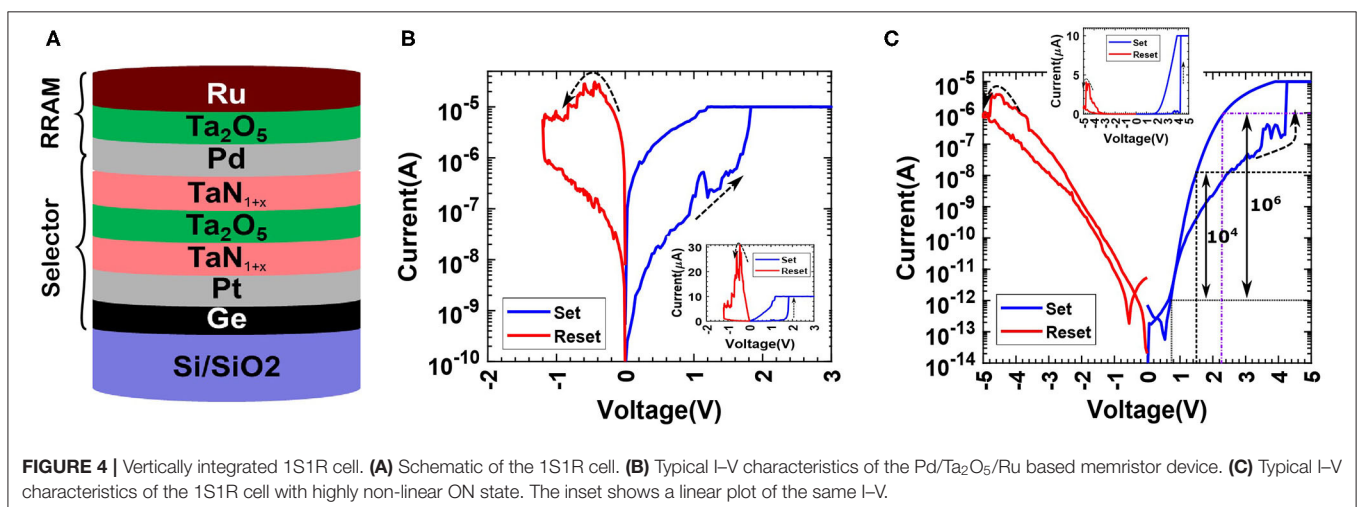
To further demonstrate the effect of the proposed smooth BE (Ge/Pt) on tunneling selectors, we fabricated uniform barrier devices consisting of the TLTB stack's layers. **Supplementary Figure 7** shows the schematic of the devices and their electrical performance. **Supplementary Figures 7A,B** shows schematic of the Ge/Pt/Ta_2O_5/Pd and Ge/Pt/TaN_{1+x}/Pd devices and **Supplementary Figures 7C,D** shows their respective I–V characteristics. The NL of the single tunnel barrier selectors based on Ta_2O_5 and TaN_{1+x} layers was measured to be 2×10^3 and 1×10^3, respectively. It is worth noting that the NL demonstrated by these simple uniform barrier devices is an order of magnitude higher than the NL of previously reported similar single barrier devices and other tunneling selector devices (Kawahara et al., 2013; Woo et al., 2014). We attribute this improvement in NL to the use of a Ge/Pt based smooth BE layer.

VERTICALLY INTEGRATED 1S1R CELL

To demonstrate the feasibility of integrating the proposed selector device with a memristor, a vertically integrated 1S1R cell has been fabricated. We used a recently proposed Ru based memristor device (Yoon et al., 2020) for this demonstration. Ru based memristor exhibit forming free and low power switching operations, making it suitable for a 1S1R integration. **Figure 4A** presents a schematic of the vertically integrated 1S1R stack. A polished Si/SiO_2 (100 nm) substrate was cleaned and Ge (2 nm)/Pt (15 nm), TaN_{1+x} (4 nm)/Ta_2O_5 (3 nm)/TaN_{1+x} (4 nm) layers were deposited following the methods described in the previous section. Afterward, the Middle electrode (ME) was

patterned using photolithography. A 40 nm thick Pd layer as the ME was sputter-deposited on top of the tri-layer tunneling stack, followed by the lift-off process. To isolate the selector layer from the memristor layer to be deposited on top of it, a 20 nm thick SiO_2 blanket isolation layer was deposited using sputtering. Then the SiO_2 isolation layer was patterned and etched away using the RIE ($CHF_3 + O_2$) to define the device region (see **Supplementary Figure 8** for details). A 10 nm thick blanket Ta_2O_5 switching layer was deposited using RF magnetron sputtering. Finally, the TE was patterned using the photolithography process, and a 40 nm thick Ru layer was sputter-deposited using the DC magnetron sputtering followed by the lift-off process (see the Experimental Section for more details). **Supplementary Figure 8** presents a wide-angle view of the cross-section of the 1S1R device. For the top memristor (1R) device, the Ru (TE) acts as an active electrode, while Pd (ME) serves as the inert electrode. It is worth noting that in this vertically integrated 1S1R cell, the selector was deliberately placed at the bottom to exploit the smooth BE (Ge/Pt) for achieving a high NL. We designed this testing structure in a way that the ME can be electrically accessed so that measurements can be made not only on the "1S1R" cell but also on the individual "S" and "R" to better understand the device stack.

For characterizing the Ru based memristor device, bias was applied to the TE of the integrated cell, the ME was grounded, and the BE was left floating. **Figure 4B** presents the I–V characteristics of the memristor device. To SET the device, a positive dual-sweep voltage (blue lines) was applied with current compliance (I_{cc}) set to 10 µA. Starting with a high resistance state (HRS), the device switched to a low resistance state (LRS) at 1.8 V and maintained its state during the reverse sweep. A negative dual-sweep voltage (red lines) was applied to RESET the device without any I_{cc}. Beginning with the LRS, device RESET started at about −0.4 V, and it switched to HRS at about −1.2 V and maintained its state afterward during the reverse sweep. The linear plot of the same I–V is presented in the inset. This switching mechanism is attributable to the Ru conductive path's formation/rupture in the switching layer. A metallic path in the

FIGURE 4 | Vertically integrated 1S1R cell. **(A)** Schematic of the 1S1R cell. **(B)** Typical I–V characteristics of the Pd/Ta_2O_5/Ru based memristor device. **(C)** Typical I–V characteristics of the 1S1R cell with highly non-linear ON state. The inset shows a linear plot of the same I–V.
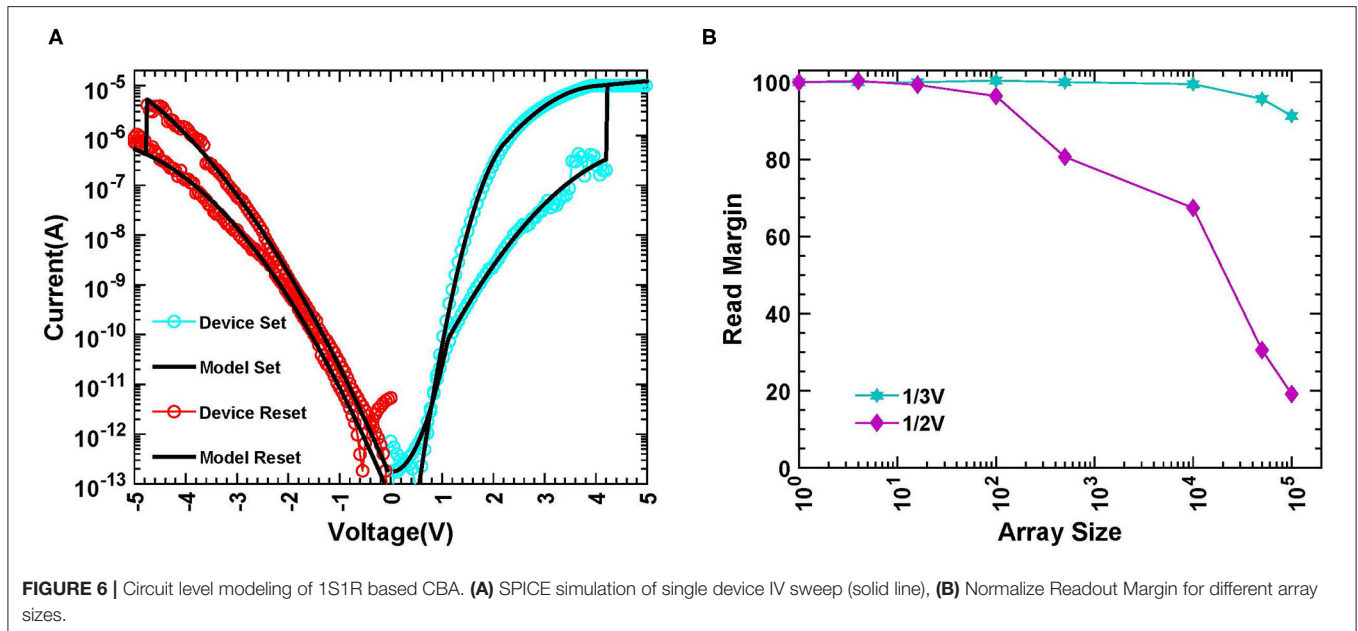
LRS is corroborated also by the Ohmic behavior observed in the LRS (Yoon et al., 2020).

Next, the vertically integrated 1S1R cell was electrically tested to demonstrate successful 1S-1R operations. Bias was applied to the TE, and the BE was grounded with the ME left floating. The non-linear I–V characteristic of the device is presented in **Figure 4C**. The 1S1R cell exhibit a NL of 10^4 (10^6) for one-half (one-third) biasing scheme at $V_{read} = 1.5$ V with an ON/OFF ratio of around 50. The highest ON/OFF ratio of 100 could be achieved at $V_{read} = 3.4$ V but with a reduced NL

value of 150. Interestingly there is a trade-off between high NL and maximum memory window size and can be leveraged depending on the use cases. It should be noted that adding a resistor (memristor in the 1S1R) reduces the NL of the selector by an amount depending on the relative resistance of the resistor and the selector. Nevertheless, the non-linearity exhibited in the proposed 1S1R cell is the highest among any vertically integrated 1S1R cell presented so far to the best of our knowledge. SEM micrograph showing the vertically integrated 1S1R device's top view is presented in **Figure 5a**.
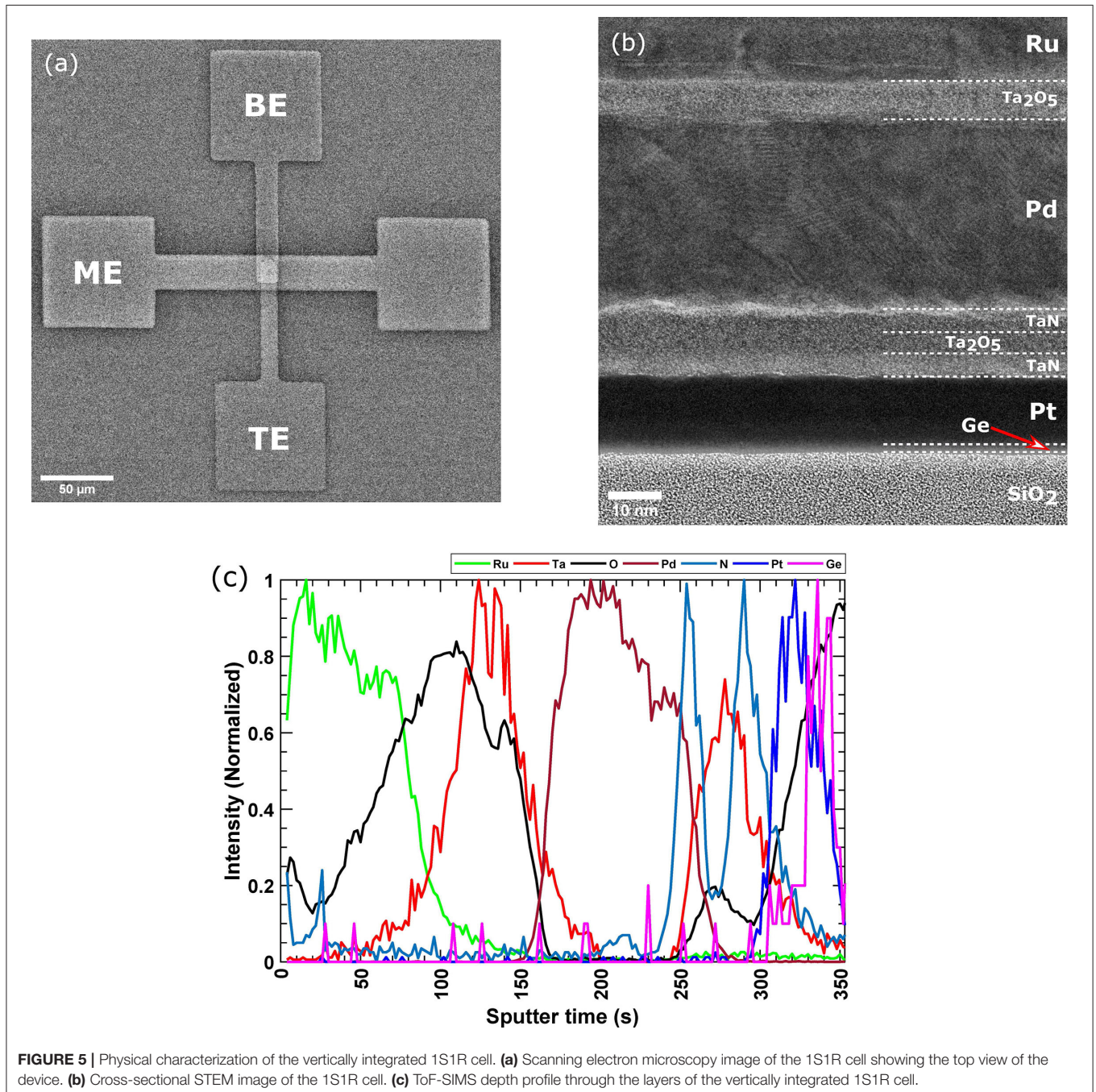
FIGURE 5 | Physical characterization of the vertically integrated 1S1R cell. **(a)** Scanning electron microscopy image of the 1S1R cell showing the top view of the device. **(b)** Cross-sectional STEM image of the 1S1R cell. **(c)** ToF-SIMS depth profile through the layers of the vertically integrated 1S1R cell.

FIGURE 6 | Circuit level modeling of 1S1R based CBA. **(A)** SPICE simulation of single device IV sweep (solid line), **(B)** Normalize Readout Margin for different array sizes.

TE, ME, and BE are marked on the figure. Cross-section scanning transmission electron microscopy (STEM) image of the 1S1R cell (Ge/Pt/TaN$_{1+x}$/Ta$_2$O$_5$/TaN$_{1+x}$/Pd/Ta$_2$O$_5$/Ru) is presented in **Figure 5b**. STEM micrograph revealed that the TLTB layers were amorphous. Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) was conducted at the active region of the 1S1R device. **Figure 5c** presents the depth profile through the vertically integrated 1S1R cell, identifying the stack's key elements.

To demonstrate the proposed selector capability, we did a circuit simulation of the 1S1R based CBA. The SPICE model was validated by comparing the experimental and simulated I–V characteristics of the single device, as shown in **Figure 6A**. The normalized readout margin for different sizes of the CBA is presented in **Figure 6B**. We considered the two most popular biasing schemes for our simulation: one-half and one-third voltage schemes. The readout margin for a 100 kbits CBA is around 20% for the one-half biasing scheme and more than 90% for the one-third biasing scheme. The one-third biasing scheme is more resilient to the sneak path current issue than the one-half biasing scheme. We can conclude from the results that the proposed selector helps mitigate the effect of the CBA's sneak path currents. It could potentially support a larger array size before the read margin hits the minimum criterion of 10% to differentiate the states (Lo et al., 2013). **Supplementary Figure 9** presents the readout resistance state of the selected device for various array sizes. HRS resistance decreases with array size because of an increase in sneak path current. Since readout current for LRS is larger than HRS, LRS current is only mildly affected by the sneak path current and so does the LRS resistance state.

CONCLUSION

In summary, we proposed and experimentally verified the critical role of layer smoothness and tunnel barrier shape

in determining tunnel-based selectors' non-linearity. To prove the concepts, we developed a Ge/Pt/TaN$_{1+x}$/Ta$_2$O$_5$/TaN$_{1+x}$/Pd based TLTB selector, which combined the benefit of a staircase potential barrier with the smooth BE. The proposed selector is CMOS compatible, 3D stackable, and exhibits a record NL value. We have engineered the BE layer (Ge/Pt) to make it an ultrasmooth surface. The measured rms roughness and peak-to-valley height distribution were 185 and 700 pm, respectively. This ultrasmooth BE surface and crested barrier lead to the demonstration of a record-high NL of 3×10^5. We further vertically integrated the proposed TLTB selector with a Ru based (Pd/Ta$_2$O$_5$/Ru) memristor device to demonstrate the feasibility of 1S1R integration and operation. The I–V characteristics recorded from this vertically integrated 1S1R cell show a maximum ON/OFF ratio of 100 and a NL of 10^4, also a record-high NL of any vertically integrated 1S1R cell ever reported. The excellent device NL performance suggests that our selector could be used to realize a large passive memristor array, which has remained elusive so far.

EXPERIMENTAL SECTION

Trilayer Selector Fabrication

A p-type (100) Si wafer with 100 nm thermal oxide was used as the substrate. The standard photolithography and lift-off process were used to define 15 μm wide Ge (2 nm)/Pt (15 nm) bottom electrode and 20 μm wide Pt (20 nm) top electrode using e-beam evaporation. A trilayer structure consists of TaN$_{1+x}$ (4 nm)/Ta$_2$O$_5$ (3 nm)/TaN$_{1+x}$ (4 nm) layers were sputter-deposited on top of the BE without breaking vacuum. TaN & Ta$_2$O$_5$ ceramic targets were used for RF magnetron sputtering in an Orion 8 (AJA international) sputtering system in the presence of an Ar-N$_2$ mixture (15:5) and Ar-O$_2$ mixture (20:1), respectively. Finally, 15 μm wide Pd (40 nm)

was sputter-deposited following standard photolithography and lift-off process.

Vertically Integrated 1S1R Device Fabrication

On a p-type (100) Silicon substrate with 100 nm thick thermal oxide, a $20\,\mu m$ wide Ge (2 nm)/Pt (15 nm) line (BE) defined by photolithography and lift-off process, was fabricated. Then a trilayer structure consists of TaN_{1+x} (4 nm)/Ta_2O_5 (3 nm)/TaN_{1+x} (4 nm) layers were sputter-deposited on top of the BE without breaking vacuum. TaN & Ta_2O_5 ceramic targets were used for RF magnetron sputtering in an Orion 8 (AJA international) sputtering system in the presence of $Ar-N_2$ mixture and $Ar-O_2$ mixture, respectively. Afterward, a $15\,\mu m$ wide middle electrode was patterned by photolithography, and a 40 nm thick Pd layer was deposited by RF magnetron sputtering followed by a lift-off process. A 20 nm thick SiO_2 isolation layer was sputter deposited on the top of the selector layer to isolate it (in the non-device-region) from the memristor layers to be deposited on top of it. The SiO_2 layer in the device region was patterned and etched away before a 10 nm thick blanket Ta_2O_5 switching layer was deposited using RF magnetron sputtering. Finally, $10\,\mu m$ wide TE was patterned using photolithography, and then a Ru (40 nm) layer was deposited using sputtering followed by a lift-off process.

Device Characterization

The DC measurements were performed using a B1500A semiconductor parameter analyzer (Keysight), and B1530A (Keysight) was used for pulse measurement. All electrical measurements were performed by applying the bias to the TE and grounding the BE. The cross-sectional TEM study of the Ge/Pt/TaN_{1+x}/Ta_2O_5/TaN_{1+x}/Pd/Ta_2O_5/Ru device and the EDS element mapping was performed using JEOL NEOARM atomic-resolution STEM at an accelerating voltage of 200 kV. FEI Nova 200 Dual-Beam FIB was used to prepare the FIBed TEM lamella. ToF-SIMS measurements were done using a TOF.SIMS.5-NSC instrument, using a Bi_3^+ ion gun (30 keV energy, 0.49 nA current) as the primary ion source and an $O2^-$ ion gun (1 keV energy, 120 nA current, $20\,\mu m$ spot size) as the sputter source. ToF-SIMS measurements were performed in the non-interlaced mode, where every scan of chemical analysis with primary bismuth source was followed by sputtering using an $O2^-$ ion gun. A low energy electron flood gun was used for charge compensation between cycles. The vacuum level in the ToF-SIMS during the measurements ranged from 5 to 9×10^{-9} mbar.

SPICE Modeling

The device model was written using Verilog-A. Cadence Virtuoso was used for the circuit simulation. For all the simulations worst-case scenario has been considered. The selected device lies farthest to the row voltage source as well as farthest to the column current sense amplifier. All the unselected and half selected devices were switched to ON state before start of simulation.

DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/**Supplementary Material**, further inquiries can be directed to the corresponding author/s.

AUTHOR CONTRIBUTIONS

JY conceived the concept. JY, QX, and NU designed the experiments, fabricated the devices, and performed electrical measurements. MC, NU, and TB carried out the STEM experiments. AI and NU performed the TOF-SIMS experiments. PM, NL, ND, and JK helped with experiments and data analysis. JY and NU wrote the paper. All authors discussed the results and implications and commented on the manuscript.

FUNDING

SUPPLEMENTARY MATERIAL

The Supplementary Material for this article can be found online at: https://www.frontiersin.org/articles/10.3389/fnano.2021.656026/full#supplementary-material

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