Reliable 2D Phase Transitions for Low-Noise and Long-Life Memory Programming

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Extending cycling endurance and suppressing programming noise of phase-change random-access memory (PCRAM) are the key challenges with respect to the development of nonvolatile working memory and high-accuracy neuromorphic computing devices. However, the large-scale atomic migration along electrical pulse direction in the unconstrained three-dimensional phase transitions of the phase-change materials (PCMs) induces big resistance fluctuations upon repeated programming and renders the classic PCRAM devices into premature failure with limited cycling endurance. Previous efforts of superlattice-like and superlattice PCM schemes cannot effectively resolve such issues. In this work, we demonstrated that, through fine-tuning the sputtering techniques, a phase-change heterostructure (PCH) of $Sb_2Te_3/TiTe_2$ can be successfully constructed. In contrast to its superlattice-like counterpart with inferior crystal quality, the well-textured PCH architecture ensures the reliable (well-confined) two-dimensional phase transitions, promoting an ultralow-noise and long-life operation of the PCRAM devices. Our study thus provides a useful reference for better manufacturing the PCH architecture and further exploring the excellent device performances and other new physics.

Keywords: phase-change random-access memory, two-dimensional phase transitions, programming noise, cycling endurance, heterostructure

INTRODUCTION

With the development of the Internet of Things, the exponentially growing demands in data processing and storage have imposed critical requirements on the energy efficiency and computing speed for data-centric tasks. But in the current computing system based on classic von Neumann architecture, the constant data shuttling between a fast central processing unit (CPU) and other much slower program and storage memory units leads to significantly wasted working power and limited computing speed (Kestor et al., 2013; Wong and Salahuddin, 2015). Extensive studies on phase-change random-access memory (PCRAM) (Wuttig, 2005; Raoux et al., 2010) thus have been devoted to resolving the issues. One route is to renovate the von Neumann architecture by alleviating performance mismatch among hierarchical memories (Lam, 2010; Rao et al., 2015; Yu and Chen, 2016; Rao et al., 2017), such as Intel's Optane DC (Choe, 2017) chips bridged between volatile dynamic random-access memory (DRAM) and nonvolatile solid-state drive (SSD) flash memory. The other is to innovate non-von Neumann architecture by unifying processing with storage in PCRAM cells, such as neuromorphic computing of three paradigms (Kuzum et al., 2012; Tuma et al., 2016; Burr et al., 2017; Boybat et al., 2018; Ielmini and Wong, 2018; Le Gallo et al., 2018; Sebastian et al., 2018): in-memory computing, deep neural networks, and spiking neural networks.

Commercialized PCRAM device encodes digital information through reversible transformation between amorphous and crystalline phases of chalcogenide PCMs (Chen et al., 2019; Rao et al., 2019), e.g., $Ge_2Sb_2Te_5$ (GST). Typical (mushroom- or pillar-type) PCRAM devices execute three-dimensional (3D) phase transitions of GST film, where extensive cycles of high-energy/high-bias RESET (melting and amorphization) operation pulses trigger long-distance migrations of Sb (Ge) and Te elements in opposite (vertical) directions (Padilla et al., 2010; Xie et al., 2018), giving rise to the phase segregation and the formation of large voids near the bottom electrode. This degrades the performing reliability and limits the endurance of mass-produced GST devices to $\sim 10^9$–10^{12} cycles (Yu and Chen, 2016; Xie et al., 2018), obstructing the implementation of PCRAM as nonvolatile working memory (with $> \sim 10^{16}$ cycles) for the deep modification of the von Neumann architecture (Wong and Salahuddin, 2015). Such a considerable deviation/ variation in composition and microstructure during the unconstrained 3D phase transitions generates large fluctuations (noises) in programming resistance states, which poses crucial challenges to the accomplishments of high-accuracy and high-efficiency matrix-vector multiplications, unsupervised learning of temporal patterns, and other data-centric computational tasks (Burr et al., 2017; Sebastian et al., 2018).

Many efforts, e.g., superlattice-like (SLL) (Chong et al., 2006; Lu et al., 2012; Chia Tan et al., 2013) and superlattice (SL) (Simpson et al., 2011; Soeya et al., 2013; Takaura et al., 2014) PCM architectures, have been made to address the issue of limited endurance, attempting to tailor the 3D phase transitions into 2D fashion. However, both schemes encounter difficulties in maintaining a reliable 2D structural transformation upon repeated programming, because the RESET operations must be cautiously performed to avoid local overheating; otherwise the multilayers may melt together and then quench into a mixed amorphous phase (Simpson et al., 2011; Li et al., 2018), as the melting temperatures (T_m, being ~ 900–$1,000$ K) of the adopted PCMs in SLL or SL architectures are quite close (Chong et al., 2006; Simpson et al., 2011; Lu et al., 2012; Chia Tan et al., 2013; Soeya et al., 2013; Takaura et al., 2014). In addition, the growth condition must be tightly controlled to construct Ge(Sn)Te/Sb_2Te_3 SLs as Ge(Sn)Te is chemically reactive and may alloy into Ge(Sn)SbTe-like compounds easily during synthesis (Li et al., 2018). Inspired by the previous findings, we recently proposed a distinct approach to address the above issues by an innovative PCH design using Sb_2Te_3/$TiTe_2$ stackings (Ding et al., 2019). The relations between crystal quality of such stackings and the derived electrical performances have not been disclosed yet. In this work, we draw direct comparisons between Sb_2Te_3/$TiTe_2$ SLL and PCH (SL) cases. Note that here we only care about the sputtering technology that is commonly employed in mass production of PCRAM chips, rather than other techniques such as molecular beam epitaxy or chemical vapor deposition. We further reveal that, in contrast to the SLL case, only the well-textured (highly oriented) PCH architecture can guarantee a reliable 2D switching to inhibit large-scale (long-distance) atomic

diffusion along electrical pulse direction, enabling substantially prolonged cycling endurance and suppressed programming noise.

EXPERIMENTAL SECTION

Film Preparation and Characterization

The Sb_2Te_3 and $TiTe_2$ films were deposited on a SiO_2/Si substrate by sputtering the respective pure target in ultra-high vacuum with a base pressure of $< \sim 1 \times 10^{-8}$ Torr, and the deposition pressure was under ~ 4.7 mTorr. For *in situ* heating (at $\sim 300°C$) deposition of the Sb_2Te_3, $TiTe_2$, and PCH films, the deposition rate of Sb_2Te_3 and $TiTe_2$ sublayers was controlled to be ~ 0.5–1.0 nm/min. A ~ 5 nm thick Sb_2Te_3 seed layer was predeposited on the substrate before PCH film deposition. The ordinary Sb_2Te_3, $TiTe_2$, and SLL films were deposited at room temperature without the seed layer, and the deposition rate of Sb_2Te_3 and $TiTe_2$ sublayers was controlled to be ~ 5 nm/min. The deposited Sb_2Te_3 and $TiTe_2$ sublayers are ~ 5 nm and ~ 3 nm thick in PCH and SLL architectures. Half of the as-deposited films were postannealed at $300°C$ for 1 h. A ~ 10 nm thick SiO_2 capping layer was *in situ* grown on top of each film inside the vacuum chamber to avoid oxidation. The film compositions were confirmed by Axios X-ray fluorescence spectrum (PANalytical B.V. Netherlands). The surface morphology of the films was analyzed by field emission scanning electron microscope (SEM) ZEISS SUPRA 55. The X-ray diffraction (XRD) method was employed to characterize the crystal structures of the films (~ 100 nm in thickness) in the 2θ range of 5–$60°$, using Cu/K_α radiation with a scanning step of $0.02°$.

Device Fabrication and Electrical Characterization

Mushroom-type SLL- and PCH-based PCRAM devices with tungsten bottom electrode contact of ~ 190 nm in diameter were fabricated using the 0.13 μm node complementary metal-oxide semiconductor technology. The thickness of the SLL and PCH films in the devices was controlled to be ~ 70 nm. The ~ 15 nm thick TiN and ~ 300 nm thick Al films were used as top electrode in all devices. The PCH film was deposited onto the bottom electrode of the PCRAM device under $\sim 300°C$, while SLL film in the PCRAM device was deposited at room temperature. The as-fabricated SLL-based device then was postannealed at $300°C$ for 1 h. All the electrical measurements on PCRAM devices were performed by using the Keithley 2400C source meter (measuring device/film resistance) and the Tektronix AWG5002B/AWG5202 pulse generator (generating voltage pulse with a minimum width of ~ 6 ns).

Ab Initio Simulations

All the ab initio simulations were carried out with Vienna Ab initio Simulations Package (VASP) (Kresse and Hafner, 1993). The Perdew-Burke-Ernzerhof (PBE) functionals (Perdew et al., 1996) and the projector augmented wave (PAW) pseudopotentials (Blöchl, 1994) were used for VASP. The 233-atom hexagonal supercells of SLL and PCH architectures were

FIGURE 1 | (A) XRD curves of ~100 nm thick Sb_2Te_3, $TiTe_2$, and SLL films sandwiched between SiO_2 layers (see the corresponding sketch). The films were all deposited at room temperature and then postannealed at 300°C for 1 h, mainly showing the hexagonal (Hex) lattice configuration. For the sake of better observing the weak diffraction peaks, the diffraction intensity is multiplied by 50 for all the curves. **(B–D)** SEM images of the postannealed Sb_2Te_3, $TiTe_2$, and SLL films, respectively.

simulated with periodic boundary conditions by NVT density functional theory- (DFT-) based molecular dynamics (DFMD). The energy cutoff is 180 eV and the time step is 3 femtoseconds.

RESULTS AND DISCUSSION

Crystal Orientation and Morphology

Regarding the SLL films synthesized at room temperature, the sublayers are usually amorphous or have poor crystallinity (Chong et al., 2006; Lu et al., 2012; Chia Tan et al., 2013). Similar situation was observed for the Sb_2Te_3/$TiTe_2$ SLL samples, as well as the pure Sb_2Te_3 and $TiTe_2$ films grown on SiO_2 substrates (**Supplementary Figure S1**). We employed strong postannealing actions (at 300°C for 1 h) on the as-deposited samples to promote crystallization (**Figure 1A**). Both the Sb_2Te_3 and $TiTe_2$ films possess a hexagonal lattice configuration with multiple different (random) crystal orientations (**Figure 1A**), showing polycrystalline morphology with quite small grain size (< ~20 nm) (**Figures 1B,C**). One can find many crystal ribbons and particles that may belong to the Ti-rich titanium tellurides precipitate from the annealed $TiTe_2$ film (**Figure 1C**), which shall form rough interfaces between the sublayers inside the SLL film. It is clear that the postannealed Sb_2Te_3/$TiTe_2$ SLL film inherits almost all the crystal orientations from its subunits (**Figure 1A**), as well as an unsmoothed surface

where some crystal grains aggregated into small islands (**Figure 1D**).

In stark contrast to the inferior crystalline qualities of the as-deposited and postannealed SLL films, the diffraction intensity, crystal orientation, and surface morphology of the samples fabricated by using *in situ* heating (at ~300°C) and slow growth (~0.5–1.0 nm/min) technique (see Materials and Methods) are significantly optimized (**Figure 2**). A ~5 nm thick hexagonal Sb_2Te_3 seed layer was pregrown on the SiO_2 substrate before the film deposition (Saito et al., 2016; Zhou et al., 2016), acting as a crystallization template to assist epitaxial-like crystal growth. All the *in situ* heating samples have much higher diffraction intensities than those of the postannealed ones, denoting the complete crystallinity for the formers (**Supplementary Figure S2**). It is also worth noting that only the strong (0 0 *l*) diffraction peaks appear for the *in situ* heating Sb_2Te_3 sample (**Figure 2A**), whereas the most prominent diffraction peaks of the postannealed Sb_2Te_3, i.e., (0 1 5) and (1 0 10) in **Figure 1A**, become invisible. This identifies that the degree of *c*-axis orientation of Sb_2Te_3 crystal is greatly improved by the optimized growth technique. The *in situ* heating Sb_2Te_3 sample has quite larger hexagonal grains (>~150–200 nm), with the (0 0 *l*) plane parallel to the substrate surface (**Figure 2B**). The *in situ* heating $TiTe_2$ sample is also well oriented along *c*-axis (**Figure 2A**), exhibiting a uniform surface morphology (**Figure 2C**), without any big segregated crystals of non-(0 0 *l*) orientations. On this basis, we then alternately deposited the
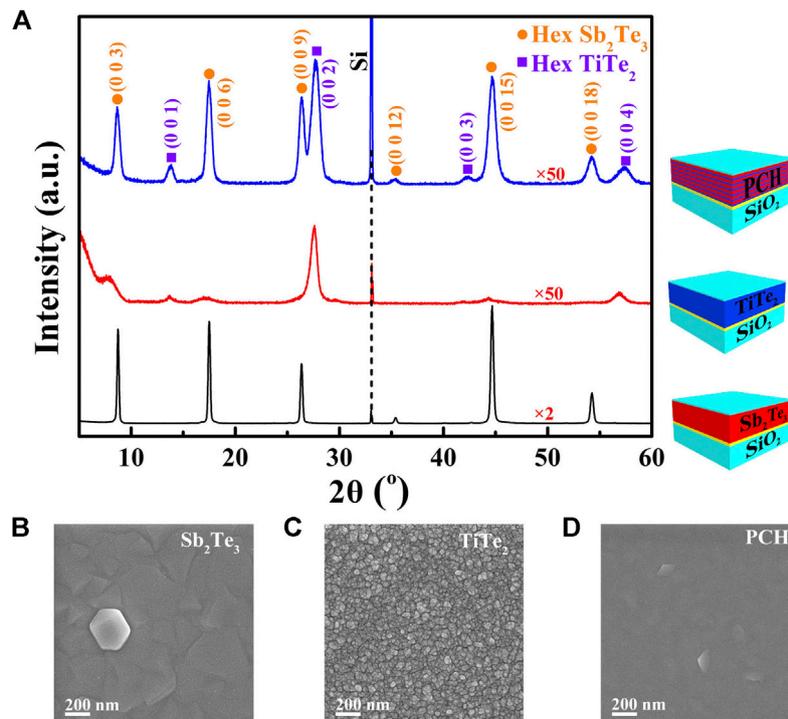
FIGURE 2 | (A) XRD curves of ~100 nm thick Sb_2Te_3, $TiTe_2$, and PCH films sandwiched between SiO_2 layers (*see* corresponding sketch). All the films were deposited at 300°C on the pregrown seed layer (yellow thin layer in each sketch), exhibiting hexagonal (Hex) lattice configuration with strong *c*-axis (0 0 *l*) orientation. For the sake of better observing the weak diffraction peaks, the diffraction intensity is multiplied by 2 for the Sb_2Te_3 curve and 50 for the $TiTe_2$ and PCH curves. **(B–D)** SEM images of the *in situ* heating deposited Sb_2Te_3, $TiTe_2$, and PCH films, respectively.
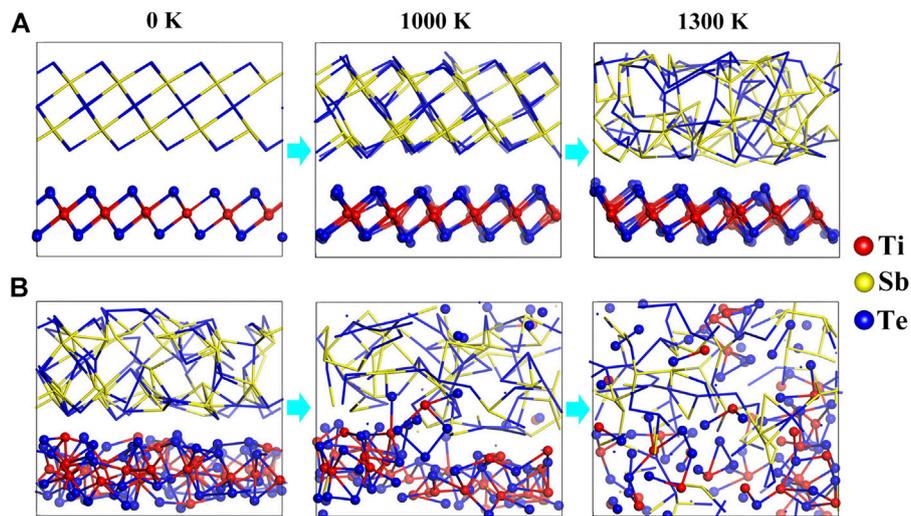
FIGURE 3 | (A) DFMD simulations of the melting process of the PCH model. The PCH model is firstly heated up to 1,000 K rapidly within 30 ps. The Sb_2Te_3 and $TiTe_2$ sublayers are ordered. The Sb_2Te_3 sublayer is fully melted at 1,300 K after 30 ps, while the $TiTe_2$ sublayer remains in the stable crystalline form. **(B)** DFMD simulations of the melting process of the SLL model. The SLL model contains partially ordered Sb_2Te_3 and $TiTe_2$ sublayers. After heating up to 1,000 K for 30 ps, the Sb_2Te_3 sublayer becomes fully disordered and mixes with the $TiTe_2$ sublayer. As the model is further heated at 1,300 K for 30 ps, the whole model becomes a fully disordered liquid phase.
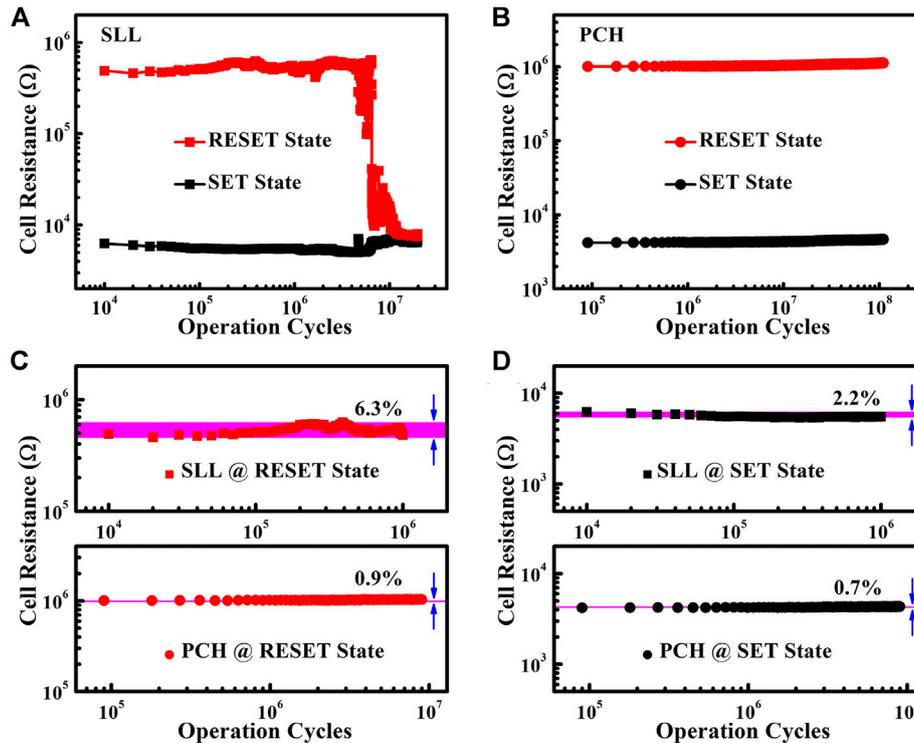
FIGURE 4 | (A) Approximately ~10^7 cycling endurance of the SLL-based PCRAM device that finally failed due to SET stuck: SET (under 2.1 V) and RESET (under 3.2 V) with 20 ns width voltage pulses. **(B)** Approximately ~10^8 cycles of the PCH device without failure under 10 ns width SET (1.6 V) and RESET (2.4 V) operations voltage pulses. **(C)** Comparison of the RESET resistance fluctuations between the SLL- and PCH-based device, with the RSD being 6.3 and 0.9%, respectively. **(D)** Comparison of the SET resistance fluctuations between the SLL- and PCH-based device, with the RSD being 2.2 and 0.7%, respectively.

Sb_2Te_3 and $TiTe_2$ nanolayers to construct the PCH architecture. Unsurprisingly, it also displays only the (0 0 *l*) diffraction peaks corresponding to the ones of its subunits (**Figure 2A**). Compared to the coarse granular surface of the SLL film, triangular crystals with rather bigger size (> ~100 nm) and pretty smooth texture were formed in the PCH film with (0 0 *l*) facets parallel to the substrate surface (**Figure 2D**).

Reliable Two-Dimensional Phase Transitions

In the well-textured Sb_2Te_3/$TiTe_2$ PCH, the $TiTe_2$ blocks with high chemical and thermal stabilities are capable of being the robust confinement layers to restrict the phase transitions of the Sb_2Te_3 blocks on 2D scale, as demonstrated by the DFMD simulations (**Figure 3A**). The initial PCH model was heated up to 1,000 K and maintained for 30 ps, where both Sb_2Te_3 and $TiTe_2$ blocks can still keep crystalline form. As the temperature further increases to 1,300 K, and after 30 ps, the Sb_2Te_3 block is fully melted, while the $TiTe_2$ block remains to be ordered.

Regarding the as-deposited and postannealed SLL films of poor crystallinity, there are most likely no clean and nonatomic (van der Waals-like) gaps between their sublayers; therefore the interlayer force cannot be weak enough. The closely bound sublayers may be merged into a compound (bulky) phase

upon aggressive RESET operation or extensive programming, making the 3D switching dominate eventually. Our DFMD simulations also qualitatively illustrated such a phenomenon (**Figure 3B**), where initially the Sb_2Te_3 and $TiTe_2$ sublayers are chosen to be partially crystallized (or quite disordered) as according to the crystallographic results shown in **Figure 1** and **Supplementary Figure S2**. The SLL model experienced exactly the same heating process as the PCH model. The sublayers in the SLL model are totally disordered after heating at 1,000 K for 30 ps, and the subsequent heating at 1,300 K for another 30 ps finally melts them down into a mixed liquid.

Extended Cycling Endurance and Suppressed Programming Noise

We fabricated the mushroom-type SLL- and PCH-based PCRAM devices with the same geometry (*see Materials and Methods* section) to draw comparison of their electrical performances. The PCH-based device has lower SET and RESET voltages as compared to those of the SLL-based device (**Supplementary Figures S3, S4**), correlating to the reduced programming energy. As for the unconstrained 3D phase transitions, PCMs are subjected to nonisothermal and nonequilibrium shocks, giving rise to composition variation upon extensive programming caused by long-range element diffusions along the electrical current direction (Padilla et al., 2010; Xie et al.,

2018). Eventually, the device fails due to severe phase segregation and big void formation near the bottom electrode. The SLL-based device underwent repeated 3D phase transitions up to $\sim 10^7$ cycles until SET sticking failure took place (**Figure 4A**). We note similar SLL-based device also presented an approximate endurance (Shen et al., 2019), but showing considerably larger resistance fluctuations in both RESET and SET states than those of the SLL-based device studied in this work. The relative standard deviations (RSDs) of RESET and SET states of the SLL-based device are 6.3% (**Figure 4C**) and 2.2% (**Figure 4D**), respectively.

The reliable 2D phase transitions of the PCH architecture inhibit the large-scale atomic diffusion along the electrical pulse direction, which effectively prolongs the endurance of the PCH-based device to $\sim 10^8$ cycles without reaching failure (**Figure 4B**). Note that the fast speed (~ 10 ns) and long-life features of the PCH-based device offer a feasible route to develop DRAM-like phase-change working memory technology. Most importantly, the PCH-based device has pretty low resistance fluctuation in both RESET and SET states, with the RSDs being 0.9% (**Figure 4C**) and 0.7% (**Figure 4D**), respectively. The ultralow programming noise of the PCH-based device should also be ascribed to the reliable 2D switching manner of the confined Sb_2Te_3 sublayers, because the randomness of phase transitions (the stochastic crystallization in particular) (Rao et al., 2017) is markedly reduced, leading to more consistent resistance contrast and hence better-defined logic states.

CONCLUSION

In summary, we have demonstrated that, through fine-tuning the deposition techniques, the multilayer $Sb_2Te_3/TiTe_2$ stackings can be made into c-axis oriented heterostructure, which shall exhibit weakly coupled interactions among the Sb_2Te_3 and $TiTe_2$ building blocks. In contrast to the SLL structure that can only execute 3D phase transitions, the PCH architecture is able to perform reliable 2D switching of the confined Sb_2Te_3 sublayers. The long-range element migration during 3D phase transitions induces device failure after extensive cycling, which can be greatly inhibited in the 2D switching manner, leading to the remarkably extended cycling endurance of the PCH-based device as

compared to the SLL-based one. This shall be conducive to the development of nonvolatile and long-life working memory to better renovate the classic von Neumann computing system. And above all, the PCH-based device presents rather smaller resistance fluctuations upon repeated programming than that of the SLL-based device. This low-noise feature is of necessity for the accomplishments of high-accuracy neuromorphic computing tasks.

DATA AVAILABILITY STATEMENT

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation.

AUTHOR CONTRIBUTIONS

TL and KD fabricated the films and performed the XRD and SEM tests. KD and FR prepared the device samples and carried out electrical measurements. KD performed ab initio simulations. FR and KD wrote the paper with contributions from BC. All authors discussed the results and commented on the manuscript. The project was initiated and conceptualized by FR.

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SUPPLEMENTARY MATERIAL

The Supplementary Material for this article can be found online at: https://www.frontiersin.org/articles/10.3389/fnano.2021.649560/full#supplementary-material.

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