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Gallium-incorporated TiO_2 thin films by atomic layer deposition for future electronic devices

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Titanium dioxide (TiO_2) with advantages including abundance in earth, non-toxicity, high chemical stability, surface hydrophobicity in dark, and extremely high permittivity could be highly promising for advanced electronics. However, the thermal stability and low bandgap (E_g) of TiO2 pose a big challenge for TiO_2 to be used as dielectric, which could be resolved by doping with other metal cations. In this work, we studied the impact of gallium incorporation on electrical and material characteristics of TiO_2 thin films. These TiO_2 and Ti_XGaO films with thickness of 15 nm were derived by atomic layer deposition (ALD) and then annealed in O_2 ambient at 500°C, where the levels of Ga incorporation were tuned by the cycle ratio (X) of TiO_2 to that of Ga_2O_3 during ALD growth. Both thin film transistors (TFTs) using Ti_XGaO (TiO_2) thin films as the channel and metal-oxide semiconductor capacitors (MOSCAPs) using Ti_XGaO (TiO_2) thin films as the dielectric were fabricated to unravel the impact of Ga incorporation on electrical properties of TiO_2 thin films. It is found that the Ga incorporation reduces the conductivity of TiO_2 thin films significantly. Pure TiO_2 thin films could be the ideal channel material for TFTs with excellent switching behaviors whereas Ga-incorporated TiO_2 thin films could be the dielectric material for MOSCAPs with good insulating properties. The leakage current and dielectric constant (*k*) value are also found to be decreased with the increased Ga content in Ti_XGaO/Si MOSCAPs. Additionally, the density of interface trap (D_{it}) between Ti_XGaO and Si were extracted by multi-frequency conductance method, where a "U-shape" trap profile with similar level of D_{it} values can be observed for Ti_XGaO MOSCAPs with varying Ga contents. Material characterizations show that the Ga incorporation destabilizes the crystallization and enlarges the bandgap (E_g) of TiO_2 while maintaining a smooth surface. Interestingly, Ga incorporation is found to decrease the overall oxygen content and introduce more oxygen-related defects in the film. As a result, the reduction of leakage current upon Ga incorporation in MOSCAPs could be explained by amorphization of the film and enlarged band offset to Si rather than oxygen defect passivation. These Ga-incorporated TiO_2 films may found promising usage in future electronic device applications such as trench capacitors in dynamic random-access memory,

where the emerging high-*k* dielectrics with low leakage currents and high thermal stability are demanded.

KEYWORDS

Ga incorporation, atomic layer deposition, crystallinity, high-permittivity dielectric, band alignment, interface traps, thin film transistor, dynamic random-access memory

1 Introduction

Metal oxides have enabled many emerging applications in advanced electronics such as CMOS back-end-of-line (BEOL)-compatible logic and memory components (Datta et al., 2019; Charnas et al., 2023; Kim et al., 2023). For instance, In-based oxides have been actively explored as channel material for BEOL-compatible transistors due to its high electron mobility, large area uniformity, excellent conformity on complex structure, and low-temperature processability (Samanta et al., 2020; Han et al., 2021; Si et al., 2022; Zhang et al., 2022; Zheng et al., 2022; Liao et al., 2023; Zhang et al., 2023). Hf-based oxides are also currently used as high-*k* dielectric in Si-based logic transistors and storage capacitors in dynamic random-access memory (DRAM) arising from its relatively high permittivity value (10–25), suitable band offsets to Si, sufficiently large bandgap (E_g), and high thermal stability (Wilk et al., 2001; Kim et al., 2013; Wang B. et al., 2018). Compared to other metal oxides, TiO_2 have unique advantages such as abundance in earth, non-toxicity, high chemical stability, surface hydrophobicity in dark, and extremely high permittivity (50–80) (Campbell et al., 1999; Kim et al., 2013; Park, 2018). In this regard, the usage of TiO_2 thin films in advanced electronics could be promising, providing a class of material of cost-effective and eco-friendly. In the literature, TiO_2 films could be semiconducting or insulating, which are dependent on the concentration of oxygen vacancy in the film (Kim et al., 2013). However, the reported mobility of semiconducting TiO_2 films is small with typical value lower than 1 $cm^2V^{-1}s^{-1}$ (Katayama et al., 2008; Park et al., 2008; Park et al., 2009; Zhong et al., 2012), which cannot meet the high current requirements. On the other hand, for insulating TiO_2 films the low E_g of TiO_2 (<4 eV) could induce high leakage currents, thereby impairing its dielectric performance (Campbell et al., 1999). These attributes have impeded the usage of TiO_2 films in advanced electronics, thus calling for more in-depth studies on the electrical and material properties of TiO_2-based thin films.

Previously, we demonstrated high-performance TiO_2 thin film transistors (TFTs) using O_2-annealed TiO_2 channel and high-*k* ZrO_2 dielectric (Zhang et al., 2019a; Zhang et al., 2019b; Zhang et al., 2020; Zhang et al., 2021a). These TiO_2 TFTs could achieve a high on/off current ratio (I_{on}/I_{off}) and low subthreshold swing (SS), which is comparable to that of InGaZnO counterparts (Zhang et al., 2019a), thus validating TiO_2 as channel material for TFT application. The excellent performance was attributed to the passivation of oxygen vacancy in TiO_2 channel from O_2 annealing, the usage of high-*k* ZrO_2 dielectric, and excellent interface between TiO_2 channel and ZrO_2 dielectric, resulting in high electron mobility of 5 $cm^2V^{-1}s^{-1}$ and low interface trap density (D_{it}) of ~10^{12} $eV^{-1}cm^{-2}$ (Zhang et al., 2021b). Furthermore, the crystallinity of TiO_2 is found to be crucial for electron transport. The conductivity of TiO_2 transits from insulting to semiconducting when the crystallinity of the TiO_2 film changes from amorphous to anatase polycrystalline by controlling the annealing temperature (Zhang et al., 2021a; Zhang et al., 2021c). Functional TiO_2 TFTs based on anatase polycrystalline TiO_2 channel could be achieved using a low temperature process of 300°C, meeting the requirements for BEOL transistors (Zhang et al., 2021a; Zhang et al., 2021c). On the other hand, the amorphous TiO_2 thin films also show a great promise for high-*k* dielectric application with a *k* value of ~28 (Zhang et al., 2021c). However, the thermal stability poses a big challenge for TiO_2 dielectrics considering the fact that TiO_2 thin film could crystallize at a low temperature of 300°C. For instance, the fabrication process for DRAM is typically above 500°C, the temperature of which would induce the crystallization of TiO_2 and cause high leakage current. Additionally, the relatively low E_g of TiO_2 (<4 eV) may also limit its dielectric usage to narrow bandgap channel materials. Doping TiO_2 with other metal cation may potentially resolve these issues, however, there are few studies on the electrical properties of doped TiO_2 in the literature.

In this work, we systemically investigated the effects of Ga incorporation on electrical and material characteristics of TiO_2 thin films by ALD, where the Ga incorporation was controlled by the cycle ratio (X) between TiO_2 and Ga_2O_3 during ALD growth. These films underwent O_2 annealing at 500 °C for 30 min after deposition. Then both TFTs and MOSCAPs were fabricated using these Ga-incorporated TiO_2 thin films. The conductivity of TiO_2 thin films is found to be reduced significantly upon Ga incorporation. The TiO_2/ZrO_2 TFTs show excellent switching behavior whereas the Ti_XGaO/Si MOSCAPs exhibit well-behaved dielectric properties. It is noted that X represents the cycle ratio during ALD instead of atomic percentage for Ti_XGaO. The leakage current and *k* value are also found to be decreased with the increased Ga content in Ti_XGaO/Si MOSCAPs, while the D_{it} value between Ti_XGaO and Si maintain roughly at the same level. A series of material characterizations were performed including Grazing incidence X-ray diffraction (GI-XRD), X-ray photoelectron spectroscopy (XPS), and atomic force microscope (AFM). It is revealed that the Ga incorporation destabilizes the crystallization and enlarges the E_g of TiO_2 while maintaining a smooth surface. Furthermore, the Ga incorporation is found to decrease the overall oxygen content and introduce more oxygen-related defects in the film. Thus, it is believed that the reduction of leakage current in MOSCAPs upon Ga incorporation could be explained by amorphization of TiO_2 and enlarged band offset rather than oxygen defect passivation. These Ga-incorporated TiO_2 films with well-behaved dielectric property under a process temperature of 500 °C may found promising usage in future electronic device applications such as trench capacitors in DRAM.

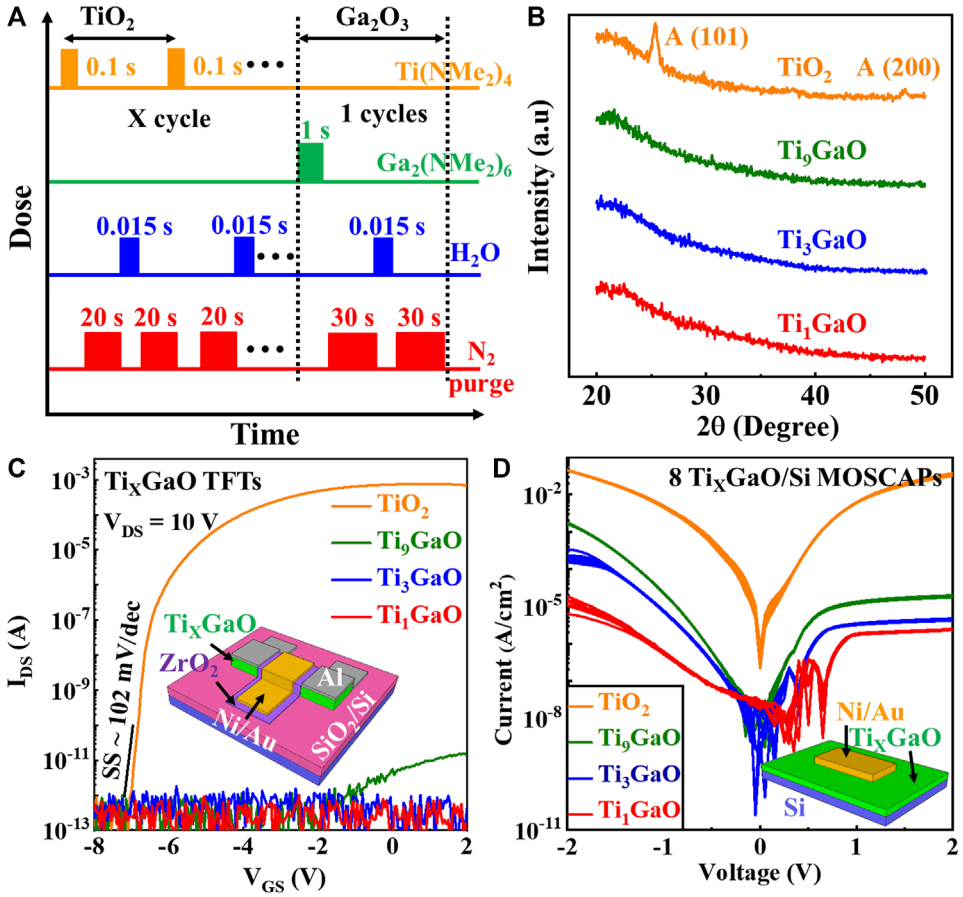

FIGURE 1
(A) Schematic of Ga-incorporated TiO_2 thin films by atomic layer deposition, where the incorporated Ga level is controlled by cycle ratio (X) of TiO_2 to that of Ga_2O_3. **(B)** Grazing incidence X-ray diffraction (GI-XRD) spectrum of 15 nm TiO_2 and Ti_XGaO films after 500°C O_2 annealing. **(C)** Transfer curves of thin film transistors (TFTs) under V_{DS} of 10 V using 15 nm TiO_2 and Ti_XGaO films as the channel materials. Inset: schematic of Ti_XGaO TFTs. **(D)** Leakage current density-voltage characteristic of TiO_2/Si and Ti_XGaO/Si metal-oxide semiconductor capacitors (MOSCAPs). Inset: schematic of Ti_XGaO/Si MOSCAPs. Note that X represents the cycle ratio during ALD instead of atomic percentage for Ti_XGaO.

2 Results and discussions

Figure 1A shows the schematic of ALD growth of Ga-incorporated TiO_2 film. The supercycle of Ti_XGaO film growth consists of X cycles of TiO_2 followed by one cycle of Ga_2O_3. The ALD growth of TiO_2 started with the pulse of Ti precursor ($Ti(NMe_2)_4$) for 0.1 s followed by N_2 purge for 20 s. Then, H_2O was pulsed into the chamber for 0.015 s followed by N_2 purge for 20 s, forming one growth cycle of TiO_2. Similarly, one Ga_2O_3 growth cycle consists of a pulse of Ga precursor ($Ga_2(NMe_2)_6$) for 1 s, a N_2 purge for 30 s, a pulse of H_2O for 0.015 s, and another N_2 purge for 30 s. These TiO_2 and Ti_XGaO films were deposited at 150°C on lightly-doped p-type Si substrates with a resistivity of 5 Ω cm for MOSCAP fabrication and on heavily-doped p-type Si (10^{-3} Ω cm) with 260 nm thermally oxidized SiO_2 for TFT fabrication. The samples were pre-heat at 150°C in the chamber for 10 min before film deposition. The thickness of Ti_XGaO films were controlled by the number of supercycles, and all films have the same thickness of 15 nm as confirmed by an ellipsometer. These films were then undergone 500°C O_2 annealing for 30 min by rapid thermal processing (RTP). The fabrication process of TFTs is consistent with our previous work (Zhang et al., 2019a; Zhang et al., 2019b; Zhang et al., 2020; Zhang et al., 2021a). Briefly, TiO_2/Ti_XGaO mesa isolations were formed by F-based inductively coupled plasma (ICP) etching on Si/SiO_2 substrates. Then, 250 nm Al was deposited as the source/drain contacts using e-beam evaporation. After that, 10 nm ZrO_2 was deposited by ALD as gate dielectric at 130°C. The TFT fabrication is finished by the evaporation of Ni/Au (170 nm/80 nm) as the gate metal stack by e-beam evaporation. The fabricated TFTs are in top-gate architectures with gate length (L_G) of 3 μm, gate-source/drain offset (L_{GS}/L_{GD}) of 1.5 μm and gate width (W_G) of 70 μm. For fabricating MOSCAPs, an array of metal contacts to TiO_2 or Ti_XGaO films were formed with Ni/Au (180 nm/70 nm) by e-beam evaporation. The metal contacts are square shapes with area of 200 × 200 μm^2, which is defined by photolithography. The schematic of fabricated TFTs and MOSCAPs are shown in the inset of Figures 1C, D, respectively.

Figure 1B exhibits the grazing incidence X-ray diffraction (GI-XRD) spectrum of 15 nm TiO_2 and Ti_XGaO films after 500°C O_2 annealing. Distinct diffraction peaks at 25.4° and 48.2° can be

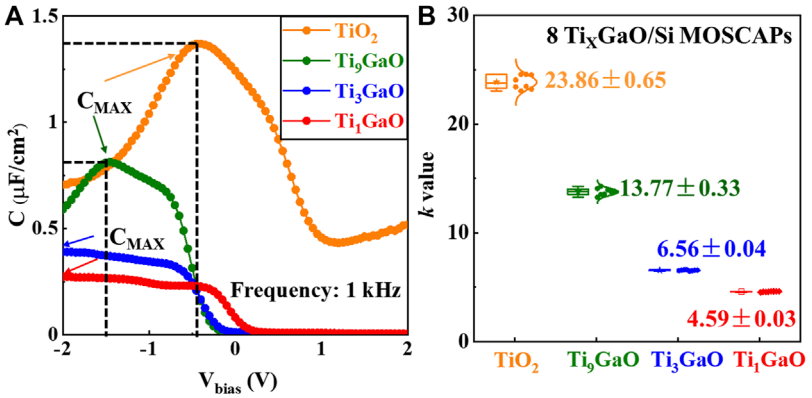

FIGURE 2
(A) Capacitance-voltage (C–V) characteristics of TiO_2/Si and Ti_XGaO/Si MOSCAPs at frequency of 1 kHz, where the maximum capacitances (C_{MAX}) of these MOSCAPs are marked. **(B)** Extracted dielectric constant (*k*) value of TiO_2 and Ti_XGaO films from C_{MAX}. Note that the *k* values of TiO_2 and Ti_9GaO can be underestimated due to the high leakage current.

observed for the TiO_2 film, corresponding to the (101) and (200) facets of anatase TiO_2, respectively (Zhang et al., 2019a). On the other hand, no observable peaks can be seen for Ti_XGaO films, indicating their amorphous nature. Thus, Ga could function as crystallization retarder to TiO_2 host, destabilizing its crystallization under 500°C process. Figure 1C exhibits transfer curves of TFTs under V_{DS} of 10 V using 15 nm TiO_2 and Ti_XGaO films as the channel materials. The TiO_2 TFTs show excellent switching behavior including a low SS of ~102 mV/dec and a high I_{on}/I_{off} of $>10^9$, being consistent with our previous work (Zhang et al., 2019a). On the other hand, the Ti_XGaO TFTs exhibit insignificant currents, which is also agree with the observation that the amorphous TiO_2 film presents insulating properties in our previous study (Zhang et al., 2021a).

This can be explained by the structural disorder induced gap states of amorphized Ti_XGaO film preventing electrons from transport within the Ti_XGaO film (Zhang et al., 2021a; Zhang et al., 2021c). Figure 1D shows the current density-voltage (J-V) characteristic of TiO_2/Si and Ti_XGaO/Si MOSCAPs, where the voltage is applied on top metal with Si substrate grounded. Consistent J-V behavior can be observed among 8 MOSCAPs for all the Ti_XGaO and TiO_2 films, which suggests the high uniformity of ALD-derived films. The TiO_2/Si MOSCAPs show a high leakage current with J value reaching 4.5×10^{-2} A/cm^{-2} under −2 V bias and 3.5×10^{-2} A/cm^{-2} under +2 V bias. The similarly large J values under both polarities of biases suggest that the TiO_2 film could not provide sufficient barrier for both electrons and holes from Si to transport into TiO_2 film by tunneling or field emission. The J values under both polarities of biases are decreased significantly upon Ga incorporation. Under −2 V bias, the J value decreases from 1.7×10^{-3} A/cm^{-2} to 2.1×10^{-4} A/cm^{-2} and 1.3×10^{-5} A/cm^{-2} for Ti_XGaO films when X reduces from 9 to 3 and 1, respectively. Similarly, under +2 V bias, the J value decreases from 1.9×10^{-5} A/cm^{-2} to 4.5×10^{-6} A/cm^{-2} and 2.4×10^{-6} A/cm^{-2} for Ti_XGaO films when X reduces from 9 to 3 and 1, respectively. The much-reduced J value under both bias voltages suggests that the increased barrier height for both electrons and holes from Si to transport into Ti_XGaO film by tunneling or field emission upon Ga incorporation. Additionally, the J values under +2 V bias are also lower than that of under −2 V bias, indicating that barrier height is larger for electrons compared to that of holes.

Figure 2A exhibits the capacitance-voltage (C-V) characteristics of TiO_2/Si and Ti_XGaO/Si MOSCAPs at frequency of 1 kHz. It is interesting to find that no depletion region can be observed under positive bias voltage (V_{bias}) in C-V characteristic of TiO_2/Si MOSCAPs, which agrees with the high J value under positive V_{bias} in Figure 1D. On the other hand, C-V characteristics of Ti_XGaO/Si MOSCAPs exhibit depletion regions, which can be explained by the low J value under positive V_{bias} after Ga incorporation. The maximum capacitances (C_{MAX}) of these MOSCAPs are also marked in Figure 2A. Both Ti_3GaO and Ti_1GaO MOSCAPs reach C_{MAX} under V_{bias} of −2 V, in contrast to that Ti_9GaO and TiO_2 MOSCAPs reach C_{MAX} under V_{bias} of −1.44 V and −0.44 V, respectively. The sudden drop of capacitance of Ti_9GaO and TiO_2 MOSCAPs under more negative V_{bias} could be due to their high leakage currents (Bonkerud et al., 2021). The dielectric constant (*k*) value can be estimated according to:

$$k = \frac{C_{MAX} \times d}{\varepsilon_0}, \quad (1)$$

where d is the thickness of TiO_2 and Ti_XGaO films, and ε_0 is the permittivity of free space (8.85×10^{-12} F/m). Figure 2B exhibits the statistically extracted *k* values for TiO_2 and Ti_XGaO films based on 8 MOSCAPs according to Eq. 1. The *k* value monotonically reduces from 23.86 for TiO_2 to 13.77 for Ti_9GaO, 6.56 for Ti_3GaO, and 4.59 for Ti_1GaO, respectively. The reduction of *k* value with the increased Ga incorporation can be understood by the fact that TiO_2 have a higher permittivity than that of Ga_2O_3 (Wilk et al., 2001; Wang B. et al., 2018). It needs to note that the *k* values of our TiO_2 and Ti_9GaO films can be underestimated due to their high leakage currents.

X-ray photoelectron spectroscopy (XPS) measurements were conducted to uncover the modification of chemical states of TiO_2 upon Ga incorporation, where spectra were taken from 15 nm TiO_2/Ti_XGaO films on Si after 500°C O_2 annealing. Figures 3A, B shows the Ti 2p and Ga 2p core-level spectrum, respectively. It is

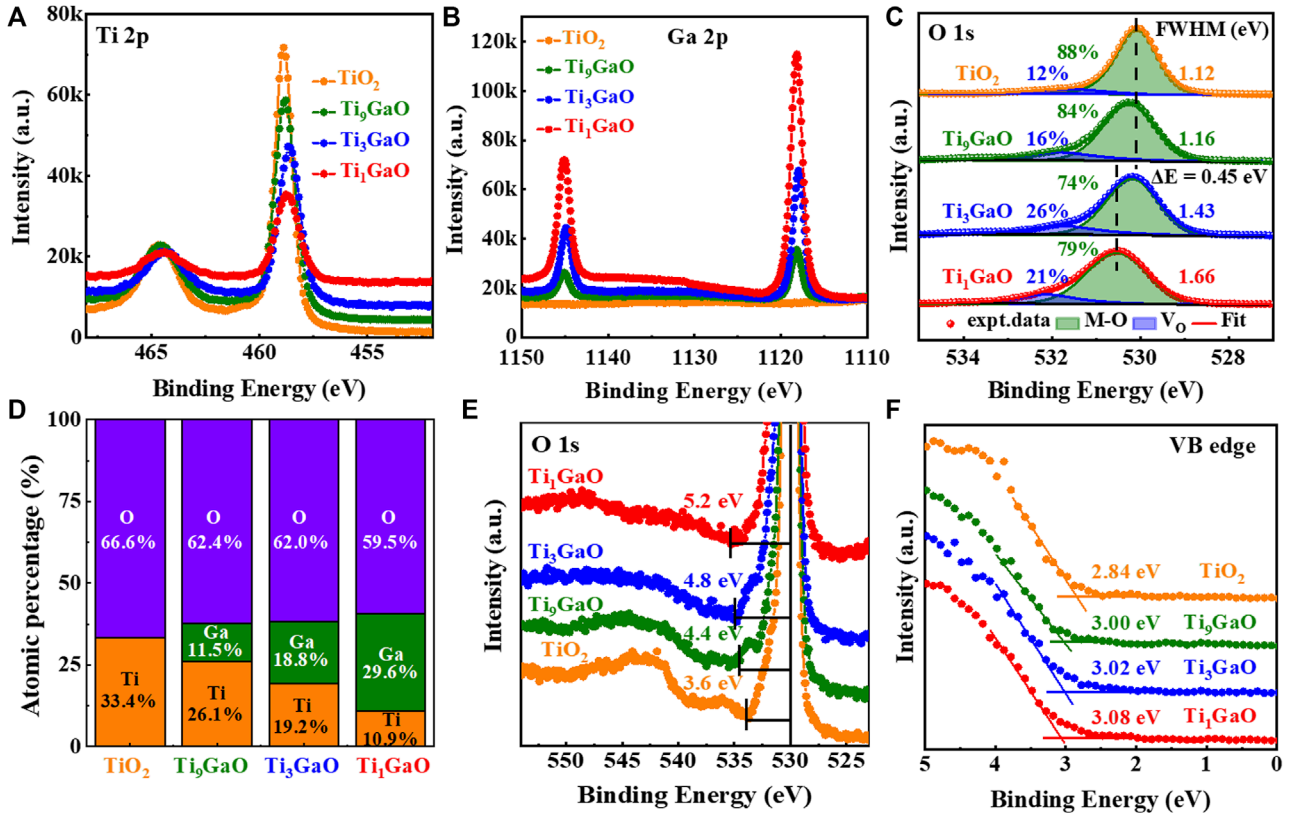

FIGURE 3
X-ray photoelectron spectroscopy (XPS) spectrum of **(A)** Ti 2p; **(B)** Ga 2p; and **(C)** O 1s of 500°C O_2-annealed TiO_2 and Ti_XGaO films with thickness of 15 nm. **(D)** Atomic percentage analysis of TiO_2 and Ti_XGaO films. **(E)** O 1s plasmon energy loss for bandgap (E_g) extraction; and **(F)** valence band (VB) edge of TiO_2 and Ti_XGaO films.

expected to observe that the intensity of Ti 2p spectrum is decreased whereas that of Ga 2p spectrum is increased with the decreased TiO_2 to Ga_2O_3 cycle ratio X. The peak position of Ti spectrum is also shifted to a lower binding energy level upon Ga incorporation in Figure 3A, where a negative binding energy shift (ΔE) of −0.17 eV can be observed from TiO_2 to Ti_1GaO. This is in contrast to that no distinct ΔE can be observed for Ga 2p spectrum in Figure 3B. Both Ti 2p and Ga 2p spectrum exhibit broadening features, where the full width at half maxima (FWHM) is increased from 0.81 eV for TiO_2 to 1.27 eV for Ti_1GaO in Figure 3A and that is increased from 1.28 eV for Ti_9GaO to 1.43 eV for Ti_1GaO in Figure 3B. The shifts and broadening features of spectrum could be due to the Ga substitution of Ti in TiO_2 host, where a stronger Ti-O bond (776 kJ/mol) is replaced by Ga-O bond (374 kJ/mol) (Wang et al., 2018; To et al., 2023). Figure 3C shows the O 1s spectrum of TiO_2 and Ti_XGaO films, where two peaks are fitted representing O bonding with metal cations (M-O) and O-related defects (V_O) such as oxygen vacancy and hydroxyl. A positive ΔE of 0.45 eV can be observed in the M-O peaks from TiO_2 to Ti_1GaO, which is accompanied by an increase of 0.54 eV in FWHM accordingly. This can be also explained by the fact that Ga substitutes Ti, leading to more O atoms bonding with Ga atoms. It is interesting to note that the V_O is increased upon Ga incorporation from 12% in TiO_2 to 21% in Ti_1GaO, suggesting that more O related-defects are introduced into the film due to the Ga incorporation. This is corroborated by the atomic percentage analysis of the film in Figure 3D, where the overall oxygen content is reduced from 66.6% in TiO_2 to 59.5% in Ti_1GaO. The reduced overall oxygen content and the increased O related-defects could be due to the fact that O/metal cation stoichiometry of TiO_2 (value of 2) is higher than that of Ga_2O_3 (value of 1.5) and that the bonding energies of Ti-O bond (776 kJ/mol) is stronger than that of Ga-O bond (374 kJ/mol) (Wang et al., 2018; To et al., 2023). The V_O is known to work as shallow donors and increase the electron concentration in oxides (Zhang et al., 2020; Zhang et al., 2023), which cannot explain the leakage current reduction in the MOSCAPs. It is also noted that the atomic percentage of Ga is much higher than the expected value from cycle ratio X. It might be due to the much longer pulse time of Ga precursor (1 s) compared to that of Ti precursor (0.1 s), and the different nucleation behaviors between Ti precursor on top of Ga-terminated surface and Ga precursor on top of Ti-terminated surface (Hong et al., 2021). The bandgap (E_g) of TiO_2 and Ti_XGaO can be estimated from the O 1s plasmon energy loss feature in Figure 3E. It is found that the, E_g is increased upon Ga incorporation, the value of which is increased from 3.6 eV for TiO_2 to 4.4 eV for Ti_9GaO, 4.8 eV for Ti_3GaO, and 5.2 eV for Ti_1GaO. It needs to mention that the exact value of E_g should not be taken seriously due to the limits of extraction method, and it is the increasing trend that should be paid attention

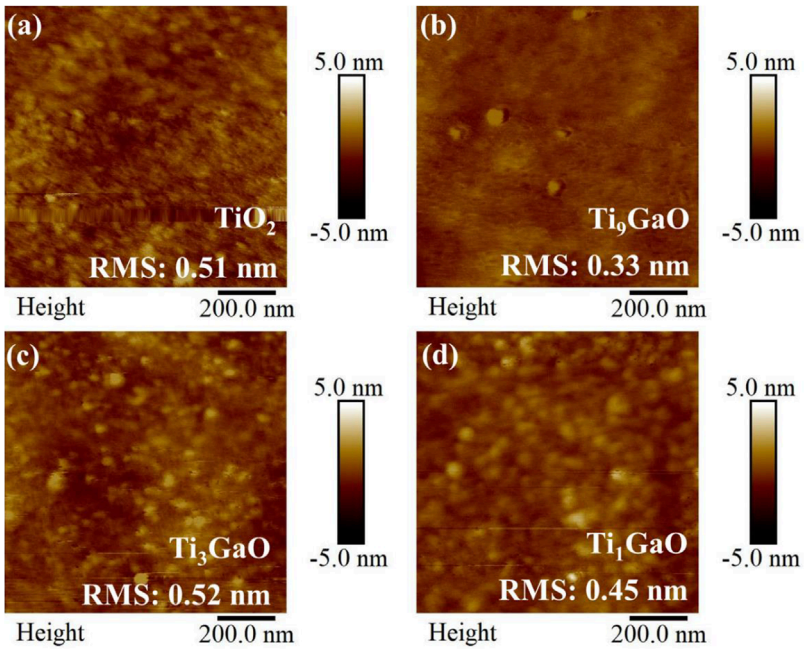

FIGURE 4
Atomic force microscope (AFM) scan of 15 nm **(A)** TiO_2; **(B)** Ti_9GaO; **(C)** Ti_3GaO; and **(D)** Ti_1GaO films on Si substrate after 500°C O_2 annealing, exhibiting a smooth surface with low root mean square (RMS) roughness. The scan area is 1 × 1 μm^2.

to. Figure 3F exhibits the valence band (VB) edge of TiO_2 and Ti_XGaO films, where a downshift of valence band maximum (VBM) can be seen upon Ga incorporation. Overall, XPS results show that Ga incorporation induces more O-related defects, enlarges the E_g and slightly downshifts the VBM of TiO_2.

The surface morphologies of TiO_2 and Ti_XGaO films were also examined by the atomic force microscope (AFM) in Figure 4. The AFM scans were in the tapping mode with the scan area of 1 × 1 μm^2. All the films show a smooth surface with a low root mean square (RMS) roughness, the value of which are 0.51 nm for TiO_2, 0.33 nm for Ti_9GaO, 0.52 nm for Ti_3GaO, and 0.45 nm for Ti_1GaO, respectively. The low RMS value is crucial for suppressing surface-roughness-induced leakage current and reducing the surface-roughness-related interface traps, thus benefiting to their applications in electronic devices. The density of interface trap (D_{it}) between Ti_XGaO and Si were extracted by multi-frequency conductance (G/ ω) method. Figure 5 show the conductance-voltage (G-V) measurements of TiO_2/Si and Ti_XGaO/Si MOSCAPs, where the applied frequency is varied from 1 kHz to 1 MHz. The TiO_2/Si MOSCAPs show large G/ ω values under both positive and negative V_{bias}, which is consistent with high leakage currents under both polarities of V_{bias} in Figure 1D. The changes in magnitude of G/ ω values and the shifts of G/ ω curves with the increased frequency can also be observed in Figure 5, which are induced by the trapping and detrapping of electrons through the interface traps. It is also well-known that two types of interface traps, acceptor-like traps and donor-like traps, exist at Si/oxide interfaces with "U" shape (Sze and Ng, 2006), which contributes to the frequency response of G/ ω curves.

The behavior of equivalent parallel conductance (G/ω) as a function of angular frequency (ω) can be modelled by the equation (Liu et al., 2015; Chandrasekar et al., 2017):

$$\frac{G}{\omega} = \frac{e\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2}, \tag{2}$$

where e is the elementary electron charge, D_{it} is the density of interface trap, τ_{it} is the trap lifetime constant. Figure 6 show the fitting results of the measured G/ω from TiO_2/Si and Ti_XGaO/Si MOSCAPs using Eq. 2, where the lines are the fitting results and symbols are the experimental data, matching each other well. Under a fixed bias voltage for every MOSCAP, each curve can be fitted into two trap states, suggesting the existence and contribution of two distinct trap states. The extracted D_{it} with corresponding τ_{it} can be mapped into the trap energy level relative to the conduction band of Si (E_C-E_T) by the Schockley-Read-Hall statistics (Liu et al., 2015; Chandrasekar et al., 2017):

$$\tau_{it} = \frac{1}{v_{th}\sigma_{n(p)}N_C}\exp\left(\frac{E_C - E_T}{kT}\right), \tag{3}$$

where v_{th} is the thermal velocity of Si (10^7 cm/s), $\sigma_{n(p)}$ is the capture cross section of electrons or holes (2×10^{-16} cm^2), and N_C is the effective density of states of Si (2.8×10^{19} cm^{-3}) (Sze and Ng, 2006).

Figure 7A exhibits the extracted D_{it} as a function of the E_C-E_T for TiO_2/Si and TixGaO/Si MOSCAPs based on Eqs 2, 3. A "U-shape" profile of interface trap can be observed for all the MOSCAPs, with a similar level of D_{it} values ranging from 4×10^{11} $eV^{-1}cm^{-2}$ to 10^{13} $eV^{-1}cm^{-2}$. This similar level of D_{it}

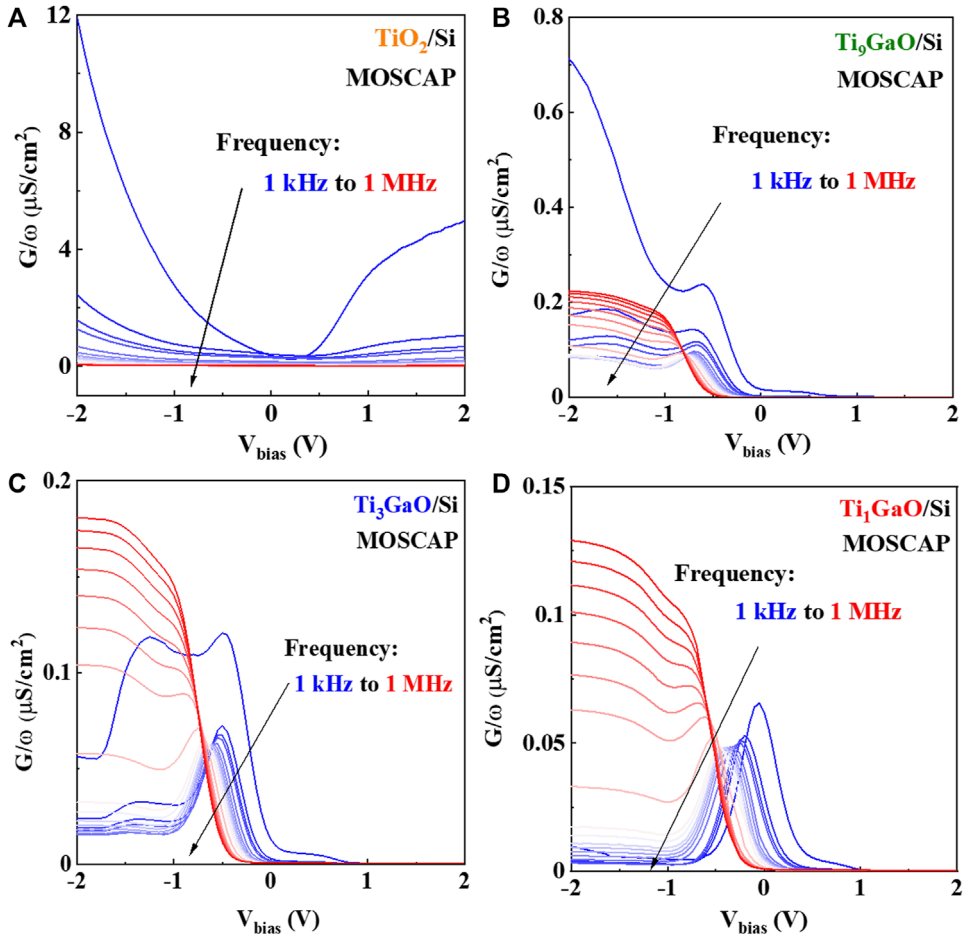

FIGURE 5
Multi-frequency conductance-voltage (G–V) measurement of **(A)** TiO_2/Si; **(B)** Ti_9GaO/Si; **(C)** Ti_3GaO/Si; and **(D)** Ti_1GaO/Si MOSCAPs, where the applied frequency is varied from 1 kHz to 1 MHz.

can be originated from the growth schematic of our Ti_XGaO films, which starts with TiO_2 growth cycle and may result in similar interface quality between Ti_XGaO and Si. Thus, the reduced leakage current in TixGaO/Si MOSCAPs with increased Ga incorporation could not be explained by interface trap passivation, which is also corroborated by XPS results showing increased O-related defects by Ga incorporation. Figure 7B shows the band alignment of Si, TiO_2, and Ti_1GaO derived from XPS results (Figure 3), where the valence band (E_V) offset is increased by 0.24 eV and the conduction band (E_C) offset is increased by 1.36 eV with Ga incorporation. The increased band offset can function as potential barrier for carriers, thereby reducing the leakage current. The asymmetric band offset could also explain why leakage currents of TixGaO/Si MOSCAPs are lower under positive V_{bias} than that of under negative V_{bias} in Figure 1D, where electrons are more difficult to overcome the larger E_C offset. Base on the above information, it is believed that the reduction of the leakage current in TixGaO/Si MOSCAPs upon Ga incorporation could be explained by the amorphization of Ti_XGaO film and the enlarged band-offset to Si rather than defect passivation.

3 Conclusion

In summary, we demonstrate that the Ga incorporation could be an effective way to improve the dielectric performances of TiO_2 films. Pure TiO_2 thin films could be the channel material for TFT application whereas Ga-incorporated TiO_2 thin films could be used as high-*k* dielectric with good insulating properties. The leakage current and *k* value are decreased with the increased Ga content, while the D_{it} value between Ti_XGaO and Si maintain roughly at the same level. The reduction of leakage current upon Ga incorporation is believed to be due to that the amorphization of TiO_2 and enlarged band offset to Si rather than oxygen defect passivation. These Ga-incorporated TiO_2 films with well-behaved dielectric property under a process temperature of 500 °C may found promising usage in future electronic devices such as trench capacitors in DRAM.

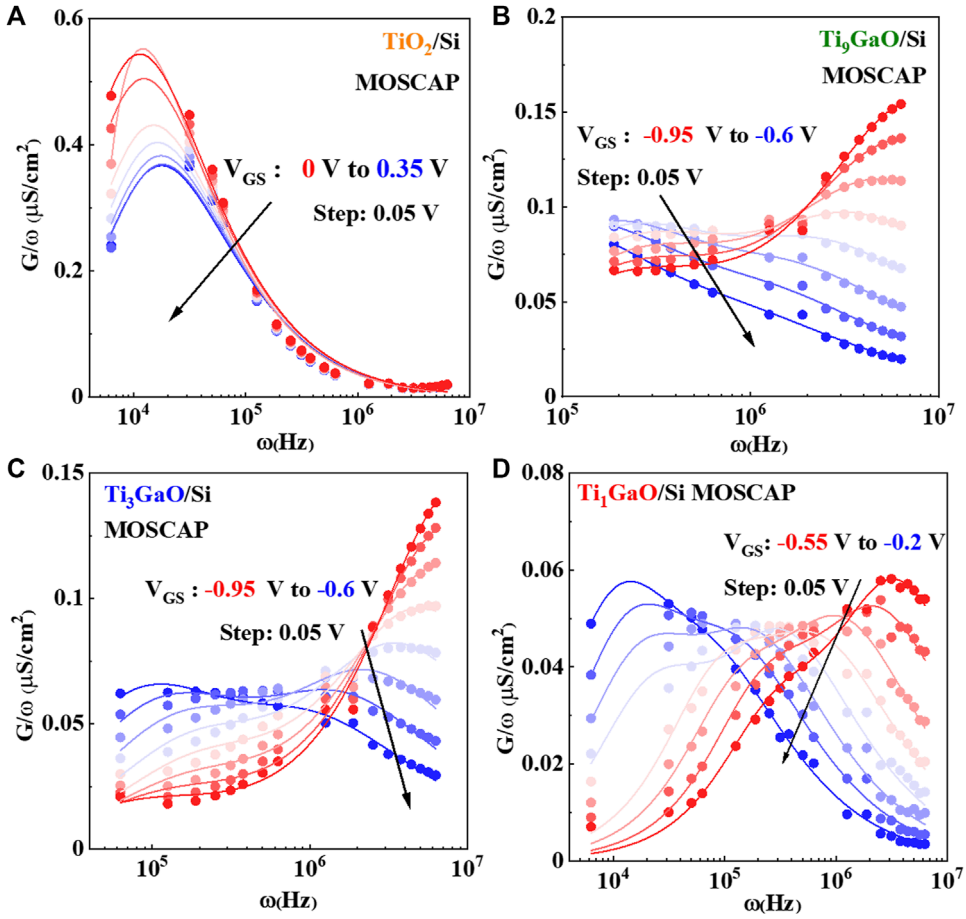

FIGURE 6
Equivalent parallel conductance (G/ ω) as a function of angular frequency (ω) for interface trap (D_{it}) extraction using conductance method for **(A)** TiO_2/Si; **(B)** Ti_9GaO/Si; **(C)** Ti_3GaO/Si; and **(D)** Ti_1GaO/Si MOSCAPs. The lines are the fitting results and symbols are the experimental data.

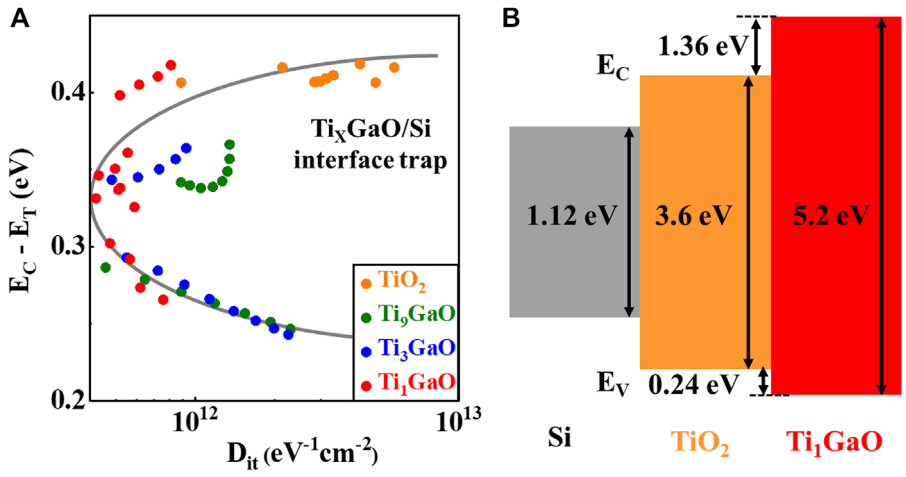

FIGURE 7
(A) Extracted D_{it} as a function of the trap energy level relative to the conduction band of Si (E_C-E_T) for TiO_2/Si and TixGaO/Si MOSCAPs. A "U-shape" profile of interface trap can be observed and the differences of D_{it} values between TixGaO/Si MOSCAPs are not pronounced. **(B)** Band alignment of Si, TiO_2, and Ti_1GaO, where the leakage current reduction could be due to the amorphization of TiO_2 and the enlarged band-offset upon Ga incorporation.

Data availability statement

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

Author contributions

QS: Formal Analysis, Writing–original draft. YnL: Formal Analysis, Validation, Writing–original draft. CH: Data curation, Writing–review and editing. ZY: Data curation, Validation, Writing–review and editing. YgL: Data curation, Validation, Writing–review and editing. YZ: Project administration, Supervision, Writing–review and editing. WY: Project administration, Supervision, Writing–review and editing. JZ: Funding acquisition, Project administration, Writing–original draft, Writing–review and editing.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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