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Ternary Logics Based on 2D Ferroelectric-Incorporated 2D Semiconductor Field Effect Transistors

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Ternary logic has been proven to carry an information ratio 1.58 times that of binary logic and is capable to reduce circuit interconnections and complexity of operations. However, the excessive transistor count of ternary logic gates has impeded their industry applications for decades. With the modulation of the ferroelectric negative capacitance (NC) properties on the channel potential, MOSFETs show many novel features including steep subthreshold swing and non-saturation output characteristics, based on which an ultra-compact ternary inverter can be achieved. Compared with traditional bulk materials, layered 2D materials and 2D ferroelectrics provide a clean interface and better electrostatic control and reliability. Even though ultra-low SS (~10 mV/dec) has been experimentally demonstrated in ferroelectric-negative capacitance-incorporated 2D semiconductor (NC2D) FETs, the available models are still rare for large-scale circuit simulations. In this study, the superb electrical properties of pure 2D material stack-based NC2D FETs (layered $CuInP_2S_6$ adopted as the 2D ferroelectric layer) are investigated through device modeling based on the Landau–Khalatnikov (LK) equations in HSPICE. We managed to realize an ultra-compact ternary inverter with one NC2D-PMOS (WSe_2) and one NC2D-NMOS (MoS_2) in HSPICE simulations, whose transistor count is significantly reduced compared with other counterparts. We also proposed a novel input waveform scheme to solve the hysteresis problem caused by ferroelectric modulation to avoid logic confusion. Additionally, the power consumption and propagation delay of the NC2D-based ternary inverter are also investigated. This work may provide some insights into the design and applications of ferroelectric-incorporated 2D semiconductor devices.

Keywords: ternary logics, 2D semiconductors, ferroelectrics, negative capacitance, device modeling

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INTRODUCTION

Two-dimensional semiconductors including graphene and transition metal dichalcogenides (TMDs) have gained tremendous research interest due to their atomically thin monolayers, which enable better electrostatic control and aggressive scaling capability when adopted as a channel material in future field-effect transistor (FET) fabrication (Radisavljevic et al., 2011; Desai et al., 2016). However, it is still hard to achieve a sub 60 mV/dec subthreshold swing (SS) without incorporating extra gate

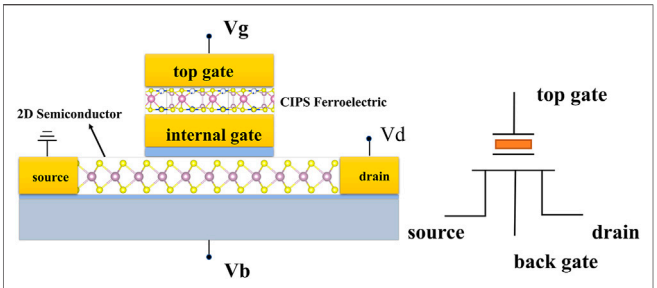

FIGURE 1 | Structure and circuit symbol of the NC2D FET. 2D CIPS is adopted in the top gate stack as the ferroelectric negative capacitance layer.

stack modulation due to the so-called Boltzmann tyranny (Salahuddin and Datta, 2008; Taur and Ning, 2013).

Owing to the negative capacitance (NC) features of ferroelectrics, ultra-steep SS has been demonstrated on both silicon-based and 2D-based FETs by incorporating a ferroelectric layer such as hafnium zirconium oxide $Hf_{0.5}Zr_{0.5}O_2$ (HZO) or P(VDF-TrFE) polymer (McGuire et al., 2016; McGuire et al., 2017; Si et al., 2017). By eliminating the interface traps caused by dangling bonds and charged impurities, layered ferroelectrics $CuInP_2S_6$ (CIPS) with atomically flat surfaces may offer superior performance and reliability for NC-FETs as compared to bulk ferroelectrics. Recently, a low SS (sub 30 mV/dec) has been achieved in CIPS-based NC2D FET, which will further reduce the power consumption during logic state transition. Thus, it will facilitate its industry applications such as logic and memory devices (Si et al., 2018; Wang et al., 2019; Wang et al., 2021).

To analyze the operation principles of NC2D devices and to build up high-level circuit simulation, SPICE models are highly in demand. However, the available result for NC2D modeling, especially the CIPS-based NC2D FET model, is quite rare. In this work, customized compact Verilog-A models based on the time-dependent LK equations have been established for the CIPS-based NC2D FETs and validated with experimental data. By tuning the parameter associated with the MOS capacitance and negative capacitance of the ferroelectric layer, the model is compatible with different sets of LK coefficients, which can be extracted from experimental electric field-polarization (EP) tests. Several NC2D FET features including ultra-steep SS, drain voltage–induced negative differential resistance, and internal gate voltage amplification have been explored and discussed. Additionally, with the availability of the NC2D FET compact models, an ultra-compact ternary inverter with the same structure as its CMOS binary counterpart has been demonstrated and analyzed through HSPICE simulation.

COMPACT MODELING AND ANALYSIS OF NC2D FETS

Modeling Methodology and Flow

In this study, the NC2D FET adopts a purely 2D material-based metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure, in which the 2D ferroelectric $CuInP_2S_6$ (CIPS) was added to the gate stack in a conventional 2D semiconductor FET structure (**Figure 1**). The NC2D FET compact model was established by solving charge and potential equilibrium equations between the ferroelectric layer and the channel of the baseline FET self-consistently in HSPICE, as shown in **Figure 2A**.

The ferroelectric layer was modeled as a capacitor whose charge and voltage dependence relation were defined by the time-dependent LK equation (Lo, 2003; Salahuddin and Datta, 2008; Aziz et al., 2016) given as follows:

$$E = \frac{V_{FE}}{T_{FE}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho\frac{dP}{dt}, \quad (1)$$

$$V_{FE} = T_{FE}\left(2\alpha\frac{Q_{FE}}{A_{FE}} + 4\beta\frac{Q_{FE}^3}{A_{FE}^3} + 6\gamma\frac{Q_{FE}^5}{A_{FE}^5}\right) + \rho\frac{T_{FE}}{A_{FE}}\frac{dQ_{FE}}{dt}, \quad (2)$$

$$P = \frac{(Q_{FE} - \varepsilon_0 E_{FE})}{A_{FE}}. \quad (3)$$

Here, T_{FE}, Q_{FE}, A_{FE}, E_{FE}, and P are the thickness, charge, area size, electrical field, and polarization of ferroelectrics, respectively. The ferroelectric charge can be further considered as polarization (P) multiplied with the ferroelectric area (A_{FE}) P* A_{FE} by neglecting the minor term ε_0 *E_{FE} from Equation. (3). It should be noted that α, β, and γ are LK coefficients that can be extracted from experimental tests of the ferroelectric. ρ is the kinetic coefficient, and the value can be calculated by considering the polarization switching time ~200 ps (Li et al., 2004). For pure 2D MFMIS NC2D modeling, CIPS is used as the ferroelectric layer. **Figure 2B** shows LK coefficient extraction from the polarization vs. electrical field polarization (EP) test curve of CIPS (Si et al., 2018). The extracted α = −6.59E10 cm/F, β = 6.21E21 $cm^2/F/C^2$, and γ = 1.15E11 $cm^9/F/C^4$ will later be used in the modeling framework and circuit simulations.

Simulation Results and Discussion

Figure 2C shows the comparison of the simulated transfer characteristics of the MoS_2 FET with and without the ferroelectric CIPS stack incorporation. Similar to the experimental demonstrations of both bulk and 2D semiconductors, the overall current level of the NC2D devices is improved due to the internal voltage amplification compared with the underlying transistor without the ferroelectric stack. This can be explained based on the principle $V_i = V_g - V_{FE}$ (Huang et al., 2020). When the FET works in the second and third quadrant of the ferroelectric S curve (also known as the negative capacitance region due to the reverse relation between charge and voltage), the CIPS layer voltage will be negative, which makes the underlying internal gate voltage to be larger than the applied top gate voltage. It is worth mentioning that when zero top gate voltage is applied, the FET will operate in the first and fourth quadrant, where CIPS layer voltage V_{FE} will be positive and the underlying internal gate voltage V_i be negative. This will further depress the off-state current; thus the on/off ratio of NC2D FETs will be improved.

In a typical silicon FET, SS can be mathematically described as follows:

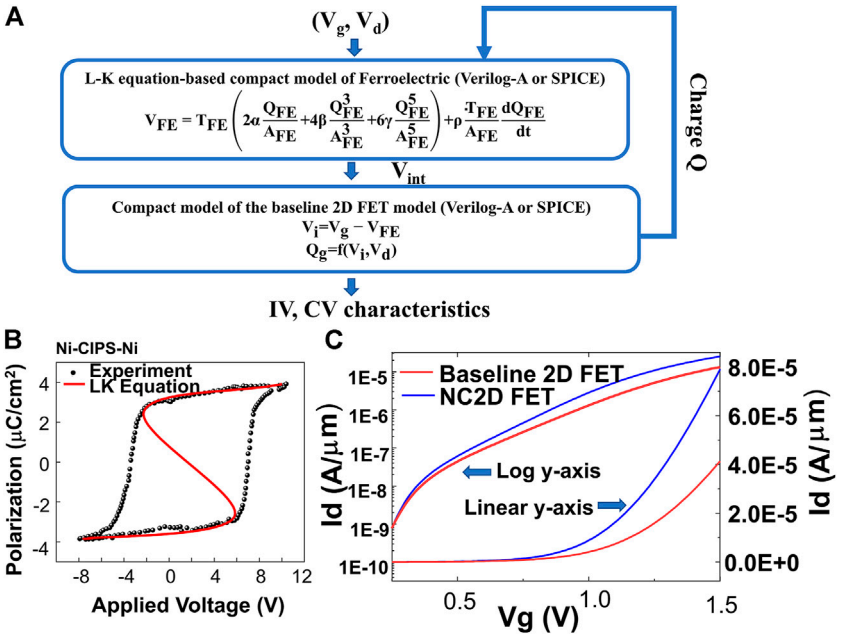

FIGURE 2 | Device modeling method of the NC2D FET. **(A)** Modeling flow of the NC2D FETs. **(B)** LK coefficient extraction from the previous EP test of the 2D CIPS ferroelectric, α = −6.59E10 cm/F, β = 6.21E21 cm^2/F/C^2, and γ = 1.15E11 cm^9/F/C^4. **(C)** Transfer characteristic comparison between the 2D FETs with/without CIPS incorporation with log *y*-axis in the left and linear *y*-axis in the right.

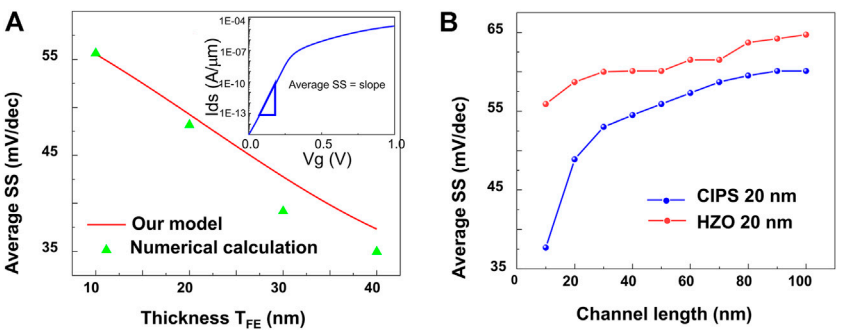

FIGURE 3 | Average subthreshold swing results and comparisons. The average SS is defined and determined by extracting the slope of transfer characteristic over the whole subthreshold region in this work. **(A)** Average SS of the NC2D FETs with varying ferroelectric layer thickness. The red line is our established model, and the green dots are the numerical calculations of previous works. **(B)** Average SS along with channel length scaling with 20 nm CIPS and 20 nm HZO incorporation.

$$SS = \ln(10)\frac{kT}{q}\left(1 + \frac{C_{MOS}}{C_{ox}}\right), \quad (4)$$

where C_{MOS} is the MOSFET gate capacitance, and C_{ox} is the gate dielectric capacitance (Wouters et al., 1990). Typically, positive C_{MOS} and C_{ox} will result in SS being always larger than the Boltzmann limit: 60 mV/dec ($\ln(10)\frac{kT}{q}$) (Beckers et al., 2020). However, with the incorporation of negative capacitance into the gate stack, SS can be decreased to sub-60 mV/dec or even sub-5 mV/dec (Li et al., 2015; Lee et al., 2018). 2D semiconductor FETs will also see a tremendous improvement in subthreshold swing with the incorporation of a negative capacitance ferroelectric layer. A record low SS of 4.97 mV/dec has recently been demonstrated in MoS_2 MOFFT with the $LiNbO_3$ layer incorporated into the back gate dielectric (Wang et al., 2020).

In this work, we also investigated the dependence of SS improvement of NC2D FETs on the thickness of CIPS. The average SS is defined and determined by extracting the slope of the I_dV_g curve over the whole subthreshold region in this work, as shown in the inset in **Figure 3A**. **Figure 3A** shows the simulated results compared with the numerical calculation of SS with a ferroelectric layer of different thicknesses. It is obvious that as the thickness increases, SS tends to decrease, speeding up the transistor on/off transition rate. This is mainly due to the capacitance matching between the negative capacitance and

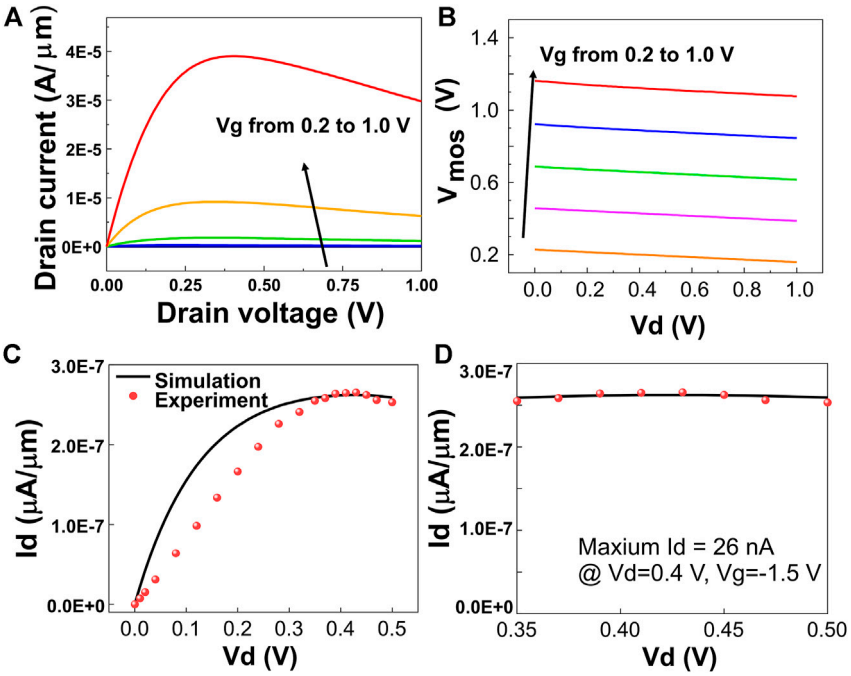

FIGURE 4 | NDR effect in device modeling. **(A)** NDR effects in the simulated output characteristics of NC2D FETs under different gate voltages. **(B)** Simulated underlying MOSFET gate voltage V_{MOS} (internal voltage); the same color means under the same condition with **(A)**. **(C)** Simulated NDR effect against the experimental measurement of CIPS incorporated NC2D FETs. **(D)** Simulation results against experiments in the NDR region.

the MOS capacitance. With increasing thickness, the absolute value of negative capacitance will decrease, which also increases the absolute value of $\frac{C_{MOS}}{C_{ox}}$, and SS will, therefore, decrease accordingly.

In order to show the superiority of the CIPS ferroelectric compared with traditional HZO, we presented the average SS of NCFET by incorporating the two kinds of ferroelectrics. The dependence of the average SS on different channel lengths with 20 nm CPIS and HZO incorporation is presented in **Figure 3B**. Based on the simulations, CIPS shows better SS improvement than HZO [LK coefficients of HZO are from (Jiang et al., 2018)] of the same thickness. This is due to the fact that based on the extracted LK coefficients, the CIPS ferroelectric will have better capacitance matching with the underlying MOSFET gate capacitance than HZO. Another intriguing phenomenon shown in **Figure 3B** is that the average SS will decrease with the decrease in the channel length, which is quite different from conventional transistors. A similar finding has been demonstrated in experiments by Wang et al. (2020). Such an effect can be explained as follows: with the decrease in the channel length, the drain terminal capacitive coupling effect will become larger, resulting in larger C_{MOS} and a smaller difference between Cox and C_{MOS} (Kwon et al., 2018). These emerging effects indicate a promising advancement of negative capacitance in semiconductor industry applications, which have been limited by the difficulties in turning off the current (the main roadblock of transistor scaling) and keeping Moore's law effective.

Drain voltage-induced negative differential resistance (NDR) is a distinctive phenomenon of NC FETs (Zhou et al., 2018; Alam et al., 2019). Drain current will decrease with drain voltage if NDR happens, which is quite different from the traditional drain field-induced potential barrier lowering effect (DIBL). NDR happens due to the drain voltage coupling effect:

$$\xi_D = \frac{C_{GD}}{C_{FE} + C_{MOS}}, \tag{5}$$

where C_{GD}, C_{FE} and C_{MOS} are the gate-to-drain capacitance, ferroelectric capacitance, and underlying MOSFET gate capacitance, respectively (Jin et al., 2020). In traditional MOSFET, the drain coupling factor ξ_D can be neglected due to $C_{MOS} \gg C_{GD}$. With the incorporation of negative capacitance and the absolute value of C_{FE} larger than that of C_{MOS}, ξ_D will be negative, which will decrease the internal gate voltage (V_{MOS}) of the channel area (as shown in our simulation results in **Figures 4A,B**). By matching the capacitance between the ferroelectric layer and the underline MOSFET, ξ_D can be adjusted while the NDR effect can be tuned and applied to some potential applications.

Recently, the NDR effect has also been observed in CIPS-based NC2D FETs (Ye, 2018). In this work, we have also tried to simulate and engineer the NDR effect in our model. In **Figure 4C**, the simulated output curve in which NDR happens when $V_d >$ 0.4 V is validated against the experimental data (Wang et al., 2019). The same device structure is adopted. For simplicity, we treated graphene as metal in our simulation, which was used to fabricate the internal gate in their work. Our model fits well with the experimental data within the NDR region. The discrepancies between the simulation curve and experiment in the low drain

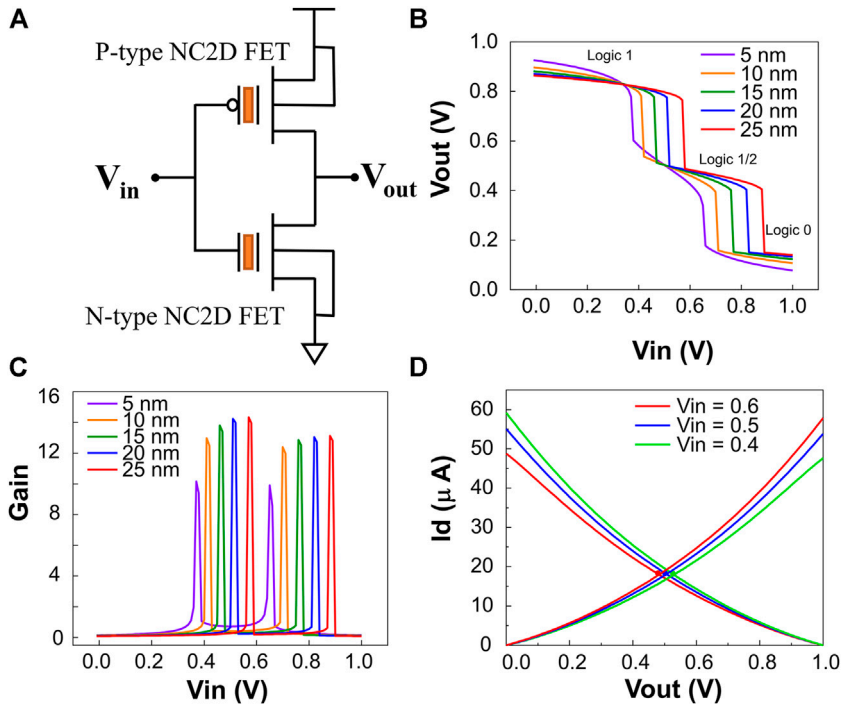

FIGURE 5 | Ultra-compact ternary inverter based on NC2D FETs. **(A)** Schematic representation of the simulated ultra-compact ternary inverter. **(B)** VTC of the ternary inverter with CIPS of different thicknesses. **(C)** DC gain of the ternary inverter. **(D)**. Load-line analysis of the ternary inverter.

voltage region are believed to be caused by voltage division on the contact, which will delay the saturation effect and lower the overall current level. Additionally, the irregularly shaped physical geometries of the fabricated devices may also account for such discrepancies.

Circuit Simulations and Ternary Inverter

The ternary logic system carries an information ratio 1.58 times that of its binary counterpart and is possible to reduce the circuit complexity, chip area, and increase the processing rate (Hurst, 1984; Wu and Prosser, 1990; Vudadha and Srinivas, 2018; Huang et al., 2019). However, the traditional realization of ternary logics suffers from the exceeding number of transistors or resistors, which severely offsets its superiority (da Silva et al., 2006). In 2017, an inverter based on ferroelectric FETs generated a gain-loss region in the voltage transfer curve (VTC) (Gupta et al., 2017). By utilizing this property and further adjusting the capacitance matching, we can achieve a ternary inverter with the same structure as its CMOS binary counterpart.

Structure and DC Simulations

Based on the established n-type and p-type CIPS NC2D FET Verilog-A compact models, we have demonstrated a standard ternary inverter with an ultra-compact structure in HSPICE. The basic schematic representation is shown in **Figure 5A**, where MoS_2 and WSe_2 are chosen as the n-type and p-type semiconductors, respectively. **Figure 5B** shows the VTC simulation results of the NC2D-based ternary inverter incorporated with different thicknesses of the ferroelectric layer (5, 10, 15, 20, and 25 nm). An intermediate state of 0.5 V appears distinctly when the input voltage is over 0.4 V with a supply voltage of 1.0 V. With the thickness of CIPS increasing, both 1→1/2 and 1/2→0 logic level transition points will shift right. This is also reflected in the DC gain of the ternary inverter presented in **Figure 5C**. The DC gain curves are obtained by the derivative dV_{out}/dV_{in}. For a given DC curve, the first peak corresponds to 1→1/2 logic level transition, and the second peak corresponds to 1/2→0 logic level transition. As can be seen in **Figure 5C**, with increasing thickness, the peak of the gain curve will shift right with larger amplitude. A larger DC gain is usually expected, which means a narrower logic level transition zone will help reduce the dynamic power consumption. Also, the voltage gain of the inverter will increase with its thickness, which indicates an improvement in the logic level transition rate and noise margin. Our further load-line analysis presented in **Figure 5D** indicates that the middle state is generated due to intersections of the transistor IV curves under the same input voltage (operation points) in the middle region. The underlying reasons are the non-saturation and aggregation effects of the NC2D FET transfer characteristic, which are due to the internal gate voltage amplification caused by CIPS ferroelectric modulations.

Hysteresis Solution and Transient Analysis

Hysteresis is observed in the dual DC sweep of the ternary inverter, as shown in **Figure 6A**. **Figure 6B** shows the load-line analysis of the proposed ternary inverter. The IV curve in the left branch from 0 to 1 V is the output characteristic of the n-type

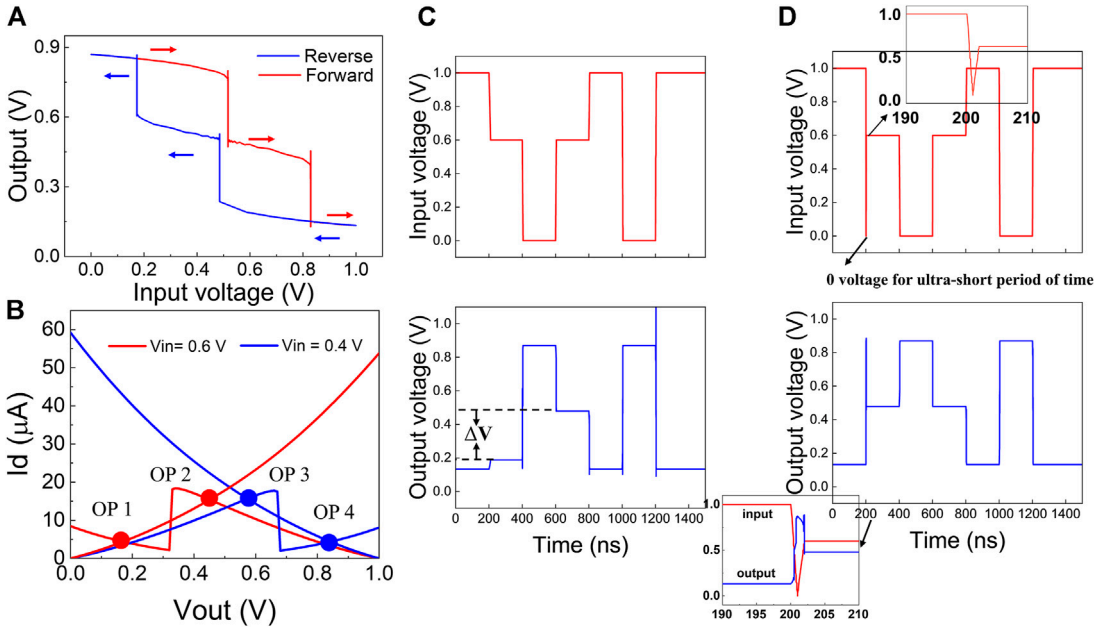

FIGURE 6 | Analysis and solution to the hysteresis problem. **(A)** Dual DC sweep of the NC2D-based ternary inverter. **(B)** Load-line analysis of the hysteresis of the ternary inverter. **(C)** Transient simulations of the NC2D-based ternary inverter using the traditional input waveform. **(D)**. Transient simulations of the NC2D-based ternary inverter using the new input waveform scheme. The aforementioned inset is the zoom-in details of the added negative pulse. The following inset shows the zoom-in rise and fall details when the inverter crosses the hysteresis region at around 200 ns (0–1 logic level transition).

NC2D FET, while the IV curve in the right branch from 1 to 0 V is the output characteristic of the p-type NC2D FET. The same color represents the IV curves under the same input voltage, and the cross points are the corresponding operation points (OP), whose *x*-axis value will generate the output of the ternary inverter. The reason for the generation of the hysteresis can be explained as follows: for a given input voltage, the ternary inverter actually has one different operation point during the forward and reverse sweep due to the NDR effect of the NC2D FETs. Considering 0.6 V input voltage as an example, under the forward sweep condition (sweep input voltage from 0 to 1 V), the operation point is OP2, generating 0.5 V output voltage; however, in the reverse sweep condition (sweep input voltage from 1 to 0 V), the operation point is OP1, generating 0.15 V output voltage. Similarly, when the input voltage is 0.4 V, the operation points will be OP4 in the forward sweep but OP3 in the reverse sweep, generating different output voltages.

We further performed transient analysis to investigate the propagation delay and power consumption of the proposed ternary inverter. For the transient simulations, 25 nm CIPS is chosen to guarantee the inverter to have a middle state at around 0.5 V with a 0.6 V input signal. We used a piecewise linear waveform as the stimulus, and the switch between states takes 5.0 ns. Different from the binary inverter, the ternary input waveform should cover much more transition conditions: (0 → 1/2, 1/2→1, 1→1/2, 1/2→0, 0→1, and 1→0). As shown in **Figure 6C**, the red waveform used as the input signal covers all the logic level transition conditions. The blue waveform is the corresponding output of the ternary inverter. Both the high and low input logic levels are correctly mapped into low and high output logic levels, respectively. However, owing to the hysteresis effect mentioned earlier, the output middle logic levels are not balanced under different transition conditions. In order to solve the hysteresis problem and avoid logic confusion in the functional ternary systems, we proposed a novel input waveform scheme, as shown in **Figure 6D** (red waveform). The main idea is to adjust the input waveform during which the hysteresis will occur, that is, 1→1/2 transition condition. We reprogrammed the input waveform to apply 0 voltage for a significantly short period of time (0.1 ns) just before the logic transition from 1 to 1/2 occurs (details shown in the inset before **Figure 6D**). A pulse duration of 0.1 ns is determined by the highest ferroelectric switch time reported in Li et al. (2004). It should be noted that this work only demonstrates a prototype ideal of using such a method to solve the hysteresis problem. A larger negative pulse amplitude or longer duration time will be needed if the ferroelectric operation frequency is lower. The nanosecond of 0 voltage facilitates the input waveform to cross the hysteresis region swiftly and will have no effect on the logic output. The red waveform in **Figure 6D** shows the corresponding output with a clear output middle state under the new input waveform scheme. The inset below **Figure 6D** shows the zoom-in rise and fall details when the inverter crosses the hysteresis region at around 200 ns (0–1 logic level transition).

We have also measured the power consumption and propagation delay using the inbuilt modules in HSPICE. The methodology used in CMOS binary inverter analysis is adopted in our calculations (Calhoun et al., 2008). Moreover, all the different

logic transition conditions are considered. The maximum delay is measured to be 1.96 ns during the 1→1/2 transition, which can be easily understood due to the adjustment that we have made to get the new input waveform scheme. The average power consumption is measured to be 8.0957 uW. Therefore, the power–delay product (PDP) is 15.87 fJ, which is close to the standard CMOS binary inverters and a promising candidate for future industrial applications.

CONCLUSION

In this study, CIPS-based NC2D FET Verilog-A compact models have been established and validated on the experimental data. Some of the feature effects observed in experiments including SS improvement, NDR, and current level improvement have been analyzed and repeated in our models. An ultra-compact ternary inverter has been successfully demonstrated based on pure 2D MFMIS structures through HSPICE simulations, whose intermediate state can be tuned by adjusting the ferroelectric thickness. We have also proposed a novel input waveform scheme to solve the hysteresis problem, which may cause severe logic confusion in ferroelectric-based logic systems. In addition, some critical parameters including power consumption, propagation delay, and PDP are investigated and compared. We believe this work will shed light on the future applications of 2D ferroelectric-incorporated 2D semiconductors, especially in the realization of ternary logics and other low-power circuit designs.

DATA AVAILABILITY STATEMENT

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

AUTHOR CONTRIBUTIONS

BT, MH, and GZ conceived and designed the project. GZ established the compact model. GZ and NH performed the DC and transient analysis of the ternary logic gates. XW was responsible for collecting the experimental data. The article was written by GZ and revised by WY, XW, and PC.

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