frontiers in
MATERIALS

PERSPECTIVE ARTICLE
published: 08 December 2014
doi: 10.3389/fmats.2014.00030

Peculiarities of the interface between high-permittivity dielectrics and semiconductors

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Replacement of the silicon dioxide thin films in metal-oxide-semiconductor structures for microelectronics with high-permittivity dielectrics (high-*k*) is a crucial step in the further down-scaling of microelectronic devices. Technological development of the fabrication processes and better theoretical understanding of the physical phenomena in the considered structures are demanded simultaneously. Important issues concerning high-*k* are discussed in this paper and directions for further development are indicated. Further progress also requires better understanding of the physical phenomena appearing in stacked high-*k*/interfacial layer dielectrics.

Keywords: high-*k* dielectrics, metal-oxide-semiconductor structures, tunneling, band offsets, permittivity

SILICON DIOXIDE THIN FILMS

Interfaces in electron devices are part of their basic structure. Functioning of such devices is inseparably connected to the presence of different interfaces. Of particular importance are metal-oxide-semiconductor (MOS) structures, where two conductive materials (metal and semiconductor) are separated by a thin dielectric layer.

Over decades, silicon dioxide has been used as a unique solution for insulating material of MOS structures due to its outstanding properties, such as exceptionally low-defect density and high band offsets both for electrons and holes.

A particular advantage of this material is the possibility to grow silicon dioxide films by oxidation of the silicon substrate itself, thus, avoiding complicated deposition processes. Simultaneously, this fabrication method ensures excellent match of the dielectric layer with the substrate, ensuring low density of defects at the insulator/semiconductor contact.

Nevertheless, there is a thin region near the semiconductor substrate containing several types of imperfections. Densities of these defects are substantially lower then in structures containing other dielectric materials. The region close to the substrate possessing different properties different from those of the bulk is referred to as interfacial layer. The notion of the interfacial layer has undergone substantial alteration since its initial introduction. In the early stage, the interfacial layer was considered a region in the oxide about 10 nm thick, in which mechanical strains (interface constraints) between the two materials are present (Jaccodine and Schlegel, 1966; Boyd and Wilson, 1987). Substantial deviations from the SiO_2 stoichiometry are present in a region about 1 nm thick (Nakazawa et al., 1989). Using scanning tunneling microscopy and spectroscopy, an interfacial transitional region about 0.9 nm thick has been found, in which the silicon oxide surface band gap increases gradually with thickness (Xue et al., 2007). Variations of the bandgap in the substrate are limited to about 0.3 nm. *Ab initio* studies show that both the optical and the static dielectric constants change abruptly in the vicinity of the SiO_2/Si interface, while the energy gap changes gradually on the SiO_2 side (Wakui et al., 2007). Therefore, the presence of a layer about 1 nm thick (about three monoatomic layers), having properties different that the bulk SiO_2 is to be taken into consideration when studying MOS structures. Such a thin layer also plays a crucial role in the modification of the properties of SiO_2/Si interface with nitridation (Mi et al., 1993; Novkovski, 1999), which is found to be an important method for improvement of electrical and reliability properties of metal/SiO_2/Si structures (Dutoit et al., 1994).

HIGH-*k* DIELECTRICS

Progressive down-scaling of the microelectronic devices leads to ultimate decrease of the thickness of the dielectric in MOS structures. Even if introducing the improvements with various technological procedures such as the nitridation, the use of silicon dioxide as dielectric is limited (Novkovski and Atanassova, 2006). Dielectrics with high-relative permittivity (high-*k*) (Al_2O_3, Ta_2O_5, $SrTiO_3$, TiO_2, ZrO_2, HfO_2, La_2O_3, Lu_2O_3, Sc_2O_3, Dy_2O_3, Y_2O_3, etc.) and their pseudobinary alloys are studied as a replacement of the silicon dioxide for various microelectronics applications (Wilk et al., 2001; Houssa et al., 2006; Wong and Iwai, 2006; Kittl et al., 2009). The main advantage of high-*k* dielectrics compared to silicon dioxide is the possibility to obtain the same capacitance with a larger physical thickness (d) of the dielectric layer and thus to reduce the leakage due to direct tunneling occurring in ultrathin SiO_2 (thinner than 2 nm). Nevertheless, high-*k* dielectrics have lower heights of tunneling barriers (band offsets, Φ), which leads to a somewhat lower benefit from the replacement of the SiO_2 with high-*k*. A real measure of the gain in reducing leakage due to

direct tunneling is roughly given by the ratio of product $\Phi \cdot d$ for the considered materials. For example, band offset for electrons at the W/SiO_2 interface is $\Phi_e = 3.45$ eV, while at the W/Ta_2O_5 interface it is $\Phi_e = 0.55$ eV (Novkovski, 2006). Relative permittivity for SiO_2 is 3.9 while for Ta_2O_5 it is about 40 (Kittl et al., 2009), and hence the same capacitance with Ta_2O_5 as dielectric will be obtained with 10 times bigger physical thickness of the high-*k* dielectric than with SiO_2. Although the benefit is diminished with the decrease of band offset (by a factor of six), it is still rather important; the capacitance can be doubled at the same level of leakage current.

The above approach is straightforwardly applicable in the case of metal-insulator-metal (MIM) structures. In the case of high-*k* deposited on semiconductor, during the formation of the high-*k* layer, however, an interfacial SiO_2-containing layer is inevitably formed at the Si substrate (Alers et al., 1998). This interfacial layer substantially modifies properties of MOS structures and hence it deserves particular attention.

ROLE OF THE INTERFACIAL LAYER

Several authors consider the interfacial layer as unwanted, and they propose different solutions for its reduction or elimination (Engstrom et al., 2012). Indeed, due to the lower permittivity of the interfacial layer than that of the bulk high-*k*, the capacitance of the stack high-*k*/interfacial layer is lower than that of a high-*k* single layer with the same total physical thickness.

Many factors determine the interfacial layer thickness. For example, interfacial layer thickness is found to be dependent on the gate material (Novkovski, 2006; Park et al., 2014). Detailed list of the factors determining the interfacial layer thickness and composition has to be a part of the future investigations. Several processes are proposed for thickness control. Interfacial thickness can be reduced to some tenths of a nanometer or even eliminated by certain technological processes; however, excessive application of these processes leads to a formation of silicides (Xiuyan et al., 2014). A kind of natural thickness saturation is perceptible in some cases. For example, in the case of Ta_2O_5 on Si, after oxygen anneals values of about 3 nm are obtained (Lau, 2012). These values are close to the values for the case of Ta_2O_5 films grown by thermal oxidation of Ta (Karmakov et al., 2012).

Although the interfacial layer degrades significantly the MOS structure capacitance, it has rather important beneficial effects. The presence of such an ultrathin layer substantially modifies the band offsets. It has been shown that in metal-Ta_2O_5/SiO_2-Si structures leakage current is limited by injection of electrons from the substrate at positive gate (band offset 3.15 eV) and with the injection of the holes from the substrate at negative gate polarity (band offset 4.7 eV) (Novkovski and Atanassova, 2004). Thus, the band offsets of the stacked layer attain significantly higher values than these for high-*k* itself, leading to substantial reduction of the leakage current. As a result, combining interfacial layer and high-*k* dielectric, low leakage simultaneously with high capacitance can be obtained, leading to rather low-equivalent oxide thickness at acceptable level of leakage current for further generations of integrated circuits. Besides, the presence of an interfacial SiO_2 layer allows maintaining the density of interface states at acceptably low level (Yang et al., 2012; Litta et al., 2014).

Possibilities of decrease of the equivalent oxide thickness by reducing the interfacial layer are limited, since subsequent processes at higher temperature cause additional growth of the layer. Better solution for decreasing the equivalent oxide thickness is the nitridation of the interfacial layer; nitridation increases the dielectric premittivity of this layer and hence decreases the equivalent oxide thickness of the entire stack. Various nitridation processes are introduced to improve the stacked dielectric layer properties (Houng et al., 2001). The main advantage of these processes is the increase of the interfacial layer permittivity (oxynitride) leading to decreased equivalent oxide thickness (Novkovski and Atanassova, 2005). However, a decrease of band offsets diminishes the positive effect of the nitridation. Therefore, optimum conditions for fabrication of dielectric stacks are to be identified in order to benefit at maximum from the nitridation process (Novkovski, 2009). Additionally, nitridation improves the dielectric integrity of the stack and hence the reliability of the devices based on it. There are many technological parameters to play with in the search for optimum conditions for a particular process. Further improvements with choosing the right combination of properties of the parts of the stack are to be expected.

Another important issue concerns the choice of the gate metal. Even if the metal gate is not in direct contact with the interfacial layer, in the case of nanosized films, it influences strongly its thickness and properties (Novkovski and Atanassova, 2015).

OPEN ISSUES

Many concepts used in description of silicon dioxide are nowadays used without serious reconsideration for description of high-*k* dielectrics. In some cases, such an approach is justified. However, in certain cases straightforward application of such concepts, measurement methods, and analysis is shown to be misleading, as is the case with the determination of conduction mechanisms (Novkovski, 2007). Therefore, in the future, much more attention is to be paid to the reconsideration of the applicability of the concepts and methods used in the description and prediction of the properties of the MOS structures containing high-permittivity dielectric layer.

Among the methods to be discussed is the determination of the density of the charges in the dielectric. In the considered structures, there are two dielectric materials and three interfaces that can contribute to charge trapping: high-*k* bulk layer, interfacial layer (silicon dioxide, oxynitride, or silicate), metal/high-*k* interface, high-*k*/interfacial layer interface, and the interfacial layer/substrate interface. Various processes of charging and discharging these traps can occur. Standard methods of determination of oxide and interface charges are probably incorrect in many cases; various methods give different results (Miyata, 2012). Very high values of the interface state densities (of the order of $10^{13}\,eV^{-1}cm^{-2}$) at midgap were determined in some cases (Miyata et al., 2014).

In addition, for film thicknesses of the order of 1 nm, some variations in the nature of the conduction mechanism can occur; in tunneling (Fowler–Nordheim, direct and trap assisted) and hopping, as well as in Poole–Frenkel field enhanced emission. Ballistic transport will be important in majority of the cases, since distance to be traveled by electrons emitted from the traps or injected from an electrode is of the order of few atomic radii. Some substantially

new integral quantum mechanical solution for the dielectric stack or the MOS structure is expected to appear. Such a model will not only give further better insight into physical phenomena in high-*k* based MOS structures but is also likely to provide solution without using several suppositions and compromises used in currently accepted methods of description of properties of MOS structures.

Based on above indicated progress lines, new technological solutions have to be developed to provide combinations of high-*k* with appropriate interfacial layers having optimal properties for MOS based microelectronic devices.

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Conflict of Interest Statement: The author declares that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Received: 06 October 2014; accepted: 24 November 2014; published online: 08 December 2014.

Citation: Novkovski N (2014) Peculiarities of the interface between high-permittivity dielectrics and semiconductors. Front. Mater. ***1****:30. doi: 10.3389/fmats.2014.00030*

This article was submitted to Colloidal Materials and Interfaces, a section of the journal Frontiers in Materials.