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# Fault current handling in large-scale MMC-HVDC systems: an improved approach with DC circuit breaker and fault current limiter

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Designing Voltage Source Converter (VSC)-based DC grids presents a significant challenge in providing dependable and cost-effective protection against short-circuit faults. Given the increased vulnerability of high-voltage DC (HVDC) lines to the faults, there is a dire need for enhanced protection equipment capable of effectively handling fault currents. By limiting the rapid increase in fault current, fault current limiters (FCLs) reduce the requirement for complex DC circuit breakers (DCCBs) design in order to isolate faults. This paper presents a novel Hybrid FCL for the protection of large scale VSC-HVDC. It provides a comprehensive analysis of DCCBs and their impact on VSC-HVDC projects with and without FCLs. It further analyses an extensive discussion comparing DCCBs equipped with FCLs to those without FCLs. For simulation analysis, an equivalent circuit modeling approach of the Zhoushan HVDC Project is used to analyze current behavior of FCL-equipped breakers. The paper presents the circuit diagram and operational principles of the proposed FCL. Subsequently, it analyzes the FCL performance with its current limiting features and outlines the parameter design requirements necessary for its implementation. Simulation results utilizing PSCAD/EMTDC are provided to validate various aspects of this research. Further, the performance of the proposed FCL is compared with existing solutions proposed in the literature. From theoretical and simulation validations, it is concluded that DCCBs equipped with FCLs outperform conventional DCCBs without FCLs for higher-rated VSC-HVDC projects.

## KEYWORDS

VSC-HVDC, MMC-HVDC, protection, DCCBs, hybrid CB, FCL

## 1 Introduction

DC transmission is a critical component of modern power systems. It provides a reliable and efficient solution for grid connections, and long-distance power transfer (Kangwa et al., 2017). HVDC grids based on updated technology of VSC, that is modular multilevel converter (MMC), have more benefits than traditional line commutated converter (LCC) and conventional two-level VSC-based HVDC transmission network. These advantages

include independent control of active and reactive power, low-harmonic distortion, ease of forming a multi-terminal DC (MTDC) system, etc., (Zhang et al., 2016). Due to its ability to resolve the issue of integrating large-scale renewable energy sources, the MMC-HVDC grid has gained attention as a center of study in recent years. A significant challenge in developing and expanding DC grids is the low impedance and absence of a zero crossing point in DC fault currents (Yan et al., 2024; Muniappan, 2021). To effectively manage fault currents caused by short circuits, various types of direct current circuit breakers (DCCBs) are considered the most effective solution (Barnes et al., 2020). DC circuit breakers (DCCBs) are categorized into three types: mechanical circuit breakers (MCBs), solid-state circuit breakers (SSCBs), and hybrid circuit breakers (HCBs). Hybrid circuit breakers have garnered increased attention because they combine the advantages of both SSCBs and MCBs. HCB performs quickly like SSCB and has the same low conduction losses as MCB (Huo et al., 2022). In 2012 ABB Grid and ALSTOM Grid developed an HCB that has useful characteristics for fault current isolation (Kolli and Rana, 2024; Nguyen et al., 2016).

However, they face limitations in terms of capacity when it comes to raising the current rating of DC grids. Two potential solutions to address this issue are adding FCLs in series with DCCBs or changing the DCCB's design to allow for high-level fault currents (Mei et al., 2021). The only objective of FCLs in DC grids is to lower the requirements and improve the performance of DCCB. In essence, FCL has two basic functions: it keeps the fault current below a certain threshold and removes faults from the power system. During normal operation, an FCL maintains very low impedance. However, it introduces significant impedance under fault conditions, thereby limiting the increase in fault current within the system.

FCLs improve power grid reliability and stability by suppressing fault currents. When combined with DCCBs, they help protect HVDC lines from high fault currents. While FCLs cannot fully isolate faults, they are effective in limiting them. Modern FCLs remain inactive under normal conditions, making them ideal for high-power, fault-current handling systems. An ideal FCL features low impedance in normal operation, high impedance during faults, fast fault current limitation, automatic activation, and quick recovery. It should also be reliable, safe for operators, and compact for high-power and DC applications. There exist three categories of FCLs: (I) the superconducting FCL (SFCL), (II) the non-superconducting FCL (NSFCL), and hybrid fault current limiters (Zhang et al., 2019; Singh et al., 2022). FCLs can operate as standalone circuits to reduce fault current. Additionally, FCL characteristics can be integrated into breaker designs to achieve fault-current limiting capabilities. In addition to these methods, certain controller-based approaches have also been employed for fault current suppression (Zhang et al., 2020). Among these methods, breaker-based methods are widely regarded as the most reliable option.

Authors in Ruiz et al. (2015) provided an updated review for resistive type SFCLs. They focus on the various methods for numerically modeling their local physical properties and the concepts that have already been tested in experiments. The work presents a comparison of the characteristics and properties of various resistive-type superconducting capacitors (SFCLs) made

of various superconducting materials. Chen et al. (2019) proposes a strategy employing a combination of resistive-type SFCL (RSFCL) and DCCB to protect a multi-terminal DC grid from fault currents. Simulation results illustrate that the RSFCL notably reduces fault current and consequently DCCB requirements during fault scenarios. In Chen et al. (2021) the resistance of the SFCL is adjusted to lower the DCCB requirements and maintain stable and safe operation in the DC network. A concept for the design and analysis of a saturated iron core SFCL is presented in Dao et al. (2020). This study investigates various options for the SI-SFCL's coil system and uses physical experiments to confirm its operating features. The findings from this investigation can help develop large-scale SI-SFCLs for high-voltage direct current (HVDC) power systems. Lee et al. (2018) conducts a comparative analysis among SI-based SFCL, RSFCL, and iron-core SFCL, focusing on their current-limiting and energy dissipation characteristics. The study reveals that the SI-SFCL demonstrates superior performance with notably lower energy dissipation and rapid recovery characteristics during faults. In Didier et al. (2015), a comparative assessment was conducted between inductive and resistive SFCLs, evaluating their effectiveness in current limitation and power system transient stability. The investigation demonstrates the superiority of the resistive SFCL across both domains, showing its enhanced performance in fault current limitation and power system transient stability. However, their use requires high-temperature superconducting materials and an expensive cooling system, thus making them unsuitable for DC grid deployment. A novel arrangement of current-limiting inductors (CLIs) is presented in Li et al. (2019) for use in DC grids. In both normal and fault states, these CLIs are ordered in series and parallel, respectively. This configuration effectively reduces the amplitude of the fault current. However, it simultaneously increases interruption speed and energy dissipation. The authors present a high-inductance DC reactor-based SFCL intended for DC network applications in Heidary et al. (2019). Two coupled inductors with low and high impedance make up this arrangement. To provide a low inductance and reduce power loss, the high-inductance inductor is bypassed under normal operation. Whereas, during fault conditions, it is placed into the fault current path to offer a high inductance path. Notably, the study does not address the DCCB's energy dissipation and interruption speed. Authors in Fu et al. (2020) and Khorasaninejad et al. (2022) introduce mutual inductance (MI) and resistive MI-current limiting circuits to alleviate the demands on DCCBs, as well as to decrease fault current magnitude and interruption speed. However, these circuits exhibit low interruption speed.

Researchers have undertaken numerous investigations into hybrid FCLs aimed at enhancing their fault current suppression capabilities. The hybrid FCL, which combines the advantages of two other topologies, appears to be a promising choice for HVDC transmission systems. Zhu et al. (2020) introduces a new design for a hybrid SFCL incorporating a biased magnetic field, featuring two-stage current limiting capabilities. Experimental findings demonstrate that the current limiting ratio achieves 89.66%, confirming the efficacy of the design and highlighting the potential application of this hybrid SFCL. Jiang et al. (2014) introduces a bridge-type HFCL utilizing MOSFETs and IGBTs to ensure rapid dynamic response. A model rated at 220 V/1 kA was

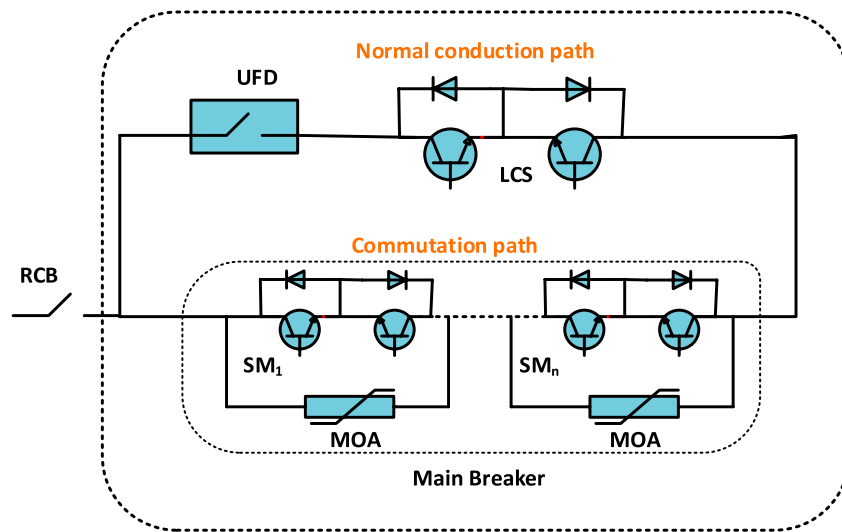


FIGURE 1  
ABB hybrid DCCB (Callavik et al., 2013).

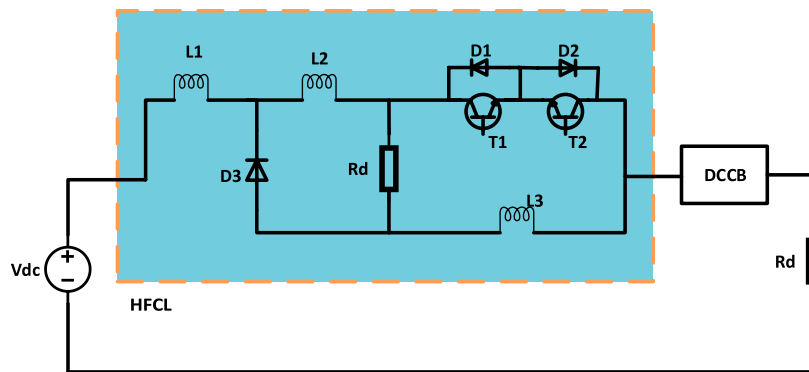


FIGURE 2  
Topology of proposed FCL.

built and tested. The HFCL design effectively limits fault currents in both transient and steady-state conditions. A new hybrid FCL based on a novel theory called the push-pull technique is introduced in Zhang et al. (2019). This FCL aims to enhance current limiting capabilities by mitigating the rate of rise and peak of fault currents. In Yuan et al. (2015), a novel hybrid saturated core type FCL that makes use of permanent magnets and DC coils is presented. The efficiency of the suggested FCL in clipping fault current is illustrated through simulation results. It is mentioned how the value of the limiting reactor affects the performance of FCL. A hybrid fault current limiter using liquid metal for large-scale power systems is developed in Wang et al. (2022). The authors assert that this FCL attains minimal operational losses by utilizing a fast mechanical switch, magnetic induction module, and multiple liquid metal units. Ahmad et al. (2020) introduces an incremental fault current-limiting circuit featuring multiple parallel branches designed to gradually reduce fault current during fault conditions. Each branch within this topology comprises a limiting inductor in series with a bidirectional

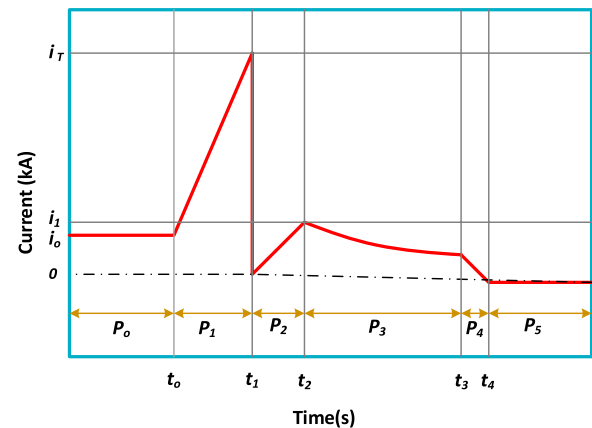


FIGURE 3  
Current-limiting characteristics with FCL.

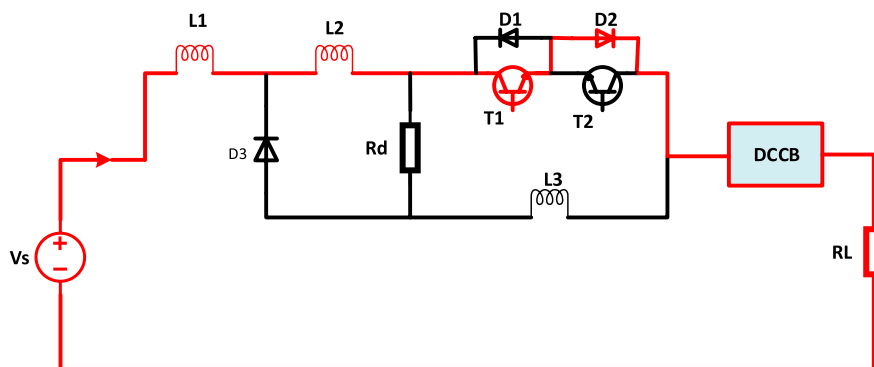


FIGURE 4  
Equivalent circuit for steady-state/normal operation stage.

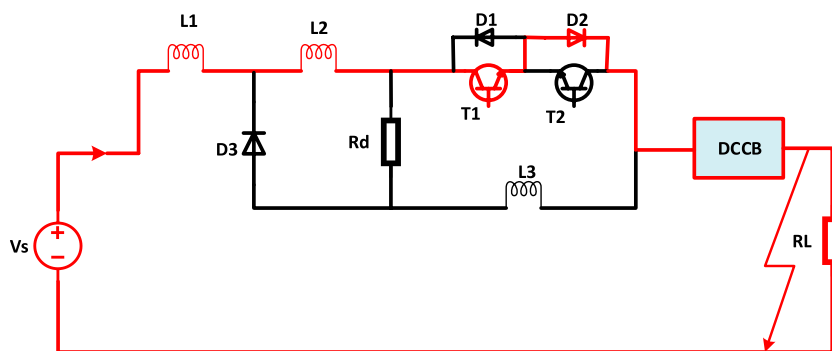


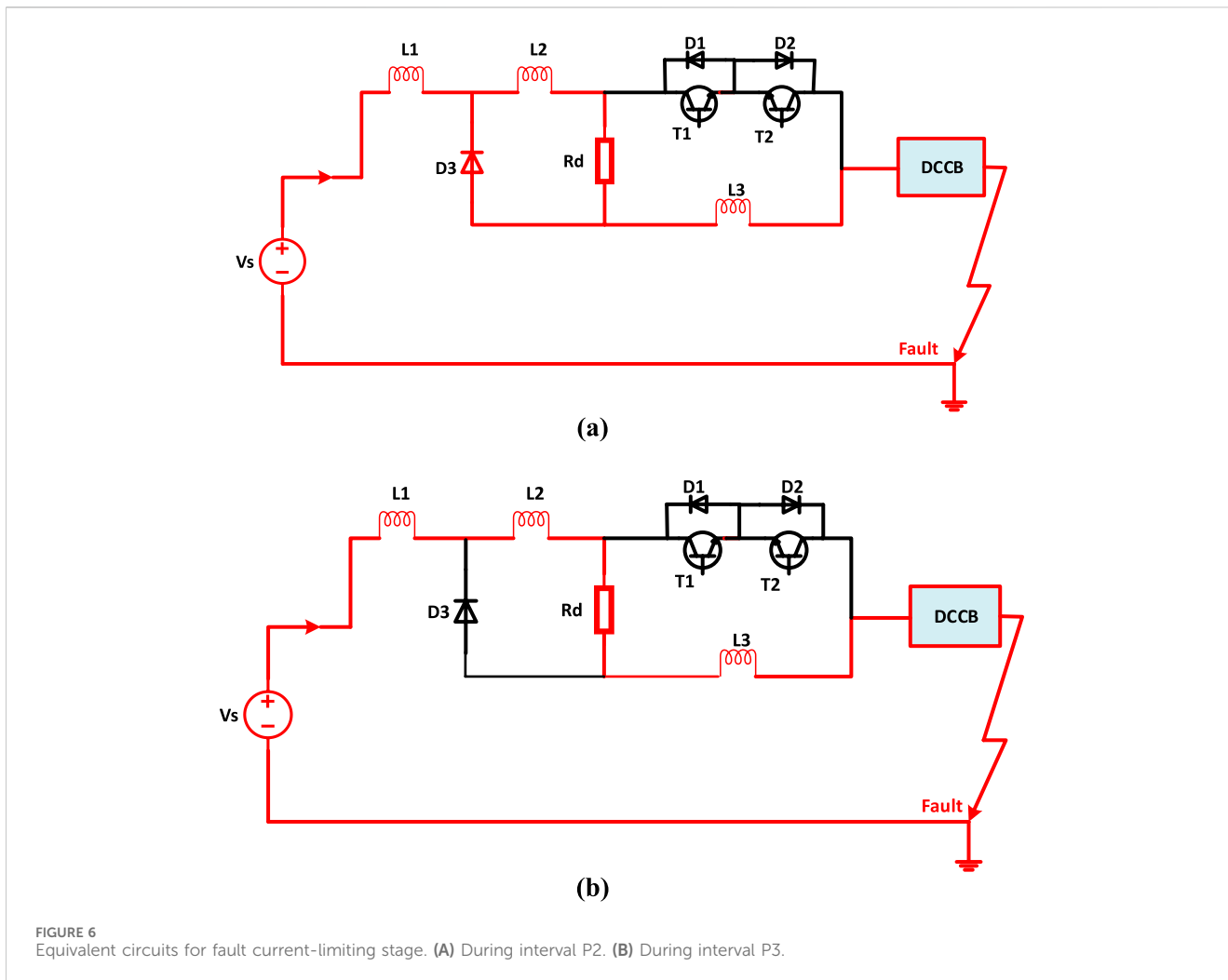
FIGURE 5  
Equivalent circuit for fault raising stage.

switch. A new hybrid superconducting FCL incorporating controlled solid-state component is shown in [Xingguang et al. \(2020\)](#). The results of the simulation show that the suggested hybrid FCL successfully limits fault currents to less than a quarter of a half-cycle even when thyristors are used. Similarly, a new approach to current limitations is presented in [Hamada et al. \(2023\)](#), which uses a capacitor to absorb energy from the commutation circuit during the interruption process in conjunction with a superconducting fault current limiter to reduce short-circuit currents. The results of the experiments demonstrated that the system could isolate errors within a very short period, which was a significantly faster response than other systems that were described in the relevant research.

There are numerous digital circuit breakers available that operate at very high frequencies and provide precise fault current control ([Yin et al., 2022](#)). However, FCL-based breakers offer several advantages over these digital systems. These include superior fault current management, enhanced protection for equipment, and reduced stress on circuit breakers. Additionally, FCL-based breakers support selective coordination, contribute to greater system stability, and seamlessly integrate with existing infrastructure, making them a valuable choice in many electrical applications. They also offer the benefits of lower power loss during

normal operation and reduced electromagnetic interference (EMI). Unlike digital systems that require continuous monitoring and control, FCLs operate passively under normal conditions and only activate under fault conditions. This can result in lower operational complexity and increased reliability.

This paper mainly provides the knowledge and importance of FCLs integrated within DCCBs to efficiently manage short-circuit faults in high-voltage direct current (HVDC) systems with increased ratings. This paper proposes a novel hybrid FCL with a hybrid DCCB to limit the DC fault current while ensuring high interruption speed. It offers a high-impedance path to limit the fault current under a fault condition and a low-impedance path in a steady-state condition. Furthermore, this approach incorporates two freewheeling paths aimed at dissipating the stored energy of limiting inductors through a discharging resistor. This feature limits the fault current and reduces the Metal Oxide Arrester (MOA) energy dissipation, and voltage drop across the DCCB. In short, this FCL provides high interruption speed and significantly reduces the peak of the fault current. It further limits the fault current in the current limiting stage effectively which improves the system stability. Energy absorbed by the breaker is lower with this FCL which reduces the stress on the components. The effectiveness of the proposed approach is evaluated within the PSCAD/EMTDC



software environment under the DC short circuit fault condition. The obtained results are compared with those presented in Ahmad et al. (2022) and Li et al. (2019) to illustrate the effectiveness of the proposed approach. A comparative analysis reveals that the proposed method outperforms both Ahmad et al. (2022) and Li et al. (2019), and demonstrates its superior effectiveness.

## 2 Topology of proposed FCL

### 2.1 ABB'S hybrid DCCB

The first hybrid DCCB was introduced by the ABB Company in 2012. In this setup, the ABB hybrid DCCB is connected in series with the HFCL. The diagram in Figure 1 illustrates the schematic representation of the ABB's HDCB.

The conventional HCB setup typically includes three main components: a residual current breaker (RCB), a load current branch, and a main breaker (MB), as illustrated in Figure 1. The load current branch consists of a series arrangement comprising the ultra-fast disconnecter (UFD) and load commutation switch (LCS). Within the MB, there are multiple Insulated Gate Bipolar Transistor

(IGBT)-based Semiconductor Modules (SMs) connected in series, alongside metal oxide arresters (MOA). In high-voltage applications, it is common for the number of SMs associated in series to be quite high, possibly reaching hundreds. However, this can significantly increase industrial costs. The primary function of the RCB is to physically separate the faulty line once the process of current interruption is complete. When the hybrid CB receives a trip signal from the protection system, it activates the MB while deactivating the LCS. Consequently, fault current begins to flow into the MB (Liu et al., 2023). Once the fault current in the load current branch reaches zero, the UFD initiates the opening process. After it finishes its opening operation, the MB is deactivated, and the fault current is directed to the arresters for dissipation. The main role of the RCB is to physically separate the faulty line once the current interruption process concludes. Upon receiving a trip signal from the protection system, the HCB activates the main breaker (MB) while deactivating the LCS). As a result, fault current starts to flow into the MB. The UFD will initiates the opening process when the current in the load current branch reaches to zero. After completion of opening process of UFD the main breaker will be deactivated and hence the fault current redirected to the MOAs for dissipation.

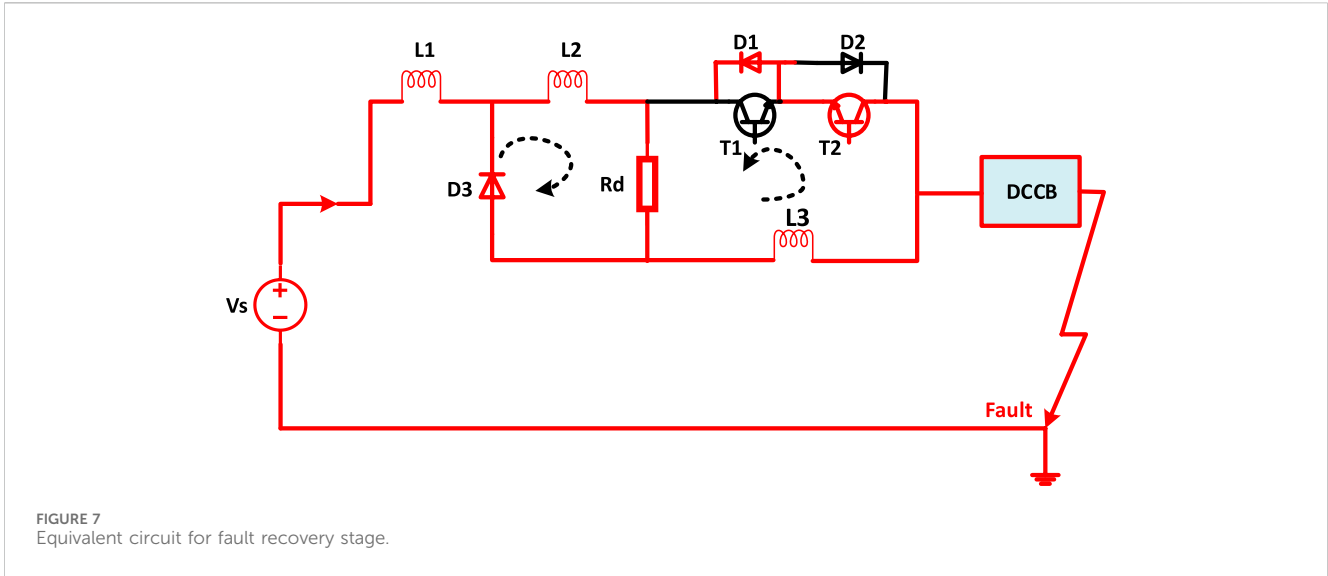


FIGURE 7 Equivalent circuit for fault recovery stage.

## 2.2 Topology of proposed FCL

The proposed FCL Topology is shown in Figure 2.

It comprises one LCS, a discharging resistor (R), a Diode D<sub>3</sub>, and three limiting inductors, L<sub>1</sub>, L<sub>2</sub>, and L<sub>3</sub>. The LCS includes components T<sub>1</sub>, T<sub>2</sub>, D<sub>1</sub>, and D<sub>2</sub>. The current-limiting characteristics with FCL are illustrated in Figure 3 by period P<sub>0</sub>-P<sub>4</sub>.

## 3 Operational principle and theoretical analysis

### 3.1 Normal operation stage

Figure 4 depicts the equivalent circuit of the proposed FCL, while the period interval P<sub>0</sub> is illustrated in Figure 3. In this stage, the line current I<sub>0</sub> flows through the L<sub>1</sub>-L<sub>2</sub>-T<sub>1</sub>-D<sub>2</sub>-DCCB path. Applying Kirchoff's voltage law (KVL) to obtain the equation for current in this stage can be written as:

$$V_s = I_0 R_{L_1 L_2} + V_{T_1} + V_{D_2} + V_{DCCB} \quad (1)$$

V<sub>s</sub> = Supply Voltage, I<sub>0</sub> = rated DC line current, V<sub>T<sub>1</sub></sub> = voltage across T<sub>1</sub>, V<sub>DCCB</sub> = Voltage across DCCB, R<sub>L<sub>1</sub>L<sub>2</sub></sub> = Resistance of L<sub>1</sub> and L<sub>2</sub>

From the above equation, the I<sub>0</sub> can be calculated as:

$$I_0 = \frac{V_s - V_{T_1} - V_{D_2} - V_{DCCB}}{R_{L_1 L_2}} \quad (2)$$

I<sub>0</sub> = I<sub>dc</sub> rated DC line current

To calculate the power loss of an FCL under normal operating conditions, we need to consider the specific type of FCL and its design parameters. Generally, the power loss P<sub>loss</sub> in an FCL can be calculated using the formula:

$$P_{loss} = I^2 * R_{FCL} \quad (3)$$

where: I, this is the nominal current the system carries under normal operation. R<sub>FCL</sub>, this is the resistance of the FCL in its normal operating state.

TABLE 1 Equivalent circuit parameters for Zhoushan HVDC grid.

Considered terminal voltage	±200 kV
Line Current	0.5 kA
Line length	200 km
Location of fault	100 km (Terminal-I)
Line Resistance/km	0.035 Ω/km
Inductance/km	0.156 mH/km

For some types of FCLs, this resistance might be very low or close to zero. So, in this research the power losses are considered negligible under normal operating condition.

### 3.2 Fault current raising stage

The equivalent circuit in this period is depicted in Figure 5. It appears that during the period marked as t<sub>0</sub>, a fault occurs in the DC grid, causing the line current to begin increasing linearly. The semiconductor switches operate according to the same switching strategy as during normal operation. During this period, the limiting inductors serve to suppress the rising rate of the fault current. The performance of the FCL during this period is represented by the interval P<sub>1</sub> in Figure 3. In this stage, the T<sub>1</sub> and D<sub>2</sub> of LCS are in conduction mode so the current flows through L<sub>1</sub> - L<sub>2</sub> - T<sub>1</sub> - D<sub>2</sub> - DCCB path.

According to the equivalent circuit and applying the KVL formula, the equations can be:

$$V_s = I_0 R_{L_1 L_2} + L_1 \frac{di}{dt} + L_2 \frac{di}{dt} + V_{T_1} + V_{D_2} + V_{DCCB}$$

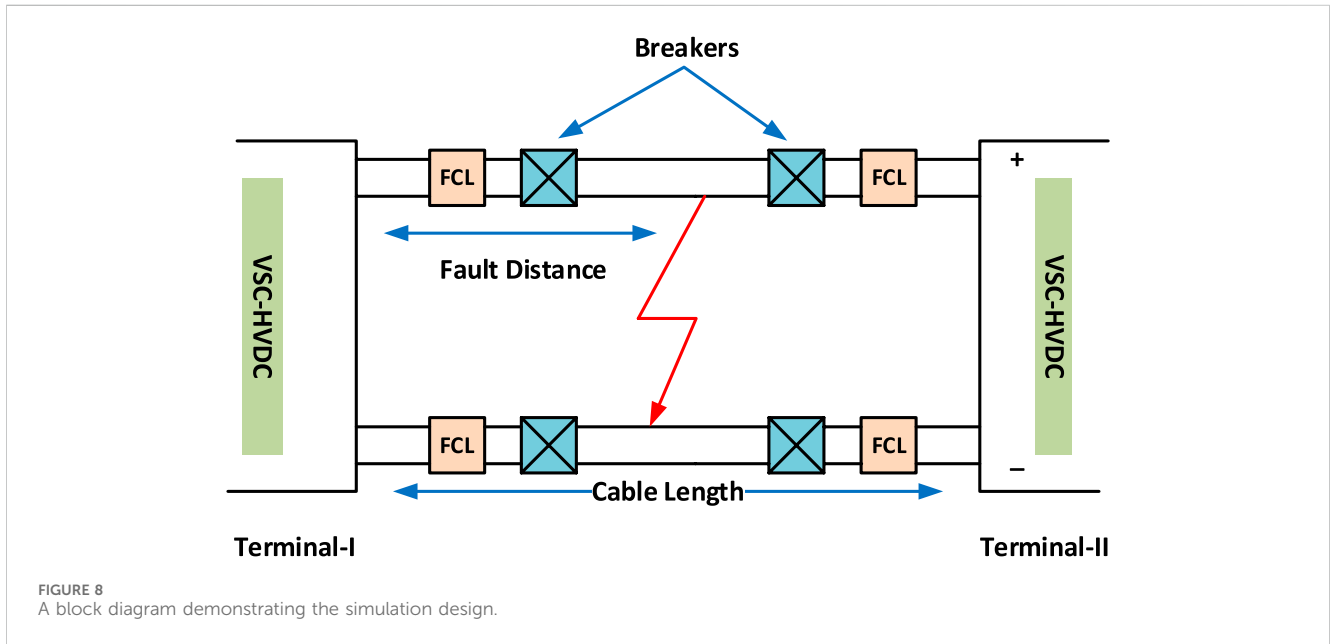
or,

$$V_s = I_0 R_{L_1 L_2} + [L_1 + L_2] \frac{di}{dt} + V_{T_1} + V_{D_2} + V_{DCCB}$$

where, L<sub>eq</sub> = L<sub>1</sub> + L<sub>2</sub>

TABLE 2 Performance Evaluation of the proposed solution.

Schemes	Current in normal condition [kA]	Current in fault condition [kA]	Voltage drop across breaker	Energy absorbed by MOA [MJ]
Ahmad et al. (2022)	0.5	2.5	More	1
Li et al. (2019)	0.5	3	More	2.5
[Proposed]	0.5	1.2	Less	0.5



$$V_s = I_0 R_{L_1 L_2} + L_{eq} \frac{di}{dt} + V_{T_1} + V_{D_2} + V_{DCCB} \quad (4)$$

$$V_s = I_0 (R_{L_1 L_2 L_3} + R_d) + L \frac{di}{dt} + V_{DCCB} \quad (6)$$

$V_{D_2}$  = Voltage across  $D_2$

Current in other lines is zero in this stage, therefore, from Equation 4 the current can be written as:

$$i_s = \left[ \frac{V_s - V_{T_1} - V_{D_2} - V_{DCCB}}{R} - I_0 \right] e^{\frac{R}{L} t} + \frac{V_s - V_{T_1} - V_{D_2} - V_{DCCB}}{R} \quad (5)$$

where,  $R_d$  = Discharging resistor and  $L = L_1 + L_2 + L_3$

$$i_s(t) = \left[ \frac{V_s - V_{DCCB}}{R_{L_1 L_2 L_3} + R_d} - i_2 \right] e^{\frac{R}{L} t} + \frac{V_s - V_{DCCB}}{R_{L_1 L_2 L_3} + R_d} \quad (7)$$

### 3.3 Fault current-limiting stage

When the fault current within interval  $P_1$  reaches the threshold value  $i_{th}$  at time  $t_1$ , the FCL triggers the opening of the LCS. Consequently, the diode ( $D_3$ ) becomes operational, conducting the fault current along the  $L_1 - L_2 - R_d - L_3$  path. The equivalent circuit of the FCL through this phase is depicted in Figure 6A. At  $t_2$ , the LCS opens, and the current through diode  $D_3$  reaches zero. Subsequently, the fault current is directed through the  $L_1 - L_2 - R_d - L_3$  path as shown in Figure 6B, where it is further limited.

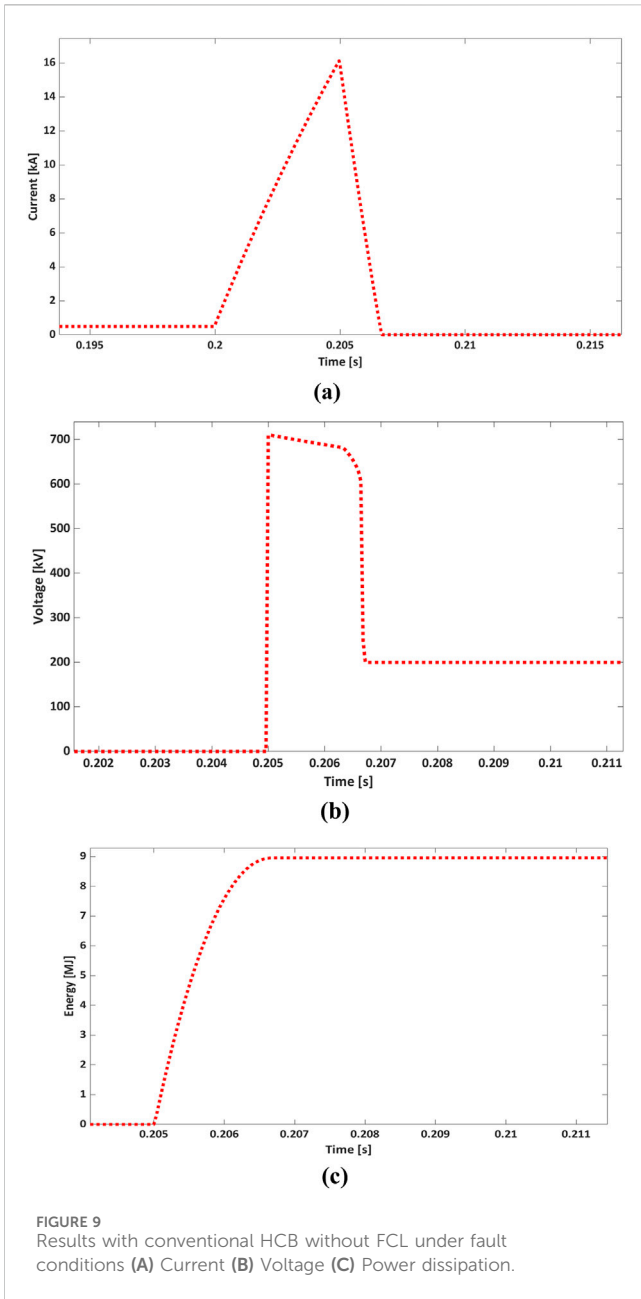
These occurrences correspond to intervals  $P_2$  and  $P_3$  in Figure 3. The KVL equations can be calculated as:

### 3.4 Fault current recovery stage

The described period commences when the DCCB is opened to isolate the fault, denoted by  $P_4$  in Figure 3. During this period, both the LCS and  $D_3$  operate in conduction mode. The equivalent circuit of the proposed FCL is illustrated in Figure 7.

The currents flow through  $L_1 - L_2$  and  $L_3$  follow paths through  $L_1 - L_2 - R_d - D_3$  and  $L_3 - R_d - D_1$ , with the resistor ( $R_d$ ) dissipating their energy. This feature of the FCL contributes to a reduction in both MOA energy ( $E$ ) dissipation and interruption speed. The energy can be calculated as:

$$E = \int v_s(t) i_o(t) dt \quad (8)$$



### 4 Parameters design

The selection of the discharging resistor  $R_d$  and the limiting inductors ( $L_1$ ,  $L_2$ , and  $L_3$ ) plays a crucial role in designing the FCL. Parameters such as the rate of increase and the magnitude of the fault current are utilized to determine the appropriate values for the FCL parameters. To meet the requirements of the DCCB, the following key factors are taken into account:

- a) During the current limiting period, it's essential to ensure that the maximum value of the DC fault current remains below the maximum interrupting current of the DCCB. Mathematically it can be written:

$$i_{ime}^{max} < i_{DCCB}^{max} \tag{9}$$

- b) The response time ( $t_r$ ) of the FCL needs to be shorter than the opening time ( $t_{DCCB}$ ) of the DCCB. The response time refers to the rising time within an initial interval of FCL to touch the threshold current. Mathematically,

$$t_r < t_{DCCB} \tag{10}$$

- c) The rate of increase in fault current must be lower than the rate of increase in DCCB current. FCLs are designed to limit the rise in fault current, allowing sufficient time for the DCCB to interrupt the DC fault current. This requirement is expressed as follows:

$$\frac{di_{ime}}{dt} < \frac{di_{DCCB}}{dt} \tag{11}$$

- d) The inductance of the limiting inductors plays a crucial role in determining the rate at which the fault current rises. Specifically, the inductance of  $L_1$ ,  $L_2$  and  $L_3$  is set to be equal (i.e.,  $L_1 = L_2 = L_3 = L_g$ ). When designing  $L_g$ , the performance of the FCL during the rising period is taken into account. As shown in Figure 3, the fault current rises with a linear slope. The slope of the fault current increase during this period can be expressed as:

$$\frac{di_{ime}}{dt} = \frac{V_s}{L_g} \tag{12}$$

According to Equation 10, Equation 11 can be written as:

$$\frac{V_s}{L_g} < \frac{di_{DCCB}}{dt} \tag{13}$$

Therefore,  $L_g$  can be written as:

$$L_g > \left( \frac{V_s}{\frac{di_{DCCB}}{dt}} \right) \tag{14}$$

- e) To control the fault current during the limiting period, selecting  $R_d$  is critical. The value of  $R_d$  must be determined to satisfy the following equation i e., Equation 9.

$$i_{ime}^{max} < i_{DCCB}^{max}$$

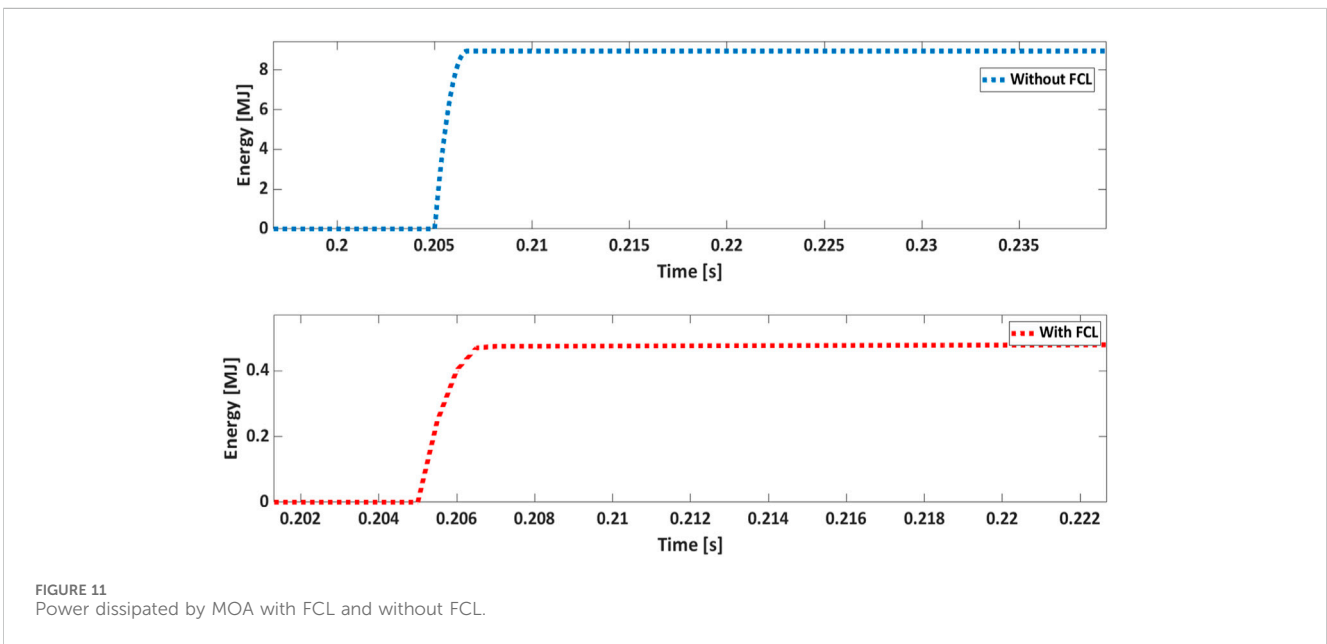
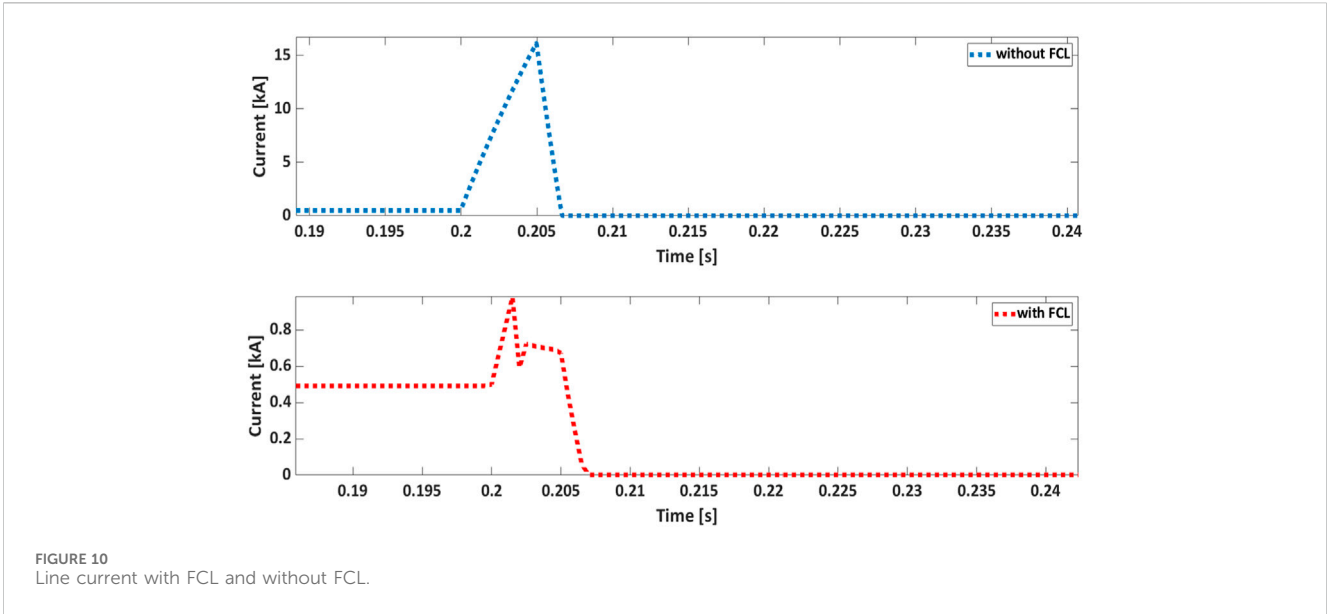
### 5 Simulation results and discussion

To validate the efficiency of the proposed FCL, simulations are conducted using PSCAD/EMTDC simulations, and the results are subsequently explained. In this work, the equivalent circuit modeling approach of the Zhoushan MMC-based HVDC grid is taken into account for simulation analysis. The equivalent circuit parameters are presented in Table 1.

For analysis, the block diagram depicted in Figure 8 illustrates the positioning of breakers with FCL between two terminals: Terminal T-1 and T-2. The short circuit fault is located on line at a specified distance from T-1.

The simulated results are categorized into two categories. The first category depicts the results of a traditional HCB lacking when the fault occurs in the DC grid. Meanwhile, the second category





demonstrates the effects of an HCB with FCL under similar fault conditions, and both sets of results are compared. Three important results are presented to highlight the importance of DCCBs equipped with FCLs. These results involve the direct voltage, current, and power consumed by the MOA within the DC breaker.

Figures 9A–C depicts the results of current, voltage and power absorption respectively with conventional HCB under fault condition. The analysis of the current response in Figure 9A reveals several observable events. Initially, from 0 to 0.2 s, the system operates under steady-state conditions, with the current maintaining a standard value of 0.5 kA in the given case study. At 0.2 s, a short-circuit fault occurs, precisely 100 km away from the T-I. Following this, the current experiences a rapid rise from its rated value, at a rate of 3.5 kA per millisecond. Within 2 milliseconds, the

current touches to approximately 16 kA. Following this transient phase, precisely at 0.202 s, the fault within the system is formally verified. In the absence of a FCL component in the conventional breaker, the current is increasing rapidly. By 0.204 s, the current peaks at approximately 16 kA, a notably substantial value. In contrast, if a FCL is implemented, the fault current undergoes a significant reduction, dropping to nearly 1 kA. As shown in the following Figure 10.

Following 0.204 s, the residual current is rerouted to the Metal Oxide Arrester (MOA) integrated across the breaker in this study to contain the fault current. Analysis of the data from Figure 10 reveals that at the end of limitation period (0.206 s) of fault current, the residual current in the HCB equipped with FCL is lower compared to that of the HCB lacking FCL. This observation indicates that

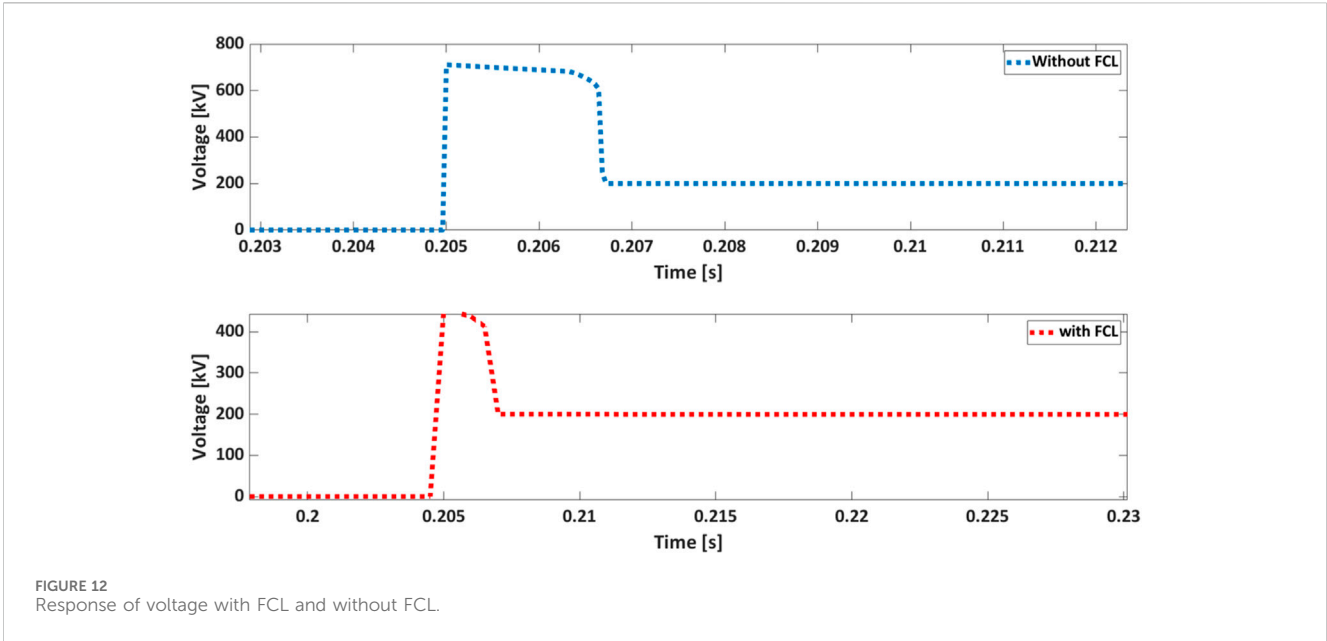


FIGURE 12 Response of voltage with FCL and without FCL.

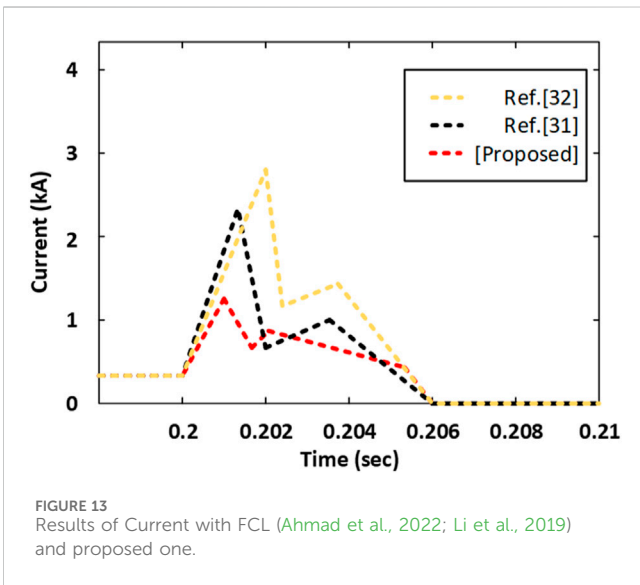


FIGURE 13 Results of Current with FCL (Ahmad et al., 2022; Li et al., 2019) and proposed one.

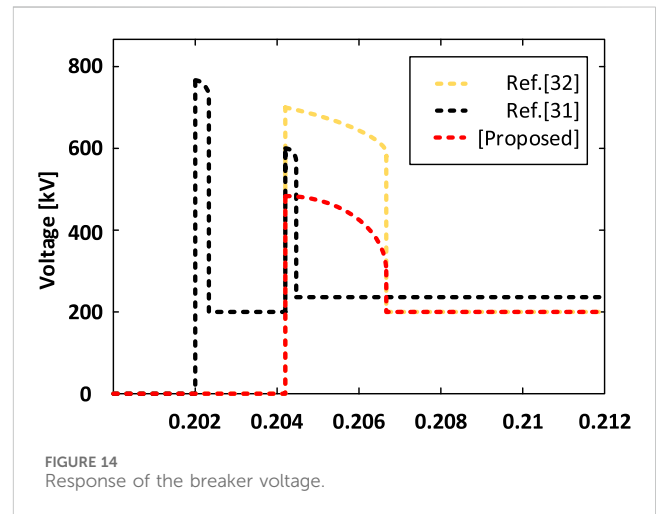


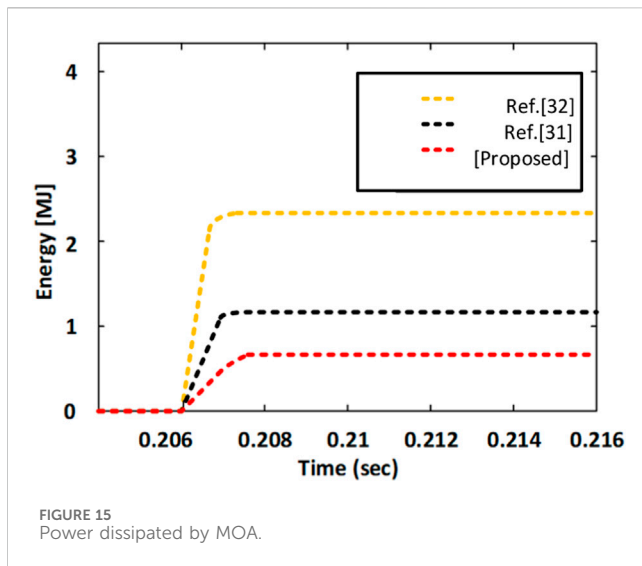
FIGURE 14 Response of the breaker voltage.

arrester in the conventional HCB lacking FCL dissipates a greater amount of energy compared to breakers with FCL as shown in the power dissipation results.

Figure 11 illustrates the power dissipation of arrester in a breaker equipped with FCL.

In describing the behavior of voltage across the breaker elements (excluding FCL), it is noted that without the presence of a fault current limiting component, transient voltage spikes are only evident in the last stage, particularly when the current is directed to the MOA. Conversely, the behavior of voltage across the breaker components with FCL is outlined differently. In Figure 12 (without FCL), during the period 0–0.2 s, the breaker works within normal working parameters, resulting in no noticeable voltage drop across the

breaker components during this phase. At 0.2 s, a system experiences a fault. However, during this period, the current flow path remains consistent with the previous stage, leading to no observable voltage drop until 0.204 s. After 0.204 s, a transient voltage spike is consistently observed across the breaker with FCL as shown in Figure 12 (with FCL). This spike is expected due to the switching action and the incorporation of Current Limiting Impedances (CLIs). When the current is directed to the MOA as indicated by the results; the voltage across it reaches the rated voltage of DC terminal, particularly evident in the case of FCL. Regarding FCL, it is important to highlight that certain current-limiting elements persist in the circuit during operational as well as non-operational phases. Consequently, a minor voltage drop is observed in last stage. To improve the transient voltage performance for breakers equipped with FCLs, it is suggested to increase the voltage ratings of the MOA.



## 6 Comparative study of the proposed FCL with other topologies

Evaluating the effectiveness and competitiveness of the proposed breaker with the FCL component, it is compared with other existing solutions. This comparative analysis aims to assess the performance and viability of the HCB-FCL system with alternative methods. FCL proposed in Ahmad et al. (2022) and Li et al. (2019) are considered to compare with their performance in this scenario. The parameters of the simulated system are presented in Table 1, corresponding to this scenario. The results depicted in Figure 13 represent the DC current flowing through the system across three distinct scenarios. In Figure 14, the voltage response across the breaker is illustrated, while Figure 15 presents the power absorbed by the MOA across various solutions. Regarding Figure 13, here are the summarized details of the discussed results: At 0.2 s, a fault occurs within the system. Subsequently, for a duration of 2 milliseconds, the current is permitted to pass through the main branch of the breaker, as discussed in Ahmad et al. (2022) and Li et al. (2019) as well as through the proposed scheme. During this period, it is evident that both the rate of increase of the current and the maximum value of the current for both the Ahmad et al. (2022) and Li et al. (2019) and the proposed scheme are identical. The limiting inductors in FCL are identical, resulting in uniform characteristics within interval P1 across all scenarios. As depicted in Figure 13, fault current surges to 3, 2.5, and 1.2 kA for Li et al. (2019) and Ahmad et al. (2022) and proposed one respectively precisely at 2.002 s. At this moment, all analyzed FCLs introduce their impedance into the fault path by opening their LCSs during fault conditions. At 0.202 s, the fault current amplitudes decrease to 1.5, 0.6, and 0.5 kA for scenarios Li et al. (2019) and Ahmad et al. (2022) and the proposed one respectively. Following the opening of HCB, the fault current amplitude decreased to zero across all cases. It can be concluded from the results that the proposed solution has more current limiting capability than that of the Ahmad et al. (2022) and Li et al. (2019).

Figure 14 illustrates the response of the breaker voltage for various cases. Among them, three responses are highlighted in

the results: one corresponds to the configuration described in Ahmad et al. (2022) another involves the use of FCL as detailed in Li et al. (2019) and the third shows the proposed configuration. The behavior of voltage across the breaker components differs among cases. In scenarios where none of the fault current limiting elements are utilized in the breaker, transient voltage spikes are primarily evident in the final phase when the current is commutated to the MOA. However, in cases involving configurations detailed in Ahmad et al. (2022) and Li et al. (2019) and the proposed setup, the voltage across the breaker components follows a distinct pattern. From 0 to 0.2 s, the breaker functions under normal operational conditions, hence no observable voltage drop occurs across the breaker components during this stage.

At 0.2 s, the system experiences a short-circuit fault, but the current flow path remains unchanged from the previous stage. Consequently, there is no voltage drop until 0.202 s. Following this, a spike of transient voltage is noted for Ahmad et al. (2022) which is expected due to switching actions and the use of Current Limiting Inductors (CLIs). Another spike of voltage is observed upon redirecting the residual current to the MOA. The results indicate that the voltage across MOA reaches the DC-rated terminal voltage when the current is redirected to the MOA, particularly in the case of Li et al. (2019) and the proposed one. Regarding Ahmad et al. (2022) it is important to observe that certain current limiting elements persist in the circuit during operational as well as non-operational stage. Consequently, a slight voltage drop is observed at the last stage. From Figure 14, it is evident that during this stage, the voltage across the proposed HCB is superior to the other two cases. The results presented in Figure 15 illustrate the power absorbed by the main arrester under various fault conditions, highlighting that the main arrester in the proposed HCB absorbs less energy compared to the others. Further, the Table 2 summarized the performance evaluation of the proposed FCL with others in literature

Based On the results presented in Figures 13–15, it was determined that the proposed FCL effectively improves the performance of HCB and surpasses the performances of the solutions outlined in Ahmad et al. (2022) and Li et al. (2019) in all aspects.

## 7 Conclusion

This research examines the significance of FCLs in DC Circuit Breakers, particularly in VSC-HVDC projects with higher ratings. The proposed FCL can carry line current during normal operation and effectively limits the rising rate of fault current by utilizing limiting inductors during the rising period. By incorporating limiting inductors and a resistor into the fault path, the system attenuates the fault current, bringing it down to zero by the end of the interval. This arrangement also helps decrease the fault current level throughout the limiting period. The system offers two freewheeling paths with a limiting resistor to dissipate the energy absorbed by the limiting inductors. Hence enhancing the energy absorption index and the interrupting speed of the breaker for the period of isolation. To assess the effectiveness of this solution, the

DC grid with parameters from the Zhoushan Grid is used to test its performance. Furthermore, its effectiveness is assessed by comparing its performance with the solutions outlined in the literature. The comparative analysis demonstrates that the proposed solution exceeds the requirements for DCCBs in terms of both current limiting capacity and energy absorption index. The results clearly demonstrate that this solution offers significant advantages for handling fault current in large-scale VSC-HVDC systems. In the future, there is ample opportunity in the literature to explore more on fault current limiters for managing fault conditions in DC systems.

## Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding authors.

## Author contributions

RC: Writing—original draft, Writing—review and editing. MS: Supervision, Writing—review and editing. AbA: Methodology, Writing—review and editing. KA: Investigation, Writing—review and editing. JS: Software, Writing—review and editing. BA: Formal Analysis, Investigation, Writing—review and editing. AhA: Validation, Writing—review and editing. MA: Resources, Software, Writing—review and editing.

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## Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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## Nomenclature

<b>CLI</b>	Current Limiting Inductors
<b>DCCB</b>	Direct Current Circuit Breaker
<b>FCL</b>	Fault Current Limiter
<b>HVDC</b>	High Voltage Direct Current
<b>HCB</b>	Hybrid Circuit Breaker
<b>HFCL</b>	Hybrid Fault Current Limiter
<b>LCC</b>	Line-Commutated Converter
<b>MMC</b>	Modular Multilevel converter
<b>MOA</b>	Metal Oxide Arrester
<b>NSCFCL</b>	Non- Superconducting Fault Current Limiter
<b>SFCL</b>	Superconducting Fault Current Limiter
<b>RSFCL</b>	Resistive Superconducting Fault Current Limiter
<b>VSC</b>	Voltage Source Converter
<b>SI</b>	Saturated-Iron
<b>KVL</b>	Kirchoff's Voltage Law