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Design and implementation of a PV-tied effective inverter with high reliability and low THD for distribution-grid applications

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Research has focused on multilevel inverters (MLIs) due to their use in electric vehicles, renewable energy systems, and industrial applications. This paper proposes a new design for a single-phase 21-level asymmetrical MLI for photovoltaic (PV) applications that reduces the number of components, voltage stress, and overall size and cost. Enhanced incremental maximum power point tracking (EINC-MPPT) is used in the PV standalone system to offer a fast dynamic response, track maximum power, and regulate the PV module output voltage. This paper presents a PV-boost DC–DC single-input multi-output (SIMO) converter linked to solar panels to provide supply voltage to the inverter. A level-shifted constant multicarrier sinusoidal pulse width modulation (LSCMSPWM) technique is used to produce a better-synthesized output waveform from the MLI, resulting in low total harmonic distortion (THD) and also meeting IEEE standards. The suggested MLI is simulated in MATLAB/Simulink and tested with a hardware prototype under various load conditions. It is suitable for medium-power and grid-connected renewable energy systems applications. The qualitative and quantitative parameters of the proposed MLI have been evaluated by cost function (CF), number of components, reliability, THD, and total standing voltage (TSV); these parameters are compared with the existing MLIs.

KEYWORDS

cost function, level-shifted constant multicarrier sinusoidal pulse width modulation, multilevel inverter, PV boost SIMO converter, total harmonic distortion, total standing voltage

1 Introduction

1.1 Background and motivation

Renewable energy sources are becoming more popular. Environmental consciousness and global energy use are increasing. In contrast, natural resources such as gas, coal, and oil are finite and rapidly depleting (Das et al., 2024). Given the limited availability of these resources, it is now necessary to explore alternative energy sources (Rahimi et al., 2023). Surprisingly, the extensive use of solar energy is leading to growing concerns about the quality, dependability, and coordination of the power grid (Tayyab et al., 2023). To ensure the safe and reliable use of photovoltaic (PV) energy, various countries have established different grid codes (Nyamathulla and Chittathuru, 2023). MLIs are increasingly using PV systems as their primary energy source (Ali Khan et al., 2020). Multilevel inverters

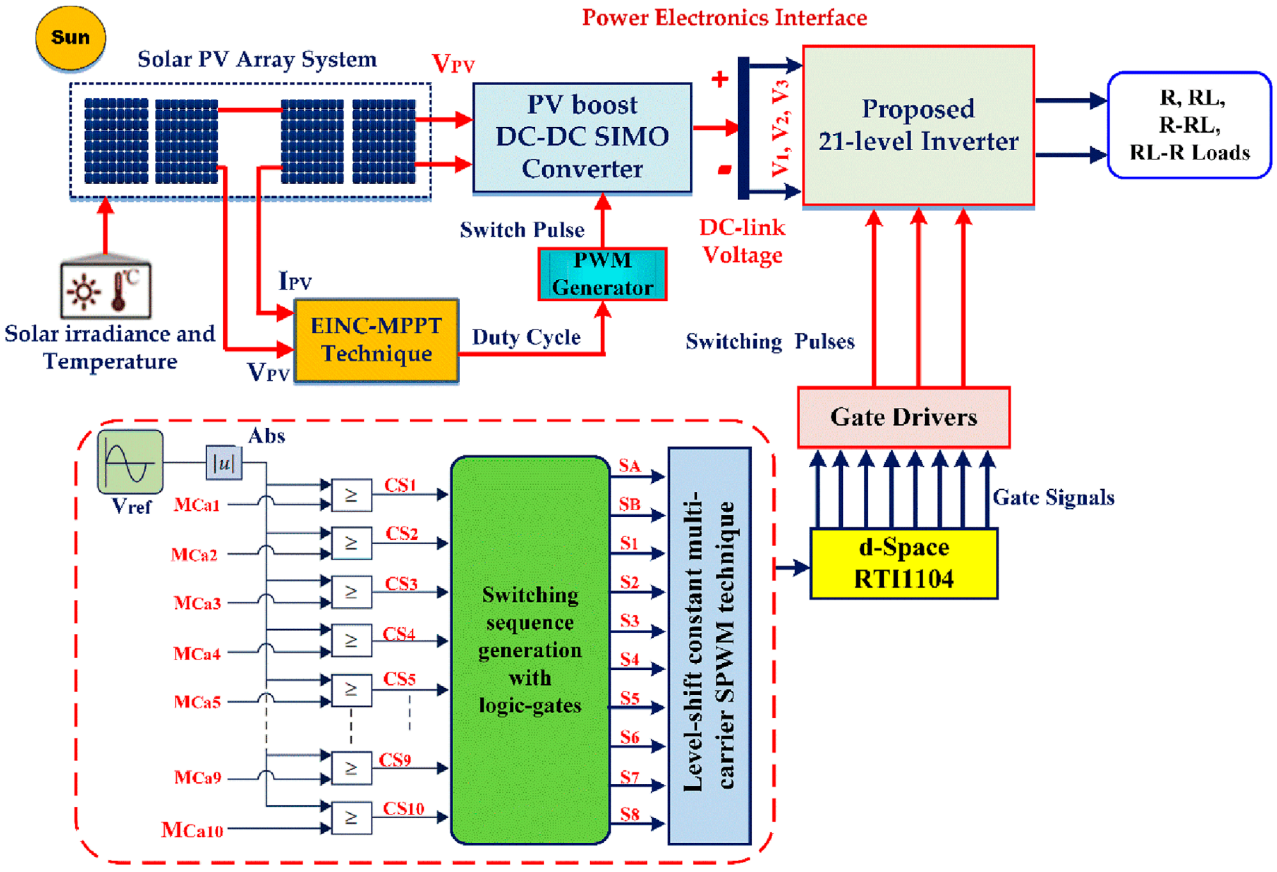

FIGURE 1
Overall proposed novelty block diagram of solar PV integrated MLI.

(MLIs) have become more common due to their many advantages, such as high power operating capacity, reduced switching losses, outstanding power quality, and low harmonics (Tayyab et al., 2022). These MLIs use several DC sources and power semiconductor switches to produce stepping voltage waveform. Raising their level could improve this voltage waveform (Chappa et al., 2021). It is difficult to achieve MLI reliability and efficiency because of the increased cost and component count of circuits. Three of the most common MLI structures are a neutral point clamped (NPC), a flying capacitor (FC), and a cascaded H-bridge (CHB) (Alhassane Soumana et al., 2022).

1.2 Literature review

According to Omer Prabhu et al. (2020a), CHB MLI provides two different single-phase H-bridge topologies—symmetrical and asymmetrical—that are dependent on DC voltage. In contrast to symmetrical MLIs, asymmetrical ones use DC voltage sources of varying magnitudes. A standard CHB-type inverter will often have a positive, zero, or negative output (Prasad and Dhanamjayulu, 2022). Rao et al. (2018) suggested assessing the output of CHB-type inverters by aggregating the output voltages of each unit. Recently developed control methods suggest CHB inverter topologies, but the full-bridge converter changes DC step outputs into AC. The limited use of full-bridge converters stems from their inability to block higher voltages, while innovative topologies can reduce both single- and three-phase system components (Majeed Shaikh et al., 2023). Some topologies used modular MLIs to provide multilevel outputs with fewer switching devices and DC sources. These topologies use antiparallel bidirectional switches to transfer current in either direction, with minimal switching components (Kumar et al., 2022). Since cascaded subunits reduce switching-device blocking voltage, they resemble modules. The problem with such topologies is that the output level increases the number of switching devices (Sinha et al., 2018). Novel MLI designs are required to provide reduced blocking voltage, more output levels, and fewer components (Bana et al., 2019). This can reduce inverter size and price. Recent work has included a stacked H-bridge MLI architecture with basic units on each side of the complete bridge (Shaik and Dhanamjayulu, 2021).

According to Das et al. (2020), researchers have been studying cascaded MLI topology configurations. There is a singular symmetric MLI that requires fewer switches. An evolutionary algorithm creates a new design and a proven way of controlling both resistive and motor loads, keeping the output voltage stable even when loads change. Babaei et al. (2014) introduced a transistor-clamped H-bridge MLI design by enabling the various output levels for higher voltage and power ratings without necessitating

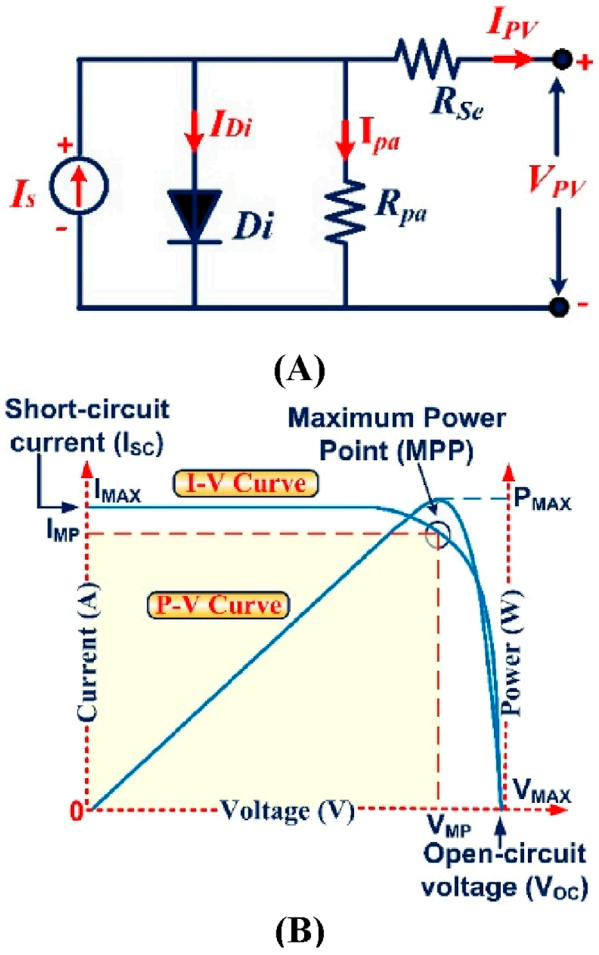

FIGURE 2
(A) PV cell equivalent circuit. **(B)** Characteristics of the solar PV panel.

an increase in component ratings. Carrier-based PWM efficiently controls the MLI, which has fewer switching losses at high switching frequencies (Siddique et al., 2020). High-frequency switching applications incur power losses. However, the topologies discussed in Omer et al. (2020b), Das et al. (2018), Sabyasachi et al. (2020), and Sarwer et al. (2020) address the challenges of more components, bulky circuits, high control complexity, THD, and low efficiency. The next step is to categorize standalone inverters as either symmetrical or asymmetrical (Prasad et al., 2021). Using the same value for each DC source indicates a symmetrical arrangement, while using different values for the DC sources results in an asymmetrical design. Meraj et al. (2020) presents two configurations ideal for low- and medium-rated solar power generation. According to Samadaei et al. (2016), FC and NPC MLIs struggle with voltage balance.

MLIs are increasingly used with PV systems as their primary energy source, and a segregated MLI architecture is best for PV integration (Alishah et al., 2017). These systems are highly efficient at electricity generation and have the added benefit of being environmentally friendly (Samadaei et al., 2018). The production of solar PV can be influenced by variations in temperature and solar radiation over time (Narendra Babu, 2024). A PV system's efficient operation heavily relies on implementing MPPT techniques. Numerous advanced MPPT techniques have been developed to improve the performance of PV systems (Alishah et al., 2016). DC–DC converters effectively handle duty cycle fluctuation to optimize power in MPPT systems. MPPT methods such as hill climbing (HC) and perturbing and observing (P&O) are commonly used due to their straightforwardness (Shaik et al., 2023). Choosing the best MPPT methodology for an application can be challenging because each approach has its advantages and disadvantages. The HC and P&O algorithms are unable to achieve global maximum partial probability (GMPP) in partial shadow (Akbari et al., 2022).

1.3 Challenges

Two-level voltage source inverters are not ideal for greater power applications due to their inability to handle high voltages and the increased electromagnetic interference caused by higher dv/dt (Krishnachaitanya and Chitra, 2021). It is necessary to address these issues to overcome these limitations. MLIs are the best option, offering advantages such as reduced voltage step, improved power quality, less switching losses, minimal harmonics, and improved electromagnetic compatibility (Mustafa et al., 2022). Additionally, as the voltage level rises in diode-clamped MLI systems, capacitor voltage balancing becomes challenging, limiting them to three levels. The utilization of FC-MLIs necessitates an increased number of DC capacitors to accommodate increased voltage levels (Hosseinzadeh et al., 2021). Nevertheless, it is possible to adjust the switching combinations and achieve balanced DC capacitor voltage (Siddique et al., 2019). CHB MLI architecture has gained in popularity and reliability because of its modularity. Nevertheless, every bridge needs a separate DC power supply. Additionally, as the levels grow, there is a greater demand for switches (Thakre et al., 2019). Topologies have been proposed as a cost-effective solution to address power quality concerns and meet high grid-code criteria (Montazer et al., 2021). These topologies are mostly derived from conventional ones; novel optimal MLI designs are required to provide high reliability, low THD, reduced blocking voltage, more output levels, and fewer components. This can reduce inverter size and price.

1.4 Contributions

Some of the most important contributions of this study are:

a. The design of a standalone solar PV system integrated with a PV boost DC–DC SIMO converter and a 21-level MLI architecture that minimizes the number of components and reduces voltage stress, total size, and cost.
b. An EINC-MPPT is used in the PV standalone system to offer a fast dynamic response, track maximum power, and regulate the PV module output voltage.
c. The LSCMSPWM approach delivers a better-synthesized output waveform from the MLI, and the resulting THD of 2.26% also fulfills IEEE standards.

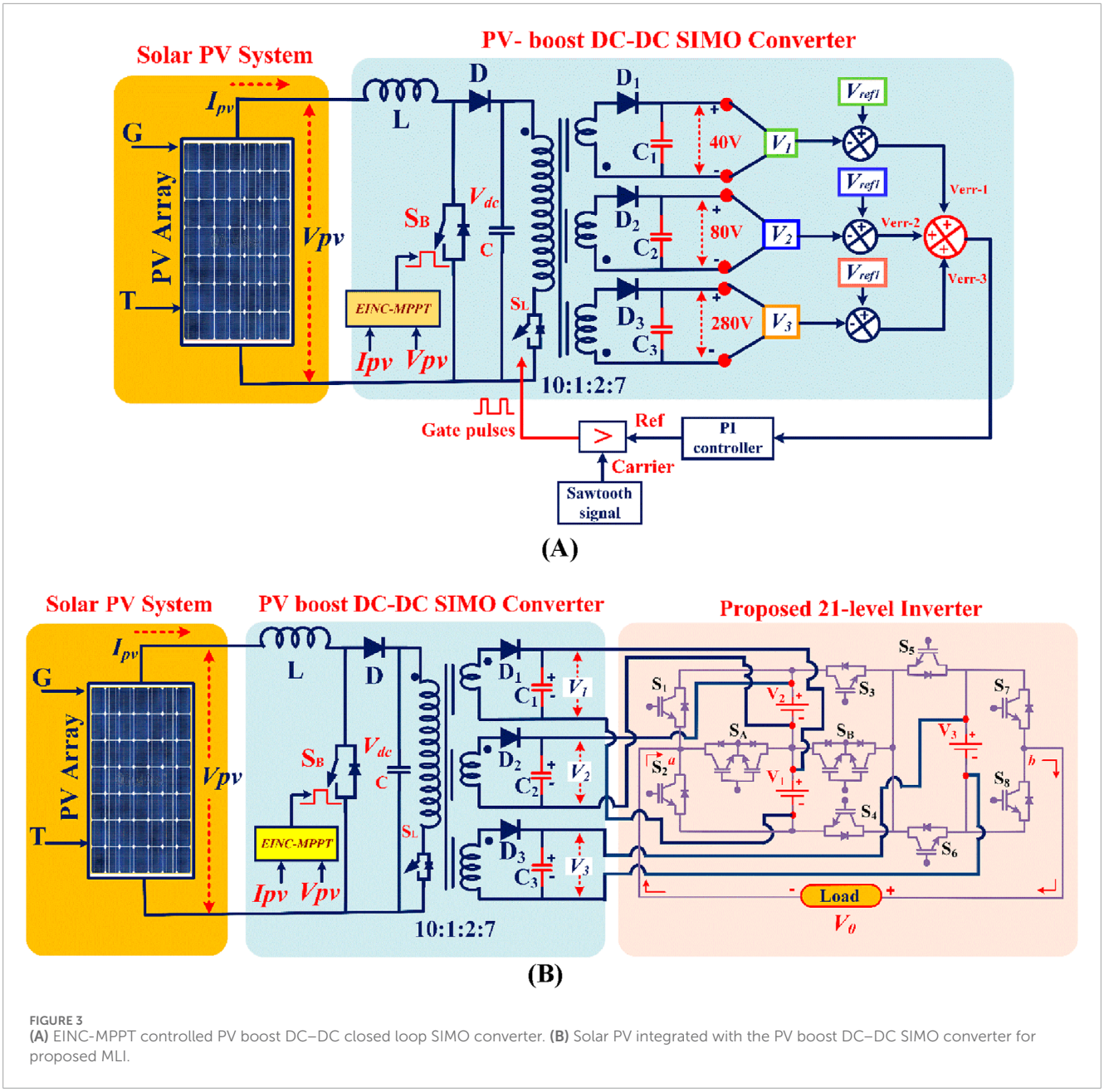

FIGURE 3
(A) EINC-MPPT controlled PV boost DC–DC closed loop SIMO converter. **(B)** Solar PV integrated with the PV boost DC–DC SIMO converter for proposed MLI.

TABLE 1 Specifications of the solar PV module SIMO converter.

215W PV module		PV boost DC-DC SIMO converter	
P_{PV}	213.15W	L	1.28 mH
I_{PV}	7.35A	C	1.31 μF
V_{PV} module	29 V	V_{PV} Input	112.8 V
I_{sc}	7.84A	δ	0.718
V_{oc}	36.3 V	V_{Bdc} Output	400 V
Irradiance	1,000 W/m^2	Capacitor ratings (3 No's)	C_1 = C2 = C3 = 9,000 μF
Temperature	25°C		

d. The suggested MLI is appropriate for medium-power and grid-connected renewable energy systems applications.
e. The qualitative and quantitative parameters of the proposed 21-level MLI outperform conventional topologies.

1.5 Structure

This study is arranged as follows. The standalone solar PV system and DC–DC boost SIMO converter are presented in Section 1. Section 2 provides a detailed explanation of the suggested 21-level MLI topology operation. In Section 3, both simulation and hardware validation results are presented. Section 4 evaluates and compares the performance parameters of various MLI topologies with the proposed MLI. Finally, Section 5 covers conclusions and future scope.

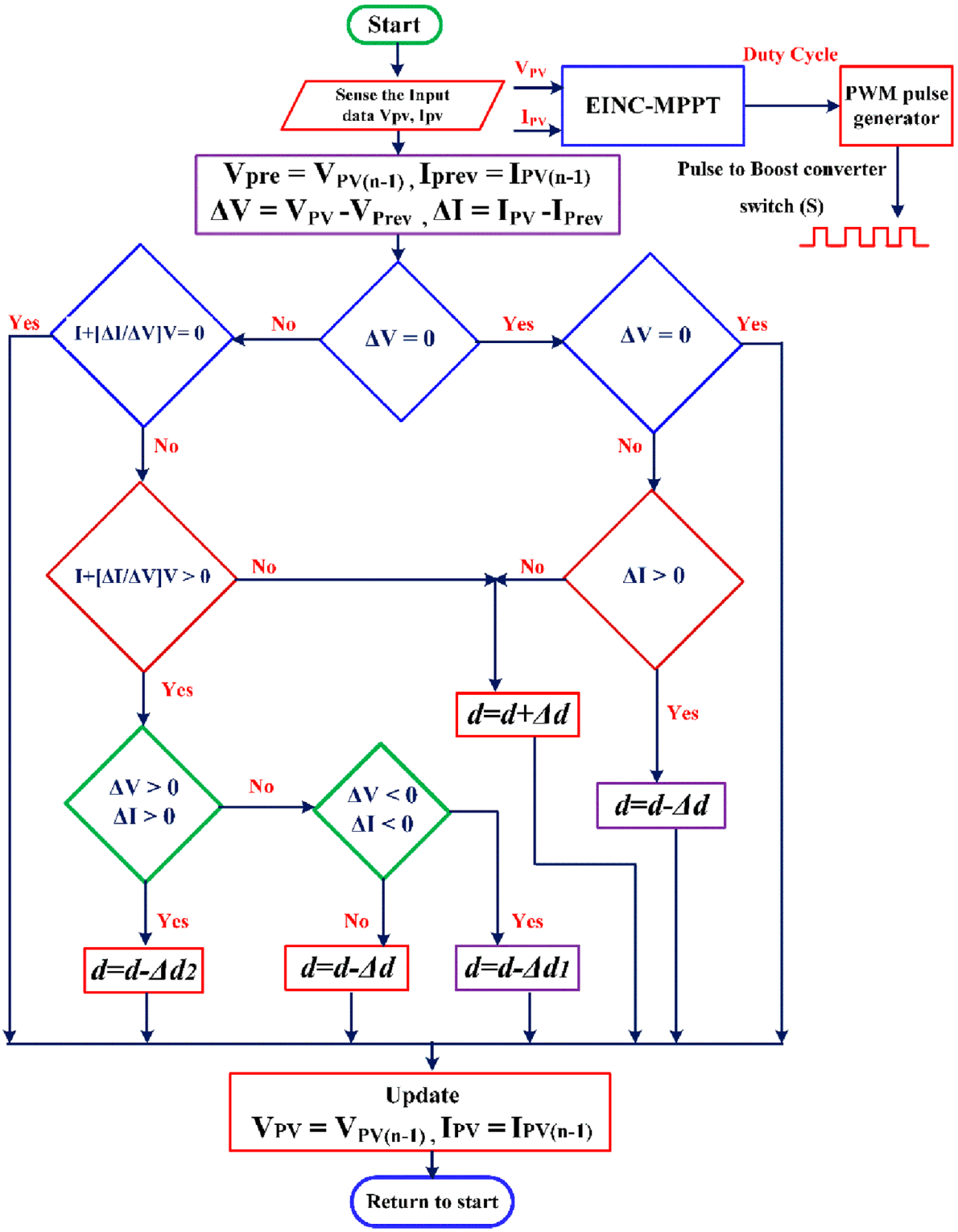

FIGURE 4
EINC-MPPT technique flowchart.

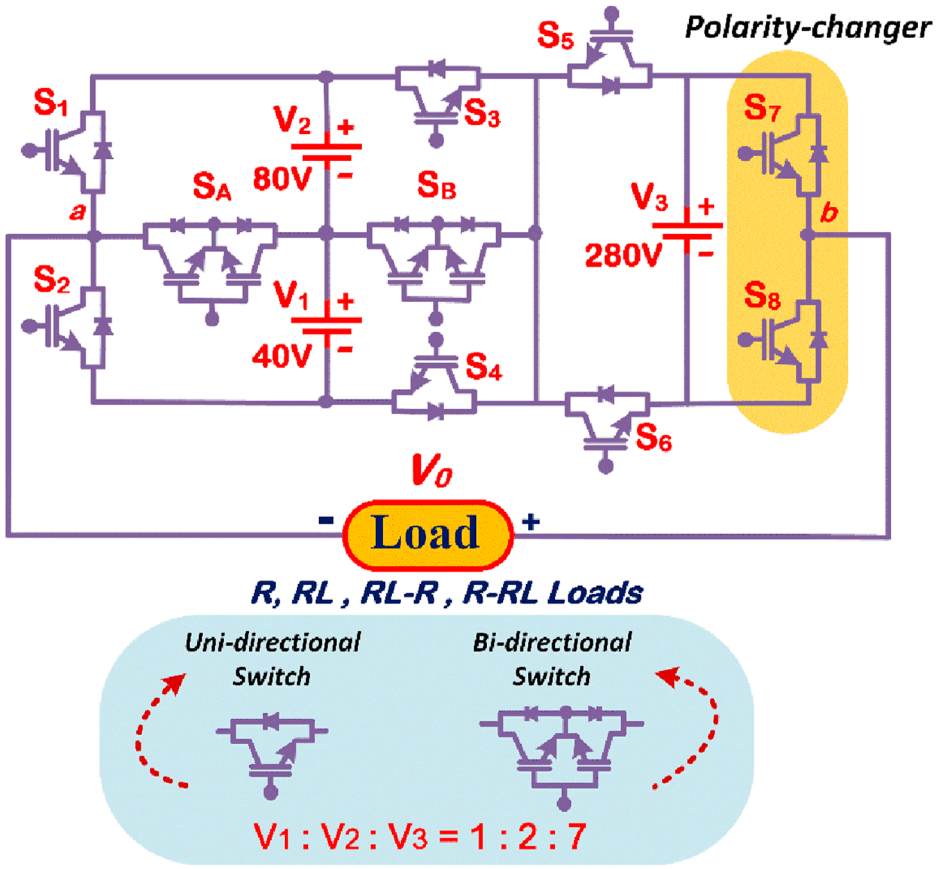

FIGURE 5
Proposed 21-level MLI architecture.

2 Proposed system

The proposed system's overall block diagram consists of a solar PV system and a PV boost DC–DC SIMO converter with a proposed MLI (Figure 1). PV technology converts light energy into electrical energy, and solar PV can modify its power production in response to changes in weather conditions and temperature. The suggested method uses a three-level converter with the EINC-MPPT technique to send DC power from PV cells to the proposed MLI architecture. The inverter collects the power that the PV panels generate. A driver circuit will activate switches as needed, employing logic circuits to produce switching pulse patterns via sequence generators. Ultimately, the proposed MLI will provide the load with 21-level output.

2.1 Design of the solar PV system

The proposed standalone solar PV system includes a selected solar panel, the 1Soltech 1STH-215-P, which has six series and two parallel units per string. Figures 2A, B display the equivalent circuit of the solar PV cell and the characteristics of the solar PV panel. D_i is the diode, R_{Pa}, R_{Se} are the resistances of parallel and series resistances, and n_{pa}, n_{se} are the number of parallel and series connected cells, respectively.

From the ideal PV circuit, the diode current can be calculated using Equation 1:

$$I_{Di} = I_0\left(e^{\frac{V_{Di}}{\gamma V_T}} - 1\right), \tag{1}$$

where γ is the ideality constant, saturation current is I_0, thermal voltage $V_T = \left(\frac{kT_c}{q}\right)$ depends on the charge of electron q, cell temperature is T_c, and Boltzmann's constant is k, equal to 1.3,806,503 $\times 10^{-23}$ J/K.

Panel Output power can be calculated by using Equation 2:

$$P_{PV} = V_{PV}\, x\, I_{PV}. \tag{2}$$

By applying KCL to the PV cell equivalent circuit,

Therefore solar PV output current can be calculated by using Equations 3, 4:

$$I_{PV} = I_S - I_{Di} - I_{pa} = I_S - I_0\left(e^{\frac{V_D}{\gamma V_T}} - 1\right) - I_p, \tag{3}$$

$$I_{PV} = n_{pa}I_S - n_{pa}I_0\left(e^{\left(\frac{1}{\gamma V_T}\right)\left(\frac{V_{PV}}{n_{se}} + \frac{R_{se}I_{PV}}{n_{pa}}\right)} - 1\right) - \frac{n_{pa}}{R_{pa}}\left(\frac{V_{PV}}{n_{se}} + \frac{R_{se}I_{PV}}{n_{pa}}\right), \tag{4}$$

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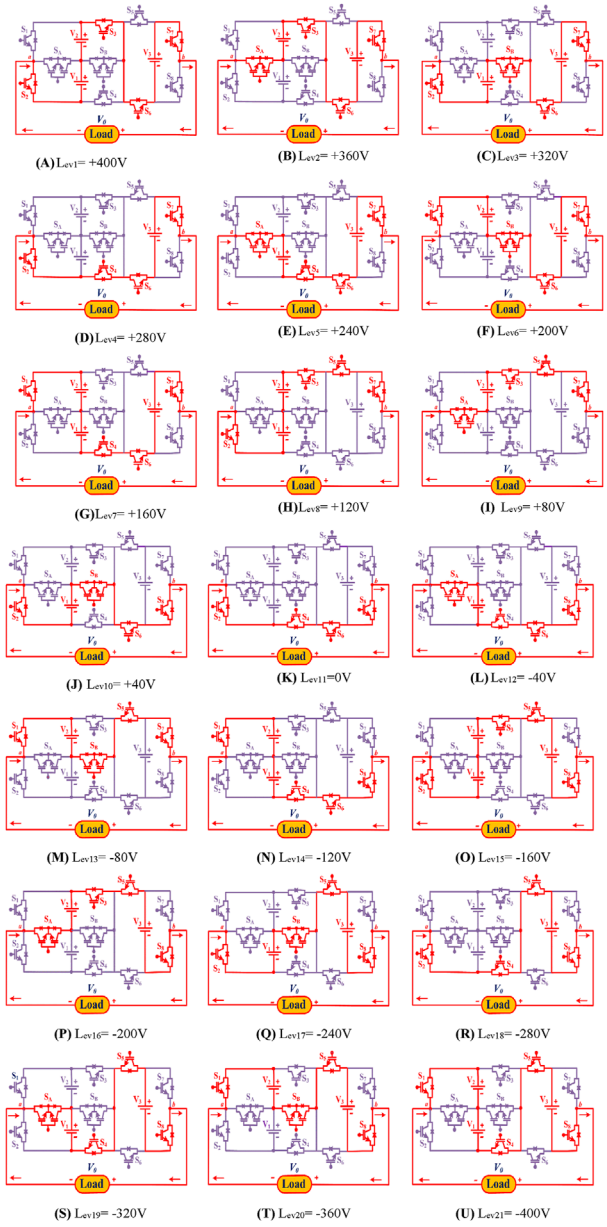


FIGURE 6
Voltage levels **(A–U)** of proposed 21-level MLI.

The short circuit current (I_S) and irradiance intensity can be calculated using Equations 5, 6:

$$I_{s(T)} = I_{s(TR)}[\beta(T - T_R) + 1], \tag{5}$$

where the temperature coefficient is β, reference temperature is T_R, and short circuit current $I_{S(TR)}$ values are included in the PV data sheets.

Therefore, the irradiance intensity is

$$I_{s(G)} = I_{s(Gn)}\frac{G}{G_n}, \tag{6}$$

where G_n indicates normal irradiation value.

The saturation current (I_0) can be calculated by Equation 7:

$$I_O = \frac{I_s}{\left(e^{\frac{V_{Di}}{\gamma V_T}} - 1\right)}. \tag{7}$$

2.2 PV boost DC–DC SIMO converter with the EINC-MPPT technique

Figures 3A, B show the connection of a PV boost DC–DC SIMO converter to solar PV panels with EINC-MPPT and solar PV-integrated with PV boost DC–DC SIMO converter for the proposed MLI. This converter consists of switches (S_B, S_L), three DC-link capacitors (C_1, C_2, C_3), and a boost inductor (L) to bring the output voltage of the PV system up to a satisfactory level for the inverter input (Rao et al., 2018). The boost converter employs an EINC-MPPT algorithm to automatically track the MPP of the PV array. The following subsections provide a comprehensive explanation of several aspects of the suggested technique.

When switch S_B is on, the output state is isolated, and an inductor (L) and a switch (S) are used to transfer the increasing input current (I_{PV}). The solar PV output voltage (V_{PV}) powers the inductor while the switch is on (T_{on}).

Therefore the inductor voltage can be calculated using Equation 8:

$$V_L = L\frac{di}{dt}. \tag{8}$$

When switch S_B is off (T_{off}), current from the inductor is forced to flow through the load and diode (D). This diode can load the inductor (L) from the voltage source.

Therefore the output voltage of converter is V_{Bdc} and can be calculated Equation 9:

$$V_{Bdc} = V_{PV} + L\frac{di}{dt}. \tag{9}$$

The boost converter output voltage is controlled by the duty cycle (δ) of the control switch. By altering the switch's on-time, the output voltage can be precisely controlled.

Therefore, the DC–DC boost converter output voltage can be calculated by Equation 10:

$$V_{Bdc} = V_{PV}\left(\frac{1}{1-\delta}\right), \tag{10}$$

where $\delta = \frac{T_{on}}{T_{on}+T_{off}}$.

The inductor and capacitor ratings are calculated using Equations 11, 12:

$$L = \frac{V_{PV} * \delta}{(f_s * \Delta I_L)}, \tag{11}$$

$$C = \frac{I_0 * \delta}{(f_s * \Delta V_{Bdc})}, \tag{12}$$

where ΔI_L is the input current, ΔV_{Bdc} is the output voltage ripple factors, and f_s is the switching frequency. To obtain a reasonable estimate of the values of the inductor and capacitor, it is recommended limiting ΔI_L to 30% and generally

TABLE 2 Proposed MLI switching states.

Level	Switching states (ON = 1 and OFF = 0)										Active sources between a and b	Output level voltage V_0 (volts)
	S_A	S_B	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8		
L_{ev1}	0	0	0	1	1	0	0	1	1	0	$V_3+V_1+V_2$	$+10V_{dc}$ = 400 V
L_{ev2}	1	0	0	0	1	0	0	1	1	0	V_2+V_3	$+9V_{dc}$ = 360 V
L_{ev3}	0	1	0	1	0	0	0	1	1	0	V_1+V_3	$+8V_{dc}$ = 320 V
L_{ev4}	0	0	0	1	0	1	0	1	1	0	V_3	$+7V_{dc}$ = 280 V
L_{ev5}	1	0	0	0	0	1	0	1	1	0	$-V_1+V_3$	$+6V_{dc}$ = 240 V
L_{ev6}	0	1	1	0	0	0	0	1	1	0	$-V_2+V_3$	$+5V_{dc}$ = 200 V
L_{ev7}	0	0	1	0	0	1	0	1	1	0	$-V_2-V_1+V_3$	$+4V_{dc}$ = 160 V
L_{ev8}	0	0	0	1	1	0	1	0	1	0	V_1+V_2	$+3V_{dc}$ = 120 V
L_{ev9}	1	0	0	0	1	0	1	0	1	0	V_2	$+2V_{dc}$ = 80 V
L_{ev10}	0	1	0	1	0	0	0	1	0	1	V_1	$+1V_{dc}$ = 40 V
L_{ev11}	0	0	0	1	0	1	0	1	0	1	—	$0V_{dc}$ = 0 V
L_{ev12}	1	0	0	0	0	1	0	1	0	1	$-V_1$	$-1V_{dc}$ = −40 V
L_{ev13}	0	1	1	0	0	0	1	0	1	0	$-V_2$	$-2V_{dc}$ = −80 V
L_{ev14}	0	0	1	0	0	1	0	1	0	1	$-V_2-V_1$	$-3V_{dc}$ = −120 V
L_{ev15}	0	0	0	1	1	0	1	0	0	1	$V_1+V_2-V_3$	$-4V_{dc}$ = −160 V
L_{ev16}	1	0	0	0	1	0	1	0	0	1	V_2-V_3	$-5V_{dc}$ = −200 V
L_{ev17}	0	1	0	1	0	0	1	0	0	1	V_1-V_3	$-6V_{dc}$ = −240 V
L_{ev18}	0	0	0	1	0	1	1	0	0	1	$-V_3$	$-7V_{dc}$ = −280 V
L_{ev19}	1	0	0	0	0	1	1	0	0	1	$-V_1-V_3$	$-8V_{dc}$ = −320 V
L_{ev20}	0	0	1	1	0	0	1	0	0	1	$-V_2-V_3$	$-9V_{dc}$ = −360 V
L_{ev21}	0	0	1	0	0	1	1	0	0	1	$-V_2-V_1-V_3$	$-10V_{dc}$ = - 400 V
Blocking voltage (BV)	$2V_{dc}$	$2V_{dc}$	$3V_{dc}$	$3V_{dc}$	$3V_{dc}$	$3V_{dc}$	$7V_{dc}$	$7V_{dc}$	$7V_{dc}$	$7V_{dc}$	$44V_{dc}$	

assuming ΔV_{Bdc} at 5%. The characteristics of the solar PV module DC–DC boost converter requirements are detailed in Table 1.

The MPPT controller controls the performance of the boost converter by considering inputs such as temperature, solar radiation, PV array (Voc and Isc) characteristics, and DC link voltage. When the operating point varies around the maximum power point (MPP), especially in situations with rapidly changing irradiance levels, the effectiveness of conventional incremental and conductance MPPT algorithms decreases. To address these problems, an EINC-MPPT technique is implemented; Figure 4 illustrates a flowchart of an EINC-MPPT technique.

2.3 Proposed 21-level asymmetrical MLI topology

The proposed 21-level MLI architecture consists of fewer components without any inductors, capacitors, and diodes (Figure 5). It consists of only two bidirectional switches (S_A and S_B), eight unidirectional switches (S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8), and three asymmetrical voltage sources (V_1, V_2, V_3) to achieve 21 voltage levels, with each voltage step V_{dc} = 40 V and the maximum output voltage 400 V. The DC voltage ratio is crucial for maximizing output voltage and reducing the inverter's TSV. Based on the recommended MLI architecture, the required component estimations follow.

TABLE 3 Proposed 21-level MLI current conduction paths.

Level	Active sources between a and b	Current conduction path	Voltage stress on switches	Output voltage V_0 (volts)
L_{ev1}	$V_3+V_1+V_2$	V_1-V_2 - S_3- S_6- V_3- S_7- L- S_2- V_1	S_1, S_4, S_A, S_B, S_5, and S_8	$+10V_{dc}$ = 400 V
L_{ev2}	V_2+V_3	V_2 - S_3- S_6- V_3- S_7- L- S_A- V_2	S_1, S_2, S_4, S_B, S_5, and S_8	$+9V_{dc}$ = 360 V
L_{ev3}	V_1+V_3	V_1- S_B- S_6- V_3- S_7- L- S_2- V_1	S_1, S_3, S_4, S_A, S_5, and S_8	$+8V_{dc}$ = 320 V
L_{ev4}	V_3	V_3- S_7- L- S_2- S_4 – S_6 – V_3	S_1, S_3, S_A, S_B, S_5, and S_8	$+7V_{dc}$ = 280 V
L_{ev5}	-V_1+ V_3	V_1- S_4- S_6- V_3- S_7- L- S_A- V_1	S_1, S_2, S_3, S_B, S_5, and S_8	$+6V_{dc}$ = 240 V
L_{ev6}	-V_2+ V_3	V_2 – S_B- S_6- V_3- S_7- L- S_1- V_2	S_2, S_3, S_4, S_A, S_5, and S_8	$+5V_{dc}$ = 200 V
L_{ev7}	-V_2-V_1+V_3	V_2-V_1 – S_4- S_6- V_3- S_7- L- S_1- V_2	S_2, S_3, S_A, S_B, S_5, and S_8	$+4V_{dc}$ = 160 V
L_{ev8}	V_1+V_2	V_1-V_2 - S_3- S_5- S_7- L- S_2- V_1	S_1, S_4, S_A, S_B, S_6, and S_8	$+3V_{dc}$ = 120 V
L_{ev9}	V_2	V_2- S_3- S_5- S_7 – L- S_A –V_2	S_1, S_2, S_4, S_B, S_6, and S_8	$+2V_{dc}$ = 80 V
L_{ev10}	V_1	V_1- S_B- S_6- S_8- L- S_2- V_1	S_1, S_3, S_4, S_A, S_5, and S_7	$+1V_{dc}$ = 40 V
L_{ev11}	-	S_2- S_4- S_6- S_8 - L- S_2	S_1, S_3, S_A, S_B, S_5, and S_7	$0V_{dc}$ = 0 V
L_{ev12}	-V_1	V_1-S_4- S_6- S_8- L- S_A- V_1	S_1, S_2, S_3, S_B, S_5, and S_7	$-1V_{dc}$ = −40 V
L_{ev13}	-V_2	V_2 – S_B- S_5- S_7- L- S_1- V_2	S_2, S_3, S_4, S_A, S_6, and S_8	$-2V_{dc}$ = −80 V
L_{ev14}	-V_2-V_1	V_2-V_1 – S_4- S_6- S_8- L- S_1- V_2	S_2, S_3, S_A, S_B, S_5, and S_7	$-3V_{dc}$ = −120 V
L_{ev15}	V_1+V_2- V_3	V_1-V_2 - S_3- S_5- V_3- S_8- L- S_2- V_1	S_1, S_4, S_A, S_B, S_6, and S_7	$-4V_{dc}$ = −160 V
L_{ev16}	V_2-V_3	V_2 - S_3- S_5- V_3- S_8- L- S_A- V_2	S_1, S_2, S_4, S_B, S_6, and S_7	$-5V_{dc}$ = −200 V
L_{ev17}	V_1-V_3	V_1 – S_B- S_5- V_3- S_8- L- S_2- V_1	S_1, S_3, S_4, S_A, S_6, and S_7	$-6V_{dc}$ = −240 V
L_{ev18}	-V_3	V_3- S_8- L- S_2- S_4- S_5- V_3	S_1, S_3, S_A, S_B, S_6, and S_7	$-7V_{dc}$ = −280 V
L_{ev19}	-V_1-V_3	V_1- S_4- S_5- V_3- S_8- L- S_A- V_1	S_1, S_2, S_3, S_B, S_6, and S_7	$-8V_{dc}$ = −320 V
L_{ev20}	-V_2-V_3	V_2 - S_B- S_5- V_3- S_8- L- S_1- V_2	S_2, S_3, S_4, S_A, S_6, and S_7	$-9V_{dc}$ = −360 V
L_{ev21}	-V_2-V_1-V_3	V_2-V_1 - S_4- S_5- V_3- S_8- L- S_1- V_2	S_2, S_3, S_A, S_B, S_6, and S_7	$-10V_{dc}$ = -400 V

2.3.1 Components selection

For the proposed MLI asymmetric operation required DC voltage sources are represented below using Equation 13:

$$V_1 = 1V_{dc}; V_2 = 2V_{dc}; V_3 = 7V_{dc}. \quad (13)$$

The required DC sources, switches, driver circuits, and maximum output voltage of the proposed MLI are determined using Equations 14–17, where N_{Lev} indicates the number of levels:

$$N_{Sources}^{Prop} = \frac{(N_{Lev} - 3)}{6}, \quad (14)$$

$$N_{Switches}^{Prop} = \frac{(N_{Lev} - 1)}{2}, \quad (15)$$

$$N_{Driver\ circuits}^{Prop} = \frac{(N_{Lev} - 1)}{2} = 10. \quad (16)$$

The maximum voltage output ($V_{o,max}$) is

$$V_{0,max}^{Prop} = \frac{(N_{Lev} - 1)}{2} x V_{dc} = 10 \times 40 = 400V. \quad (17)$$

The switches are vital in producing 21 levels using the switching pattern generated by the switching pulse generators. The suggested operational modes of the MLI topology are shown in Figures 6A–U. The various output voltage levels and their corresponding switching states are detailed in Table 2. The current conduction paths are listed in Table 3, and the waveform of the predicted output voltage of the suggested MLI is displayed in Figure 7.

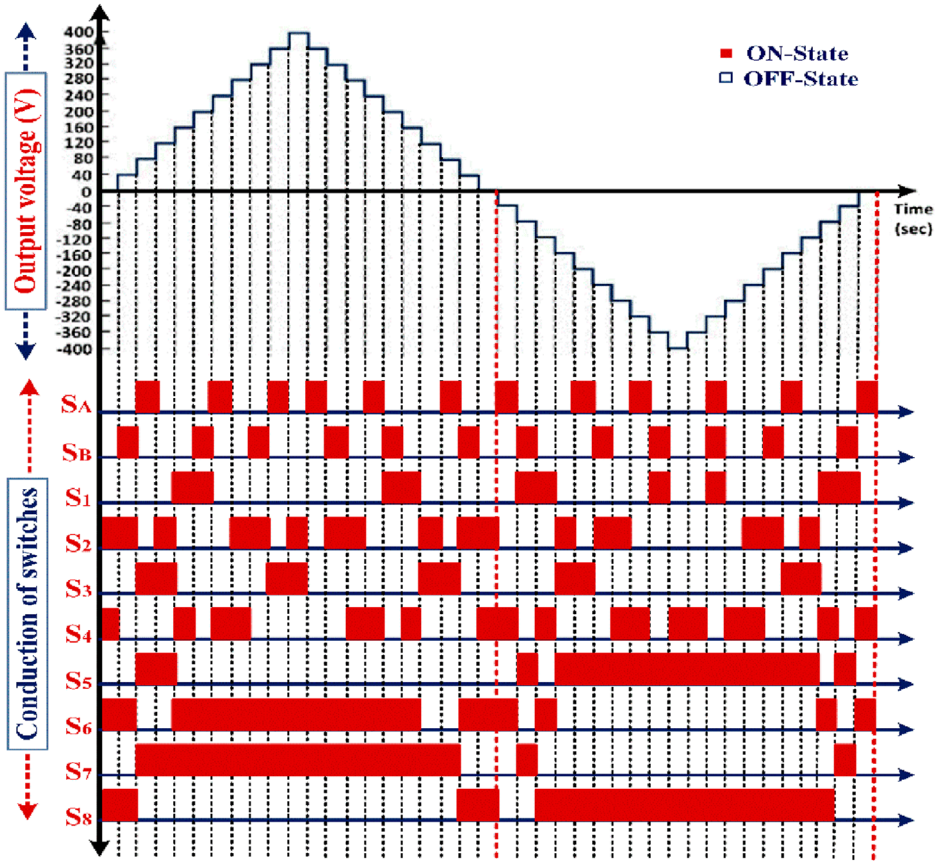


FIGURE 7
Proposed 21-level MLI expected output voltage waveform.

2.3.2 Level-shifted constant multicarrier sinusoidal pulse width modulation (LSCMSPWM) technique

The proposed MLI needs the right modulation methods to obtain a lower THD that meets the IEEE standard limits and provides good power from the MLI end. Modulation methods enhance the synthesis of the MLI output waveform. To provide gating signals for the power switching devices of the converter, the fundamental frequency is used. In this case, a pulse width modulation technique is used as a control. The optimal reference sinusoidal pulse is associated with level-shifted average level constant multicarrier signals of similar characteristics, which are used to generate gating signals for controlling power converter switches.

This control approach requires $(N_{Lev}-1)/2$ average level constant multicarrier signals to achieve the required output voltage levels. The modulation technique generates the model voltage output waveform and logic gate-based (LGB) switching gate pulse generators to store the switching order of every switching device (Figures 8A, B). Ten average-level constant multicarrier pulses (MC_{a1} – MC_{a10}) can produce 21 voltage levels with different shift values but equal frequency. Gate pulse patterns for power converter switching devices are generated by comparing average level constant multicarrier carrier signals with a pure sinusoidal waveform signal ($V_{ref} = |V_m \sin(\omega t)|$).

The amplitude of the level-shift constant multicarrier pulse modulated index (M_a) is calculated using Equation 18:

$$M_a^{index} = \frac{Vm}{[(N_{Lev}-1)/2]\,x\,Vcr}. \tag{18}$$

The variables Vm and Vcr denote the peak voltage amplitude of the reference signal and the voltage of the constant multicarrier signals, respectively. The proposed 21-level MLI topology requires one fundamental sinusoidal waveform with a 50 Hz frequency as a reference and ten average-level constant multicarrier signals to generate the pulses for power switches. The RMS output voltage of the proposed MLI with its respective modulation index can be calculated using Equation 19:

$$V_{ab}^{Out} \approx Ma^{index}\,\frac{Vdc}{\sqrt{2}}. \tag{19}$$

The optimal output voltage waveform is clipped more frequently as the switching frequency increases. This limits its fluctuation to short intervals.

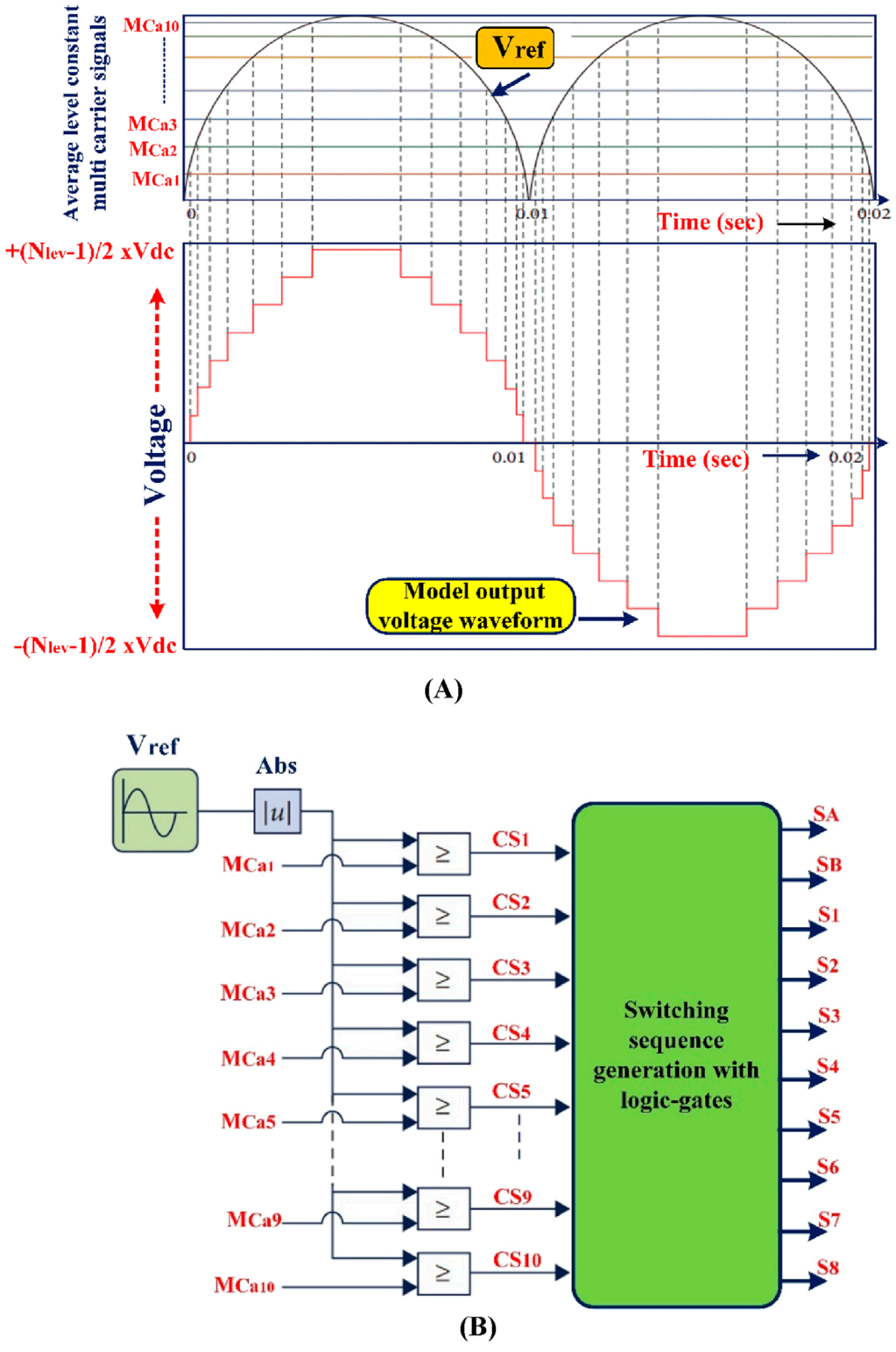


FIGURE 8
(A) Expected output voltage waveform of the LSCMSPWM technique. **(B)** LSCMSPWM technique switching sequence generation for proposed 21-level MLI.

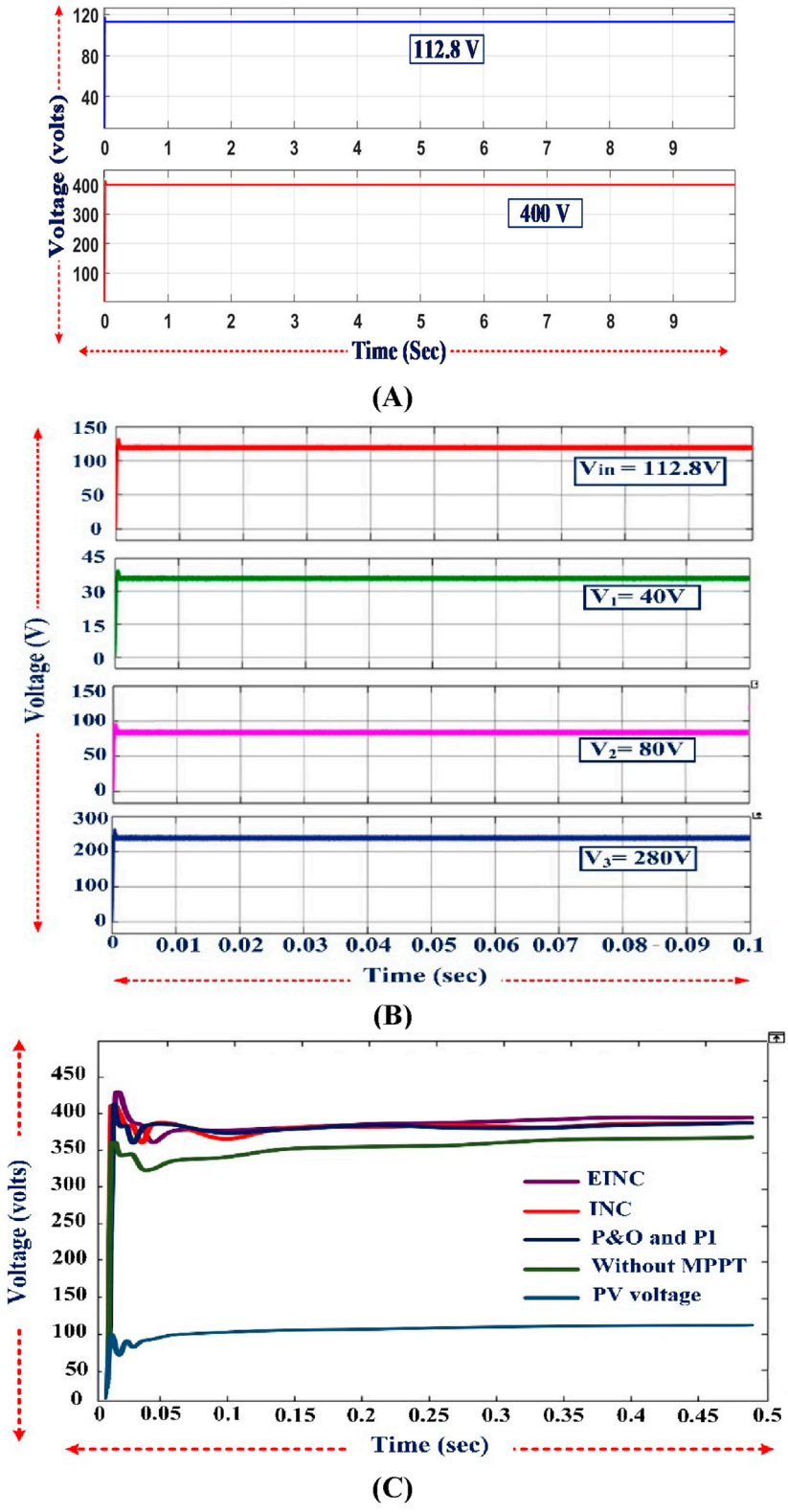


FIGURE 9
(A) Simulated output voltage of the solar PV panel and DC–DC boost converter on the side of the SIMO converter. **(B)** Simulated input and output voltages of the PV boost DC–DC SIMO converter. **(C)** DC-link voltage response with different MPPT algorithms.

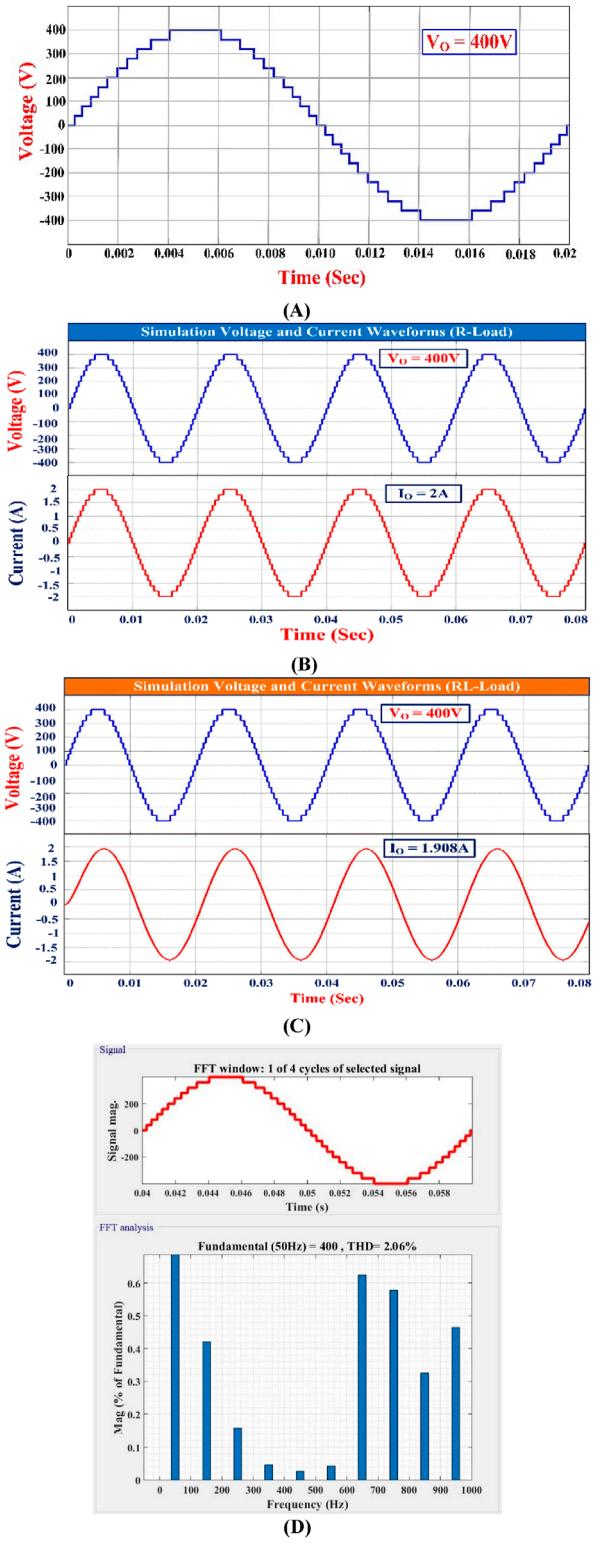


FIGURE 10
(A) Simulated output voltage of proposed 21-level MLI. **(B)** Simulated output voltage and current waveforms of proposed MLI for R-load. **(C)** Simulated output voltage and current waveforms of proposed MLI for RL-load. **(D)** Simulated THD of proposed 21-level MLI.

TABLE 4 Specifications of the proposed MLI experimental setup.

Apparatus/parameter	Range/type
Driver board	TLP-250
Load	R = 100–400 Ω, L = 100–400 mH
Switching frequency	5 kHz
DC sources	0–500 V/programmable
IGBT module	600 V, 75 A/(CM75DU-12H)
Controller	dSPACE RTI 1104
Fundamental frequency	50 Hz

3 Result analysis

To observe the proposed MLI's real-time response to various load conditions, it is necessary to simulate and validate the recommended MLI architecture by implementing the prototype. The subsequent sections detail the outcomes of both the simulation and experimental results.

3.1 Simulation results

The simulation results of the solar PV panel and PV-boost SIMO converter output voltages with EINC-MPPT are displayed in Figure 9A. The solar PV panel at MPP generates 112.8 V and is boosted to 400 V using a PV boost converter on the side of a SIMO converter. The PV boost DC–DC SIMO-converter simulated input and output voltages are displayed in Figure 9B. The DC link voltage response comparison for different MPPT techniques is displayed in Figure 9C. The proposed EINC MPPT technique is very effective, with a lower settlement time of 0.085 s than other MPPT techniques.

The suggested MLI circuit is modeled and simulated using MATLAB/Simulink software. The switch pulse patterns are produced at a switching frequency of 5 kHz by comparing the multicarrier signals through a 50 Hz sinusoidal signal. The modeled topology is tested for R-load as well as RL-loads. The output voltage and current waveforms of the proposed MLI are shown in Figures 10A–C. These show the output voltage and current waveforms of the MLI with R = 200Ω load and the output voltage and current waveforms of the MLI with an RL-load (R = 200Ω, L = 200 mH), respectively. The simulated FFT analysis THD of 2.06% is displayed in Figure 10D.

3.2 Hardware results

The experimental testing of the proposed MLI architecture was conducted, and the component specifications are listed in Table 4.

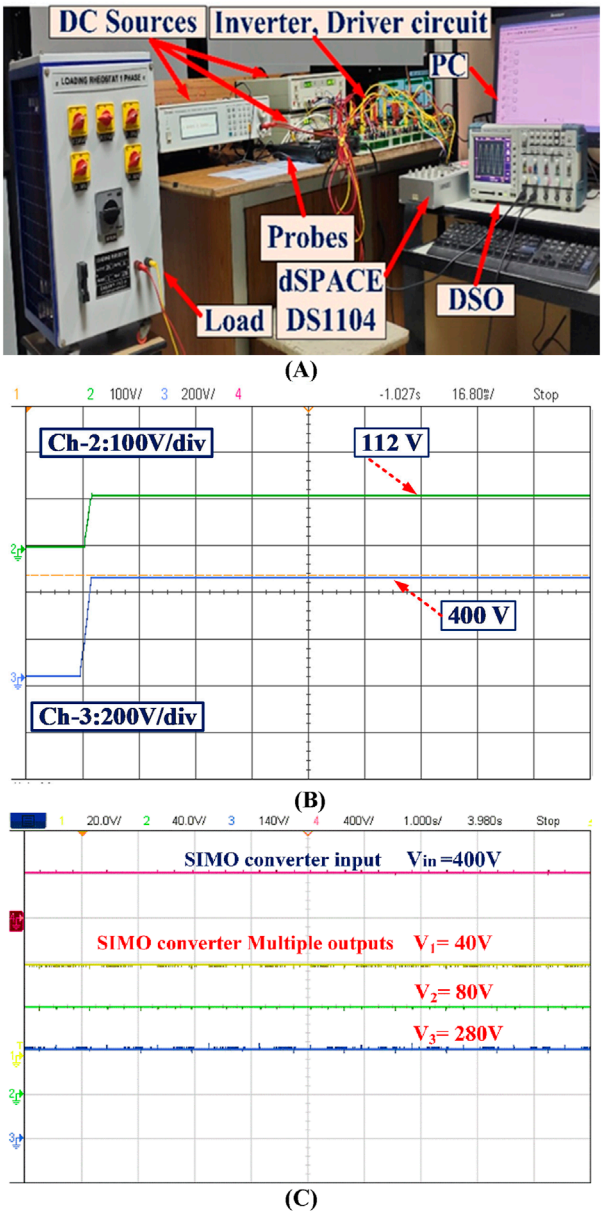


FIGURE 11
(A) Experimental setup of proposed 21-level MLI. **(B)** Experimental output voltage of the solar PV panel and PV-boost converter. **(C)** Experimental input and output voltages of the closed loop SIMO converter.

Power-switching IGBT (CM75DU-12H) devices, optocouplers (MCT2E), and asymmetrical DC sources are used to implement this hardware prototype. The dSPACE RT1104 controller is used to generate the switching sequence for each switching device, using optocouplers for activation. The hardware prototype was tested with various load conditions, achieving a 21-level output voltage of 400 V. The voltage and current output waves were examined, and the

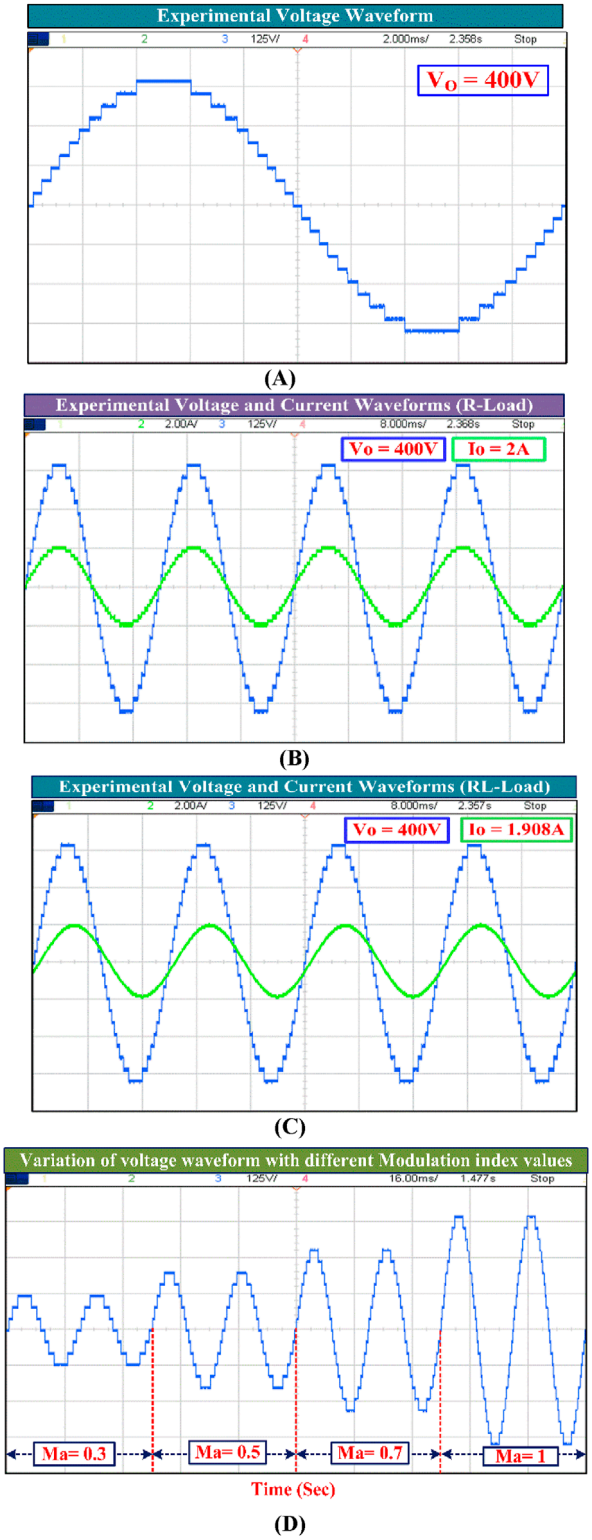


FIGURE 12
Proposed MLI experimental waveforms. **(A)** Output voltage waveform. **(B)** Output voltage and current waveforms for R-load. **(C)** Output voltage and current waveforms for RL-load. **(D)** Output voltage for different modulation index (Ma) values.

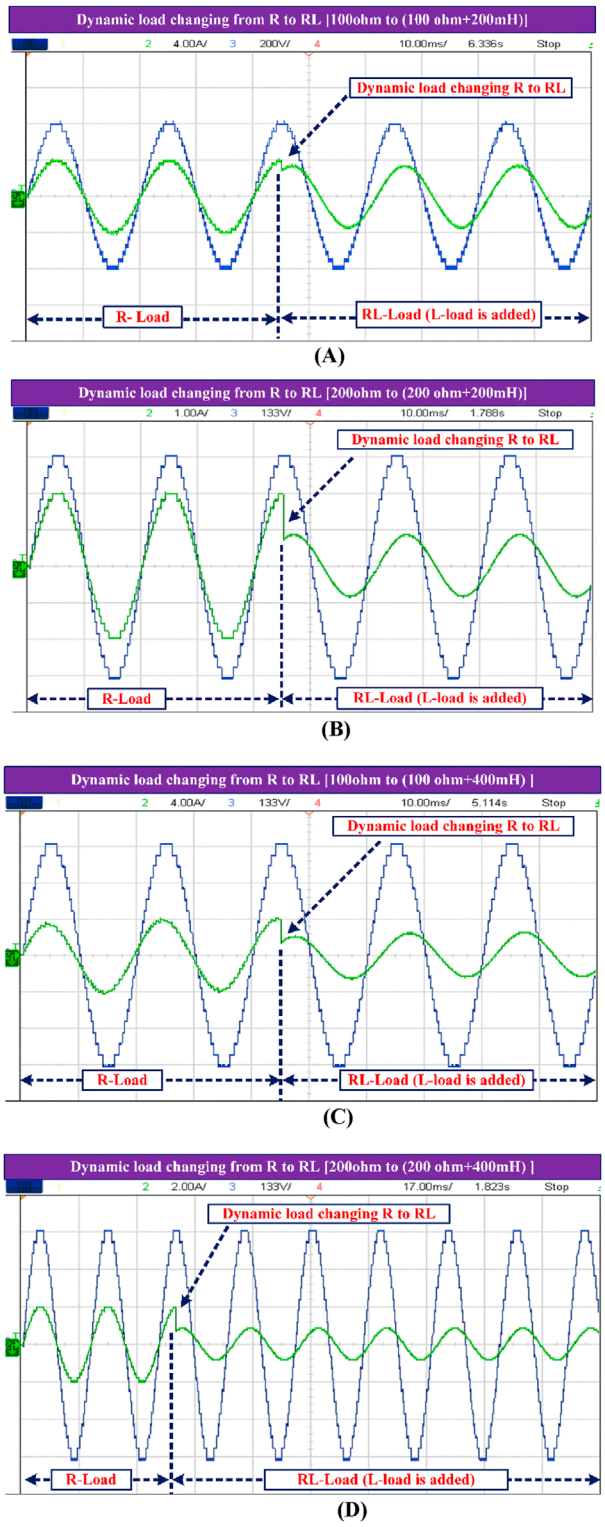


FIGURE 13
Experimental voltage and current waveforms for dynamic load changes from R- to RL-load. **(A)** 100 Ω to (100 Ω + 200 mH). **(B)** 200 Ω to (200 Ω + 200 mH). **(C)** 100 Ω to (100 Ω + 400 mH). **(D)** 200 Ω to (200 Ω + 400 mH).

results were captured using a DSO connected to the prototype via a differential probe. A hardware prototype of the suggested MLI is shown in Figure 11A.

Figure 11B presents the experimental output voltage waveforms of the solar PV panel as well as the PV-boost converter. Figure 11C presents the input and output voltages of the PV-boost DC–DC SIMO converter.

Figures 12A–D present the output voltage as well as the voltage and current waveforms of a proposed MLI for R = 200Ω load and RL-load (R = 200Ω, L = 200 mH), as well as the output voltage waveform for various modulation index (Ma) values, respectively. Figures 13A–D present the output current behavior when the dynamic load changes from R- to RL-load. Figures 14A–E present the output current behavior when the dynamic load changes from RL- to R-. The output voltage THD is 2.26%—in line with IEEE standards.

4 Comparative analysis

The proposed 21-level MLI architecture was compared using performance indicators like TSV, THD, losses, efficiency and reliability parameters' fault rate (FR_T), and mean time to failure ($MTTF_T$). Procedures and computations for these performance indicators are discussed below. Various qualitative and quantitative parameters are compared, tabulated, and graphically illustrated.

4.1 Total standing voltage (TSV) calculation

TSV is extensively used to choose power switches. All power-switching devices in the design have an influence on TSV (Prasad and Dhanamjayulu, 2022). To calculate the blocked voltage across power-switching devices, $V_{Sbi} = V_i$ and $V_{Suni} = 2V_i$ are the voltage stresses on the bi- and uni-directional switches, respectively, where i = 1, 2, n and n is the power switch.

Therefore, the maximum output voltage is calculated using Equation 20:

$$\mathbf{V_{o,max} = 10V_{dc} = 400V.} \tag{20}$$

The maximum blocking voltage (MBV) of particular switches can be calculated using Equations 21–23:

$$\mathbf{MBV_{SA} = MBV_{SB} = 2V_{dc},} \tag{21}$$

$$\mathbf{MBV_{S1} = MBV_{S2} = MBV_{S3} = MBV_{S4} = 3V_{dc},} \tag{22}$$

$$\mathbf{MBV_{S5} = MBV_{S6} = MBV_{S7} = MBV_{S8} = 7V_{dc}.} \tag{23}$$

The normalized voltage stress (NV_{stress}) is defined as the ratio of the switch's V_{stress} to $V_{o,max}$. The V_{stress} is the true voltage stress. Respective switch voltage stress values are listed in Table 5.

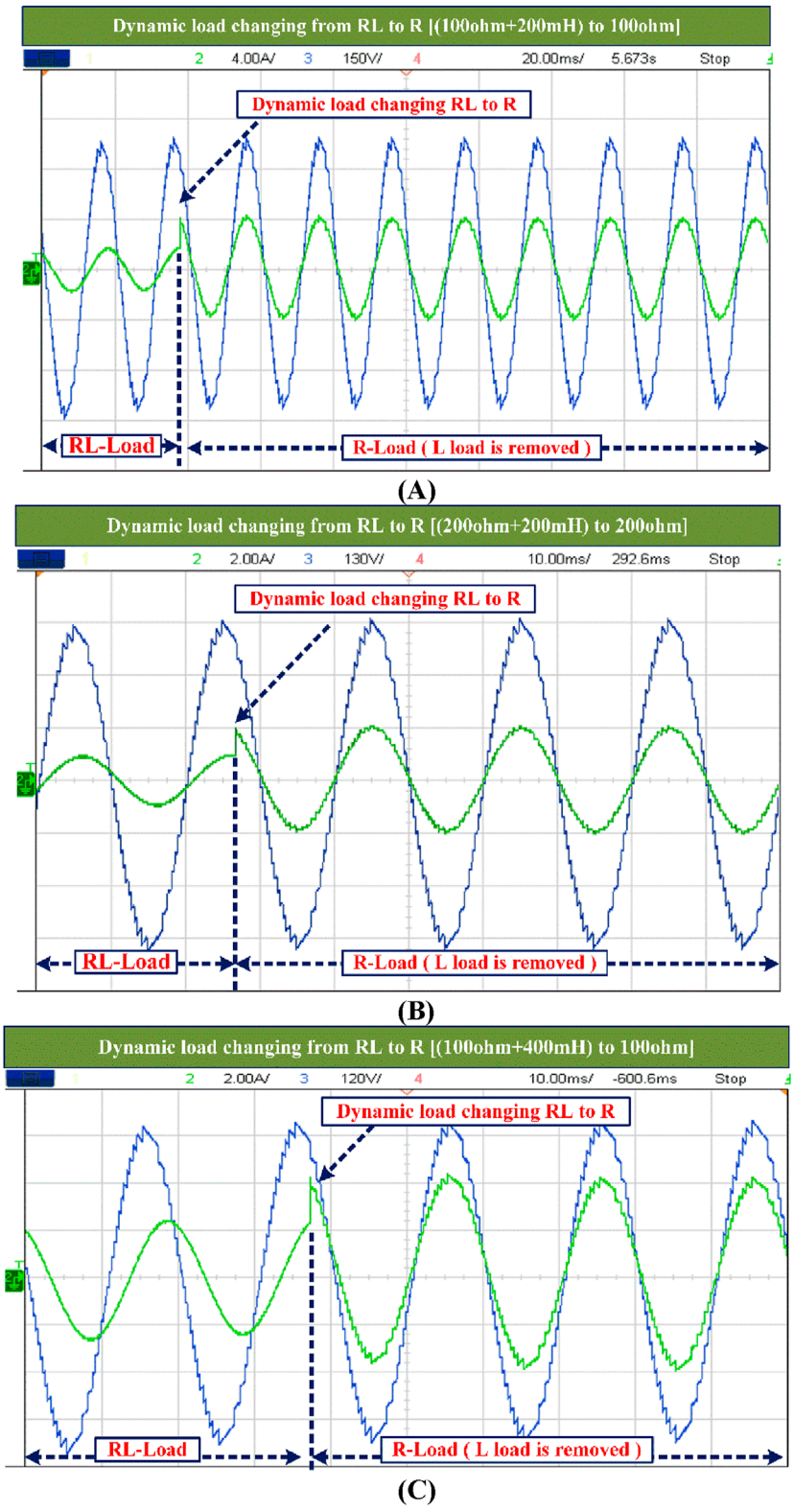


FIGURE 14
(Continued).

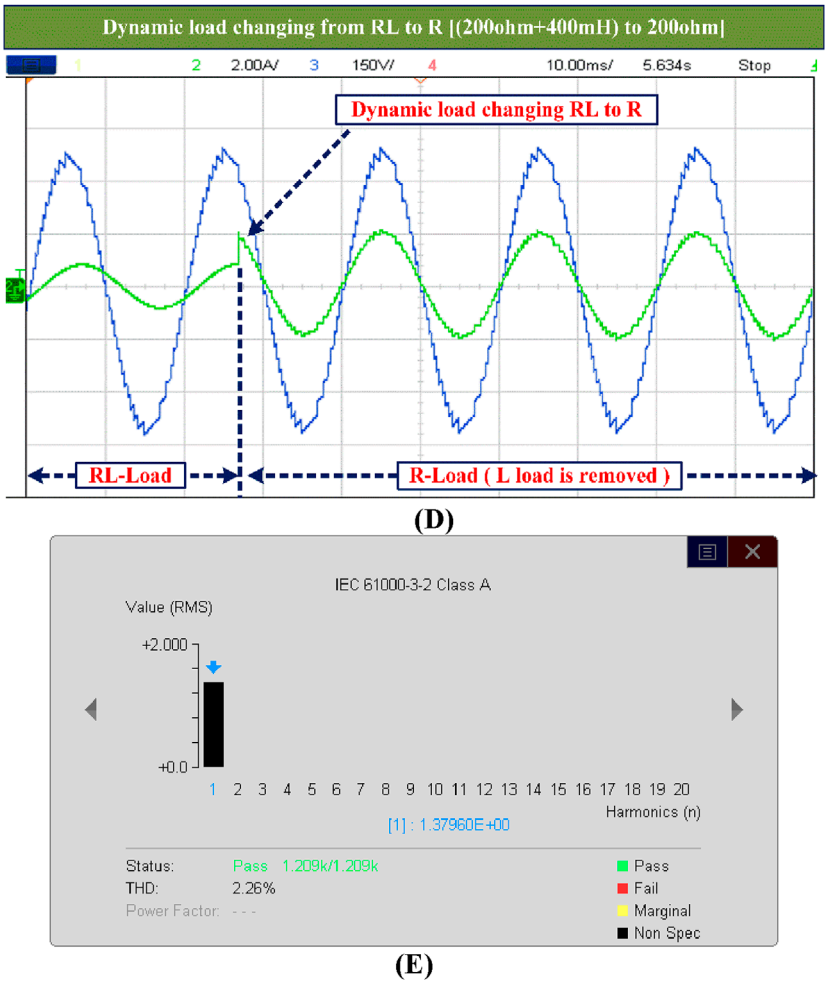


FIGURE 14
(Continued). Experimental voltage and current waveforms for dynamic load changes from RL- to R-load. **(A)** {100 Ω + 200 mH} to 100 Ω. **(B)** {200 Ω + 200 mH} to 200 Ω. **(C)** {100 Ω + 400 mH} to 100Ω. **(D)** {200 Ω + 400 mH} to 200Ω. **(E)** Experimental THD of suggested MLI.

Figures 15A, B show each switch voltage stress distribution and the normalized voltage stress (%). The MLI design's maximum output voltage is $10V_{dc}$, which has 21 levels; however, the algebraic total of DC sources exceeds the switch's MBV ($7V_{dc}$). Despite unequal voltage stress across the switches in the suggested MLI architecture, four switches have a maximum voltage stress of $7V_{dc}$ (S_5, S_6, S_7, and S_8). The smallest voltage stress is 20% of the two power switches (S_A and S_B) and 30% intermediate voltage stress of the remaining four switches (S_1, S_2, S_3, and S_4). Therefore, to save money, the suggested MLI design aims to increase DC source intake while minimizing TSV and switches.

The TSV is given as the algebraic sum of MBV across individual switches and is expressed in Equations 24, 25, providing the TSV_{PU} value thus:

$$TSV = MBV_{SA} + MBV_{SB} + MBV_{S1} + - - - + MBV_{S8}, \quad (24)$$

$$\mathbf{TSV_{PU}^{Proposed}} = \frac{\mathbf{TSV}}{\mathbf{V_{O,max}}}. \quad (25)$$

The suggested topology $TSV^{Proposed}$ can be calculated using Equations 26, 27:

$$\mathbf{TSV^{Proposed}} = \mathbf{2}[\mathbf{MBV_{SA}}] + \mathbf{4}[\mathbf{MBV_{S1}} + \mathrm{MBV_{S5}}]$$

$$= \mathbf{4V_{dc}} + \mathbf{4}[\mathbf{3V_{dc}} + \mathbf{7V_{dc}}]$$

$$= [\mathbf{4V_{dc}} + \mathbf{12V_{dc}} + \mathbf{28V_{dc}}]$$

$$\mathbf{TSV^{Proposed}} = \mathbf{44V_{dc}}, \quad (26)$$

$$\mathbf{TSV_{PU}^{Proposed}} = \frac{\mathbf{44V_{dc}}}{\mathbf{10V_{dc}}} = \mathbf{4.4}. \quad (27)$$

TABLE 5 Voltage stress comparisons across power switches.

Switch	Voltage stress (V_{stress})	Normalized voltage stress (NV_{stress}) in (%)
S_1	$3V_{dc}$	$(3V_{dc}/10V_{dc}) = 30\%$
S_2	$3V_{dc}$	$(3V_{dc}/10V_{dc}) = 30\%$
S_3	$3V_{dc}$	$(3V_{dc}/10V_{dc}) = 30\%$
S_4	$3V_{dc}$	$(3V_{dc}/10V_{dc}) = 30\%$
S_5	$7V_{dc}$	$(7V_{dc}/10V_{dc}) = 70\%$
S_6	$7V_{dc}$	$(7V_{dc}/10V_{dc}) = 70\%$
S_7	$7V_{dc}$	$(7V_{dc}/10V_{dc}) = 70\%$
S_8	$7V_{dc}$	$(7V_{dc}/10V_{dc}) = 70\%$
S_A	$2V_{dc}$	$(2V_{dc}/10V_{dc}) = 20\%$
S_B	$2V_{dc}$	$(2V_{dc}/10V_{dc}) = 20\%$

Therefore, the suggested MLI's peak inverse voltage (PIV) can be calculated by Equation 28:

$$PIV^{Proposed} = (N_{lev} - 1) = 20V_{dc}. \quad (28)$$

4.2 Cost function (CF)

The cost function (CF) can be calculated using some quantitative aspects of the suggested topology, such as a number of DC sources (N_{DC}), switches (N_{Swi}), gate driver circuits (N_{Dri}), diodes (N_{Dio}), capacitors (N_{Cap}), and the per unit value of TSV (TSV_{pu}) of the topology (Prasad et al., 2021). Therefore, the CF can be calculated by Equation 29:

$$CF = \left(N_{Swi} + N_{DC} + N_{Dri} + N_{Dio} + N_{Cap} + \alpha\, TSV_{PU}\right). \quad (29)$$

In this calculation of the cost function, the weight coefficient α value should be considered lower than 1 as well as larger than 1. In order to best evaluate the cost function, the developed MLI uses an approximation of α values of 0.5 (<1) and 1.5 (>1) (Shaik and Dhanamjayulu, 2021). Equation 30 calculates the cost function per level:

$$\frac{CF}{N_{Lev}} = \frac{N_{Swi} + N_{Dio} + N_{Cap} + N_{Dri} + N_{DC} + \alpha\, TSV_{PU}}{N_{Lev}}. \quad (30)$$

Therefore, CF/N_{Lev} for the suggested 21-level MLI topology with α values of 0.5 and 1.5 are 1.20 and 1.409, respectively.

4.3 Power loss and efficiency calculation

Two notable power losses occur in multilevel inverters: conduction (P_{Cond}) and switching losses (P_{Swil}). Total conduction loss is determined by summing the conduction losses of both IGBTs (P_{CSW}) and anti-parallel diodes (P_{CD}) along the current path (Prasad and Dhanamjayulu, 2022). This can be expressed using Equations 31, 32:

$$P_{Cond}(t) = P_{CSW}(t) + P_{CD}(t), \quad (31)$$

$$P_{Cond}(t) = \left(\left[V_{Swi} + R_{SWi} i_m^{\beta}(t)\right] + \left[V_{Dio} + R_{Dio} i_m(t)\right]\right) i_m(t), \quad (32)$$

where i_m (4A) is the peak output current. The threshold voltages for power switches and diodes are V_{Swi} (4 V) and V_{Dio} (0.7 V). Similarly, R_{Swi} (0.001Ω) and R_{Dio} (0.001Ω) represent the power switch on-state resistance and diode, respectively. The datasheet specifies β (0.01) as the power switch specification constant. If N_{Swi} and N_{Dio} are the switches and diodes are conducting at the same time (t) to produce each level, then the average conduction loss is expressed using Equation 33:

$$P_{Cond} = \frac{1}{2\pi} \int_0^{2\pi} \left[N_{Swi}(t) P_{CSW}(t) + N_{Dio}(t) P_{CD}(t)\right] dt. \quad (33)$$

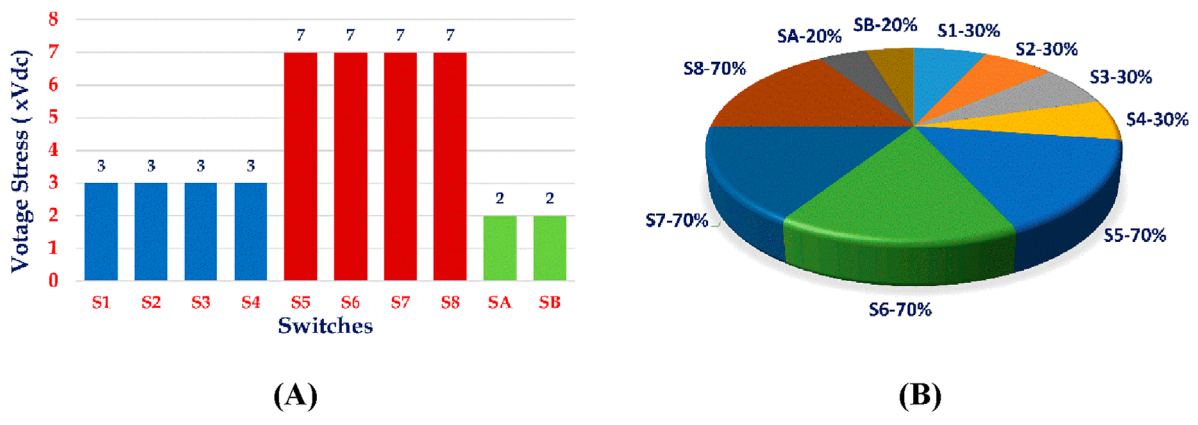


FIGURE 15
(A) Voltage stress distribution. **(B)** Normalized voltage stress in %.

TABLE 6 Summary of the proposed MLI power losses and efficiency.

Parameter/ Resistive loads	100 Ω	200 Ω	300 Ω	400 Ω
V_{rms} (V)	282.84	282.84	282.84	282.84
I_{rms} (A)	2.82	1.41	0.94	0.70
Output power P_{outp} (W)	797.61	398.80	265.86	197.98
Conduction loss P_{cond} (W)	18.82	13.40	11.25	10.70
Switching loss P_{swil} (W)	0.030	0.007	0.003	0.002
Total loss P_{Total} (W)	18.850	13.407	11.253	10.702
Input power P_{inp} (W)	816.46	412.20	277.11	208.68
% Efficiency (η)	97.69	96.74	95.93	94.87

100 Ω, 200 Ω, 300 Ω and 400 Ω are the resistive loads.

Switching loss (P_{Swil}) is the amount of power used when the switch turns on and off. This loss is calculated for the switch and the antiparallel diode. Equations 34–36 can be used to calculate the turn-on and -off energy loss (E_{on}, E_{off}):

$$E_{off-q} = \int_0^{t_{off}} (v(t)i(t))dt = \int_0^{t_{off}} \left[\left(\frac{V_{SWq}}{t_{off}}t\right)\left(-\frac{I}{t_{off}}(t-t_{off})\right)\right]dt, \quad (34)$$

$$E_{off-q} = \frac{1}{6}V_{SWq}It_{off}. \quad (35)$$

Similarly,

$$E_{on-q} = \int_0^{t_{on}} (v(t)i(t))dt = \int_0^{t_{on}} \left[\left(\frac{V_{SWq}}{t_{on}}t\right)\left(-\frac{I'}{t_{on}}(t-t_{on})\right)\right]dt$$

$$E_{on-q} = \frac{1}{6}V_{SWq}I't_{on}. \quad (36)$$

The time it takes to turn the switch off is t_{off}, the time to turn it on is a t_{on}, and the corresponding losses from the switch are $E_{off\text{-}q}$ and $E_{on\text{-}q}$, respectively. Although $V_{SW\,q}$ represents the voltage of the switch when it is in the off state, I and I^{I} represent the currents before and after the switch is turned on, respectively. The total switching losses can be calculated by Equation 37:

$$P_{Swil} = f\left[\sum_{q=1}^{N_{SW}}\left(\sum_{i=1}^{N_{on-q}} E_{on\,qi} + \sum_{i=1}^{N_{off-q}} E_{off\,qi}\right)\right]. \quad (37)$$

The fundamental frequency is denoted by f, $N_{on\text{-}q}$, and $N_{off,\text{-}q}$, and the number of times that the q^{th} switch is turned on or off during a single fundamental cycle. Therefore, the overall power losses is expressed using Equation 38:

$$P_{Total} = P_{Cond} + P_{Swil}. \quad (38)$$

The output power can thus be calculated by Equation 39:

$$P_{outp} = V_{rms} * I_{rms}. \quad (39)$$

The total efficiency (η) can be calculated using Equation 40:

$$\%\,\eta = \frac{P_{outp}}{P_{inp}} = \frac{P_{outp}}{P_{outp} + P_{Total}}x100, \quad (40)$$

where P_{outp} and P_{inp} are the output and input powers. Table 6 summarizes the power losses and efficiency of the suggested MLI. The efficiency for various loads is graphically illustrated in Figure 16.

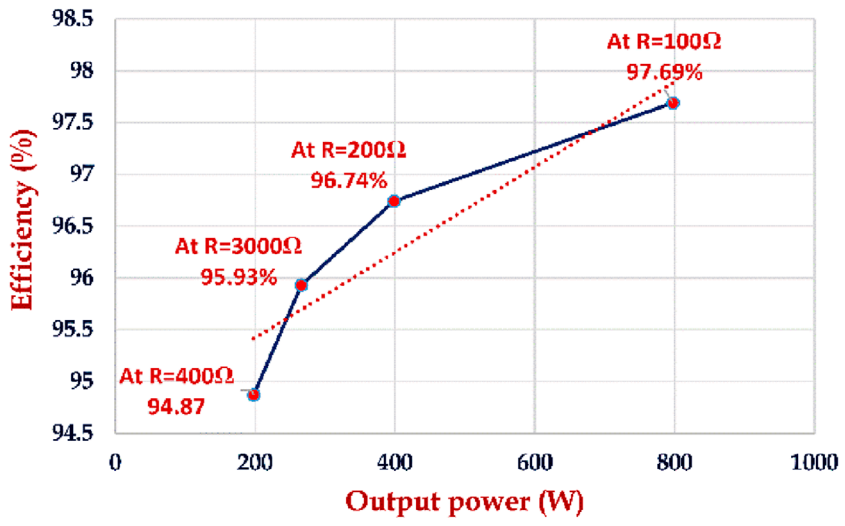
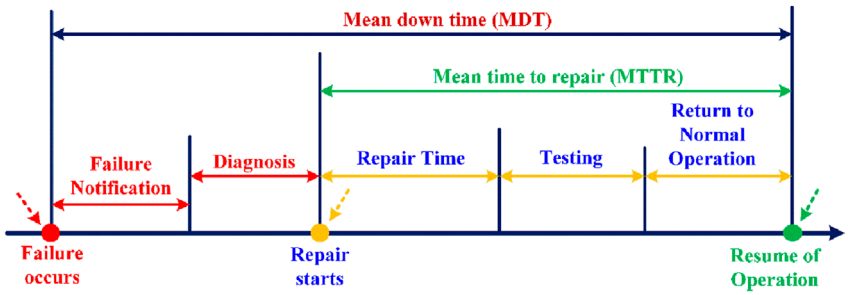
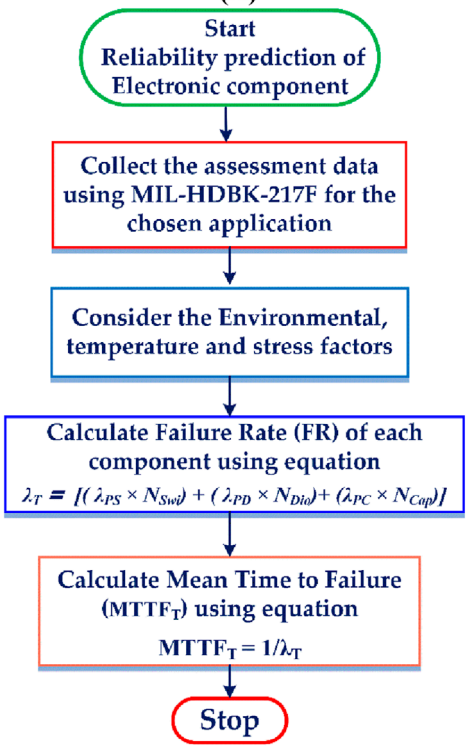


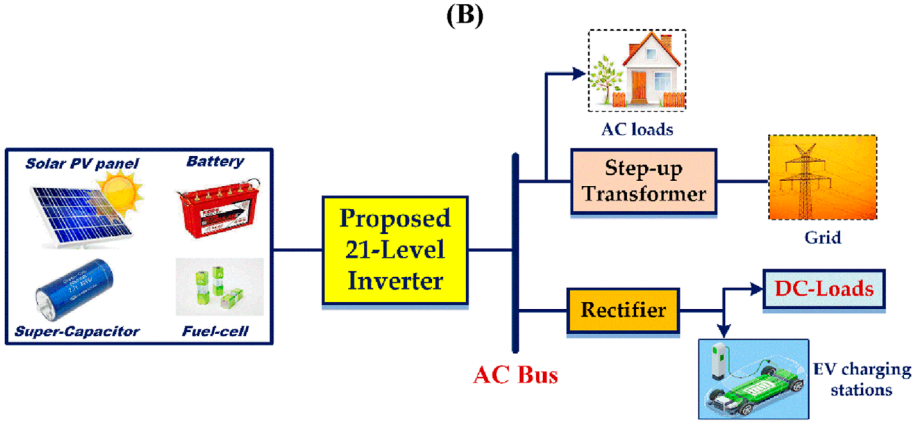
FIGURE 16
Efficiency of proposed MLI at different loads.



(A)



(B)



(C)

FIGURE 17
(A) Mean downtime and mean time to repair a generic component. **(B)** Flowchart of reliability analysis. **(C)** Applications of the proposed MLI.

TABLE 7 Failure rates of each component using the approximation method (Shaik et al., 2023).

S.no.	Component	Failure rate (failures/hour)
1	Switches	$250^{*}10^{-9}$
2	Diodes	$100^{*}10^{-9}$
3	Capacitors	$300^{*}10^{-9}$

4.4 Reliability assessment

The reliability study determines the equipment's predicted lifetime and failure rate, which are crucial to determining the health of any electronic device. Manufacturing organizations can profit from this reliability study as they seek long-lasting, high-performing, and low-maintenance products, and the industry can also estimate the mean time-to-repair and mean downtime to resume operations (Figure 17A). Therefore, an estimation of how long a device will survive is essential. To determine a device's reliability, several factors are considered.

$MTTF_T$ and FR_T are the key reliability assessment requirements. The hazard rate (λ_T) is a prediction of failure over a certain timeframe. When FR is time-invariant, R(t) is reliability. Approximation and precise methods are preferred in power electronic circuit reliability testing. The mean time to the first failure is initially calculated to determine device durability. A high mean-time-to-failure ($MTTF_T$) indicates reliability. This and the failure rate (FR_T) of a device can be determined using MIL-HDBK 217E standard handbooks (Shaik et al., 2023). The approximation approach simplifies and accurately predicts FR_T values for switches, diodes, and capacitors (mentioned in detail in Table 7), and the flowchart is shown in Figure 17B to calculate the $MTTF_T$ value.

Furthermore, as shown in Figure 17C, the suggested MLI keeps its self-voltage balanced, a unique quality that makes it suitable for a wide range of applications such as solar PV systems, fuel cells, battery-powered applications, and industrial generators. In addition, the suggested MLI might be used in medium-power micro-grids and grid configurations, offering a reliable solution for the problem of remote electrification.

The total MTTFT is estimated from power electronic circuit element FR values. Equation 41 is used to calculate λ_T:

$$\lambda_T = \left[\left(\lambda_{PS} \times N_{Swi}\right) + \left(\lambda_{PD} \times N_{Dio}\right) + \left(\lambda_{PC} \times N_{Cap}\right)\right]. \quad (41)$$

Equation 42 is used to calculate the power electronic circuit $MTTF_T$:

$$\mathbf{MTTF_T} = \frac{\mathbf{1}}{\boldsymbol{\lambda T}}. \quad (42)$$

The suggested MLI architecture was compared with numerous quantitative features of the existing MLI topologies, including the number of DC sources (N_{DC}), power switches (N_{Swi}), gate drivers (N_{Dri}), diodes (N_{Dio}), capacitors (N_{Cap}), and component count per number of levels (CC/N_{Lev}). When it comes to qualitative comparisons such as the TSVpu, THD, CF, FR_T, and $MTTF_T$ features, Table 8 presents quantitative and qualitative comparisons of the proposed 21-level MLI with existing topologies. All these comparisons indicate that the suggested 21-level MLI architecture is more economical, cost-effective, and achieves better performance outcomes.

5 Conclusion and future scope

This research proposed a novel 21-level MLI architecture for solar PV energy systems with fewer components. In addition, an EINC-based MPPT technique was used for constant PV panel power generation, even in partially shaded situations. The proposed MLI was tested for different loads, including R, RL, R-RL, and RL-R loads. The suggested MLI is simulated in MATLAB/Simulink and validated experimentally using hardware. The qualitative and quantitative comparative analysis with existing architectures demonstrates that the price, size, and TSV of the proposed MLI are reduced. The efficiency is 97.69%, and the CF/N_{Lev} for different weight coefficient ($\alpha = 0.5$ and $\alpha = 1.5$) values is 1.20 and 1.40, respectively. The reliability study parameter of λ_T is 0.0000025 failures/hour and $MTTF_T$ of 400000 h/failure are improved from the findings. The simulated THD is 2.06%, and the experimental THD is 2.26% under the IEEE standards. This suggested architecture can provide high-quality power from PV systems and improve power quality, voltage, and reactive power support for grid-connected systems, FACTS, RES, and EV applications. This research can also be appropriate for a battery storage system that the hotel and residential sectors can supply for emergency and standalone services.

Data availability statement

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation.

Author contributions

SN: conceptualization, formal analysis, investigation, methodology, software, validation, visualization, writing–original draft, and writing–review and editing. CD: investigation, methodology, project administration, resources, supervision, validation, visualization, and writing–review and editing.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

TABLE 8 Quantitative and qualitative comparisons of the proposed 21-level MLI.

	Quantitative parameters							
	Reference	N_{Lev}	N_{DC}	N_{Swi}	N_{Dri}	N_{Dio}	N_{Cap}	CC/N_{Lev}
Similar	Das et al. (2020)	21	4	12	12	0	0	1.33
	Rao et al. (2018)	21	4	13	13	0	0	1.42
	Siddique et al. (2020)	21	4	16	16	0	0	1.71
	Omer et al. (2020b)	21	4	11	11	0	0	1.23
	Sabyasachi et al. (2020)	21	3	14	14	0	0	1.47
	Sarwer et al. (2020)	21	7	16	16	0	0	1.85
	Meraj et al. (2020)	21	6	10	10	6	3	1.66
Proposed MLI		**21**	**3**	**10**	**10**	**0**	**0**	**1.09**
Others	Shaik and Dhanamjayulu (2021)	17	3	10	10	0	0	1.35
	Montazer et al. (2021)	19	5	11	10	2	0	1.47
	Thakre et al. (2019)	23	6	12	12	0	0	1.30
	Samadaei et al. (2016)	25	8	20	16	0	0	1.76
	Alishah et al. (2016)	31	6	16	16	0	0	1.22
	Samadaei et al. (2018)	33	8	24	18	0	0	1.51

	Qualitative parameters							
	Reference	N_{Lev}	TSV_{PU}	%THD	CF/N_{Lev}		λ_T (Failures/hour)	$MTTF_T=(1/\lambda_T)$ (Hours/failure)
					$\alpha = 0.5$	$\alpha = 1.5$		
Similar	Das et al. (2020)	21	4.50	6.67	1.44	1.65	0.0000030	333333.33
	Sinha et al. (2018)	21	5.50	6.43	1.41	1.67	0.0000030	333333.33
	Rao et al. (2018)	21	4.60	7.13	1.53	1.75	0.0000032	312500
	Siddique et al. (2020)	21	4.40	5.85	1.81	2.02	0.0000040	250000
	Omer et al. (2020b)	21	4.40	7.69	1.34	1.55	0.0000027	370370.37
	Sabyasachi et al. (2020)	21	5.60	-	1.60	1.87	0.0000035	285714.28
	Meraj et al. (2020)	21	4.40	4.28	1.77	1.98	0.0000040	250000
Proposed MLI		**21**	**4.40**	**2.26**	**1.20**	**1.40**	**0.0000025**	**400000**
Others	Shaik and Dhanamjayulu (2021)	17	7.05	4.12	1.56	1.97	0.0000025	400000
	Montazer et al. (2021)	19	4.66	3.20	1.59	1.84	0.0000029	344827.58
	Thakre et al. (2019)	23	11.45	4.84	1.55	2.05	0.0000030	333333.33
	Samadaei et al. (2016)	25	6.30	4.91	1.88	2.13	0.0000050	200000
	Alishah et al. (2016)	31	4.60	3.96	1.30	1.44	0.0000040	250000
	Samadaei et al. (2018)	33	5.20	4.27	1.59	1.75	0.0000060	166666.66

Publisher's note

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Nomenclature

α	weight coefficient value
E_{on}, E_{off}	energy consumption of on–off switches
STM	standard testing measurement
R_{se}, R_{pa}	series and shunt resistances of the PV cell equivalent circuit
K	Boltzmann constant
T	temperature
δ	duty cycle of boost converter
f_S	switching frequency
THD	total harmonic distortion
CF/N_{Lev}	cost function per level
TSV_{pu}	total standing voltage per unit
V_{OC}	open-circuit voltage of the PV module
I_{SC}	short-circuit current of the PV module
I_{Di}	saturation current of a diode
MPPT	maximum power point tracking
EINC	enhanced incremental conductance
P&O	perturb and observe
V_{Suni}	voltage stress on unidirectional switch
V_{ref}	reference voltage
λ_T	total failure rate
$\lambda_{PS}/\lambda_{PD}/\lambda_{PC}$	failure rate of switches/failure rate of diodes/failure rate of capacitors
$MTTF_T$	total mean time to failure
V_{rms}/I_{rms}	output RMS voltage and current
V_{Sbi}	voltage stress on bidirectional switch
P_{Total}	total power loss
G	irradiance
V_{cr}	carrier signal voltage
T_R	reference temperature
N_{Swi}/N_{Dri}	number switches/number of gate driver circuits
V_{Swi}	voltage across the i^{th} switch
FR_T	failure rate
N_{Cap}/N_{Dio}	number capacitors/number of diodes
R_{Swi}/R_{Dio}	resistance of the switch/resistance of diode
V_m	maximum voltage of the reference signal
M_a	modulation index
V_{dc}	DC source voltage
N_{Lev}/N_{DC}	number of levels/number of DC sources
β	power switch specification constant
P_{swil}	switching power losses
P_{cond}	conduction power losses
P_{outp}	output power
P_{inp}	input power
i_m	maximum output current
P_{CSW}/P_{CD}	conduction power loss of switches/conduction power loss of diodes
t	total time period
t_{off}/t_{on}	turn-off and turn-on timings