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# A digital hysteresis control method for three-level grid-tie inverter based on online prediction of sampling time without inductance

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This article proposed a digital hysteresis control method for three-level grid-tie inverter based on online prediction of sampling time without inductance. The proposed method eliminated the effect on the control accuracy of the inductor changing with the current in the LCL filter of the grid-tie inverter, and reduced the equivalent sampling rate in digital hysteresis control by predicting and correcting the sample time. The simulations and experimental tests confirm the effectiveness of the proposed digital hysteresis control method.

KEYWORDS

**three-level inverter, grid-tie inverter, digital hysteresis control, online prediction of sampling time, robustness of inductor parameters**

## 1 Introduction

GRID-TIE inverters are widely used in various distributed generation (DG) systems powered by solar photovoltaic (PV) arrays or wind power. Among the control algorithms used in the grid-tie inverters, the hysteresis control algorithm has many advantages compared with the traditional PID (Proportion Integration Differentiation) control algorithm: it can track any form of the command signal, the tracking error accuracy can be controlled and adjusted, and the control bandwidth is extremely high (Chavali et al., 2022). Therefore, it is widely used in harmonic suppression, noise filtering, and other occasions to improve power quality and electromagnetic protection in micro-grid (Viswadev et al., 2020; Wang et al., 2014). Hysteresis control algorithms have undergone development from analog hysteresis control to digital hysteresis control. Analog hysteresis control has high tracking accuracy and good control effect because the controlled signal is a real-time continuously changing analog quantity, but it relies heavily on the performance and cost of analog chips, which leads to its application being limited (He et al., 2013). In contrast, digital hysteresis control is the future direction because of its flexibility and low dependence on the microchip, which has great demand in many applications (Acuna et al., 2015; Davoodnezhad et al., 2014a). However, the accuracy of digital hysteresis control is limited by the discretization and sampling rate (Wang and Wang, 2013), which has a great influence.

As shown in Figure 1, the blue and orange waveforms in the first graph of figure (a) and (b) represent the bandwidth of the hysteresis control, indicating the upper and lower limits of the error tolerance. The red waveform indicates the command signal and the green

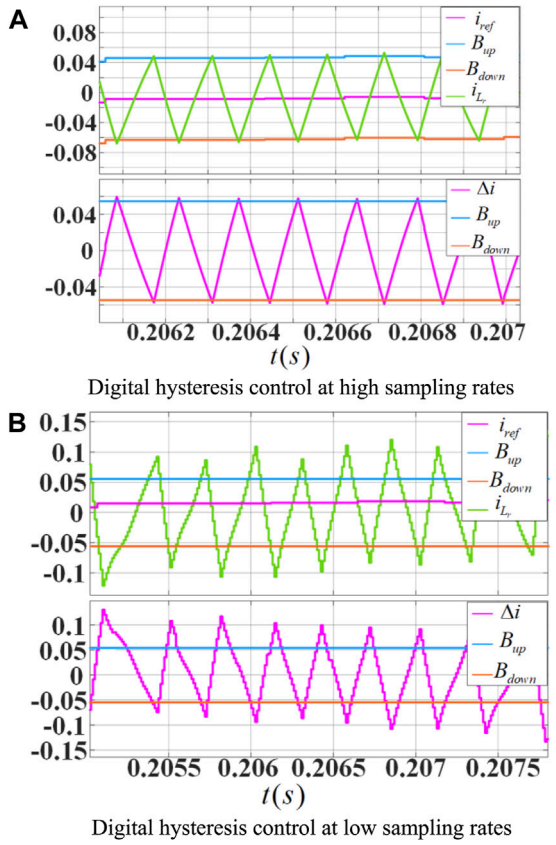


FIGURE 1
Digital hysteresis control at different sampling rates. **(A)** Digital hysteresis control at high sampling rates, **(B)** Digital hysteresis control at low sampling rates.

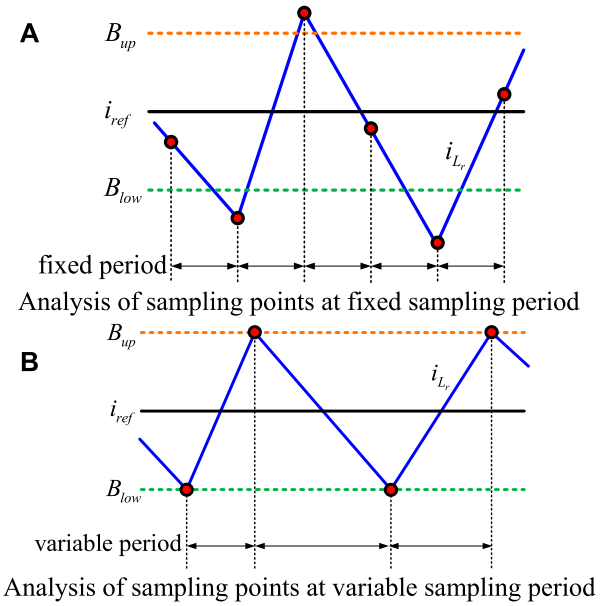


FIGURE 2
Analysis of sampling points at different sampling periods. **(A)** Analysis of sampling points at fixed sampling period, **(B)** Analysis of sampling points at variable sampling period.

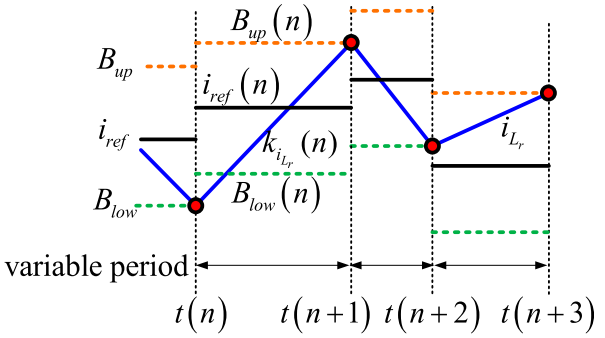


FIGURE 3
Schematic diagram of sampling time prediction at a minimum sampling rate.

waveform indicates the actual controlled signal. The red waveform in the second graph of figure (a) and figure (b) indicates the error signal. The blue signal indicates the absolute value of the bandwidth. From the comparison of the graphs, it can be seen that under a high sampling rate, the error current is close to a continuous analog signal, and the error is always kept within the hysteresis bandwidth during all the control process. While under a low sampling rate, it is difficult to accurately capture the signal at the moment of intersection of the error signal and the bandwidth, making the error signal greatly exceed the allowed boundary range, showing low precision and poor control effect.

In actual products, the ADC sampling rate of the digital controller cannot be too high, otherwise the control algorithm cannot be completed during one control period before the next data refresh. Therefore, it is of great practical importance to study how to reduce the impact of sampling rate on digital hysteresis control under the premise of ensuring control accuracy.

In the past few years, several improvements have been proposed, particularly focusing on reducing the hysteresis control equivalent sampling frequency and improving the current tracking effect (Malesani et al., 1997; Carl et al., 2009). In (Malesani et al., 1997; Stefanutti and Mattavelli, 2006; Hu et al., 2014), several digital hysteresis control methods based on oversampling and virtual sampling were proposed, but the sampling rates are high, the amount of data is too large, and the authenticity of the virtual sampling data needs to be further verified. In (Chen and Kang, 2011), a hysteresis control method with online prediction of sampling time is used, which can predict the next sampling time to ensure the effect of current tracking at a reduced sampling rate, but this method does not take into account the problem of inductor parameters changing with current, making the predicted values deviate in the practical application. In Carl et al. (2009), the error of the hysteresis control at different stages is analyzed and a method to increase the current tracking accuracy by changing the number of switch levels at the moment of maximum error is proposed, but the switching process of this method is complicated and the loss to the device is great.

In this paper, a novel online sampling prediction control method without inductance is proposed. With the proposed scheme, the

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TABLE 1 Three-level converter switching state modulation relationship.

| $S_{1a}$ | $S_{2a}$ | $\overline{S_{1a}}$ | $\overline{S_{2a}}$ | $E_g$ | $V_x$ | $\frac{di_{Lr}}{dt}$ |
|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | >0 | $\frac{U_{dc}}{2}$ | $1\times\frac{\frac{U_{dc}}{2}-E_g}{L_r}$ |
| 0 | 1 | 1 | 0 | >0 | 0 | $0\times\frac{\frac{U_{dc}}{2}-E_g}{L_r}$ |
| 0 | 1 | 1 | 0 | <0 | 0 | $0\times\frac{\frac{U_{dc}}{2}-E_g}{L_r}$ |
| 0 | 0 | 1 | 1 | <0 | $-\frac{U_{dc}}{2}$ | $-1\times\frac{\frac{U_{dc}}{2}-E_g}{L_r}$ |

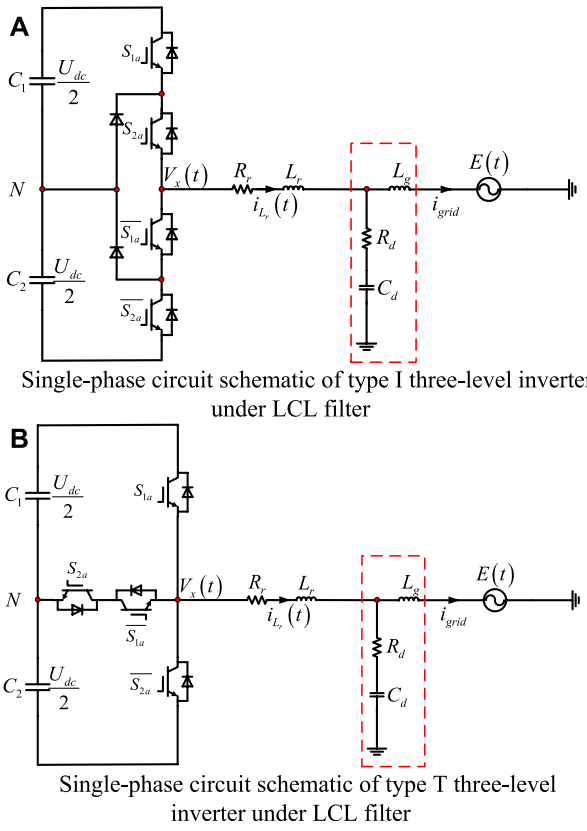


FIGURE 4
Single-phase circuit schematic of different type three-level inverter under LCL filter. **(A)** Single-phase circuit schematic of type I three-level inverter under LCL filter, **(B)** Single-phase circuit schematic of type T three-level inverter under LCL filter.

following advantages are obtained. (1) the digital hysteresis equivalent sampling frequency is reduced compared with the oversampling digital hysteresis method by the prediction control method. (2) the control accuracy is guaranteed by analyzed the error current within and beyond the hysteresis bandwidth so that the hysteresis error is fixed. (3) the problem of inductor parameters changing with current to the hysteresis control is solved.

The rest of this paper is organized as follows. In Section 2, the sampling prediction method of the digital hysteresis control for the three-level inverter is derived and the effect of inductor parameters on the control accuracy is analyzed. In Section 3, the inductance-free

TABLE 2 Simulation main circuit parameters table.

| Main components | Parameters |
|---|---|
| DC Capacity $C_1$、 $C_2$ | 9840$uF$ |
| Converter side Inductor $L_r$ | 0.7 $mH$ |
| Grid side Inductor $L_g$ | 0.05 $mH$ |
| AC Filter Capacitor $C_d$ | 30 $uF$ |
| DC voltage $U_{dc}$ | 750 V |
| Grid voltage RMS $E_{grid}$ | 380 V |
| Grid frequency $f_{grid}$ | 50 Hz |
| Target switching frequency $f_s$ | 15 kHz |

A. Simulation results of conventional three-level digital hysteresis control.

sampling time online prediction control method is derived. In Sections 4 and 5, the simulation and experimental results are presented in detail.

## 2 Principle of digital hysteresis control with sampling time prediction algorithm based on three level inverter

According to the traditional hysteresis control algorithm (Chen et al., 2012; Jiao et al., 2014) (take the current-source power electronic converter as an example), if the current sampling value is located on the boundary of the hysteresis bandwidth at each sampling moment, the converter will act at this time, and the sampling moment is valid; On the contrary, if the current sampling value at the sampling moment is within the bandwidth of the hysteresis control, the converter does not act, so the sampling point does not affect the control system, then it is meaningless. Therefore, the minimum sampling rate occurs at the moment when all the sampling points of the controlled current are located at the intersection of the bandwidth boundary of the hysteresis control (Liu and Maswood, 2006; Mohseni and Islam, 2010; Wang and Li, 2013), as shown in Figure 2.

As shown in Figure 2A, the red sampling points are inside the upper and lower boundary of the hysteresis bandwidth, which cannot trigger the converter to switch, and the sampling value is meaningless to the hysteresis control system; on the contrary, in Figure 2B, as each sampling current value is located on the upper and lower boundary of the bandwidth, it just makes the converter to switch, which is timely

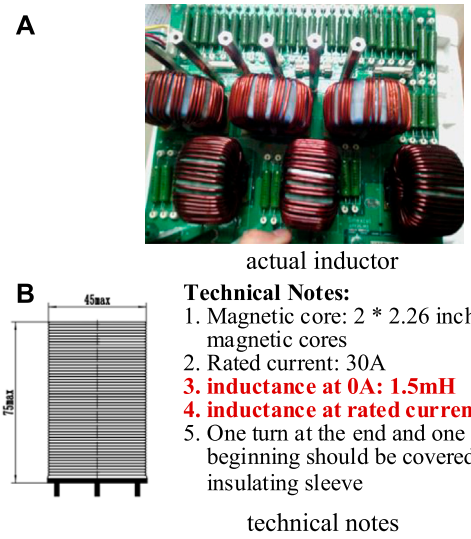


FIGURE 5
Actual inductor fabrication process. **(A)** actual inductor, **(B)** technical notes.

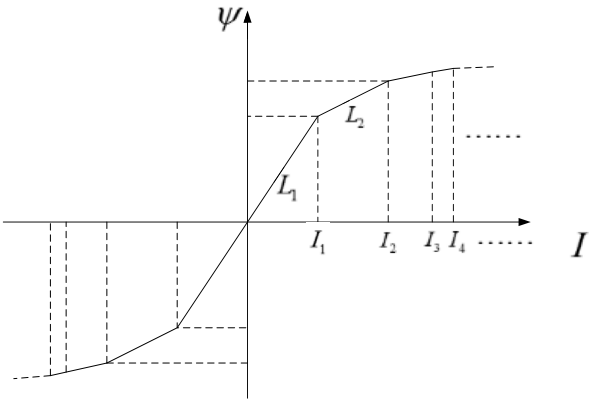


FIGURE 6
Variation curve of actual inductor flux versus inductance at different current.

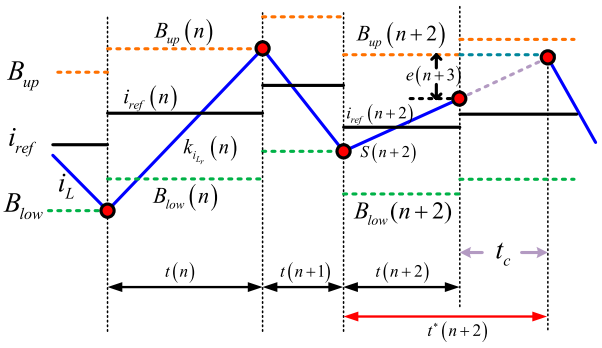


FIGURE 7
Schematic diagram of sampling time prediction correction.

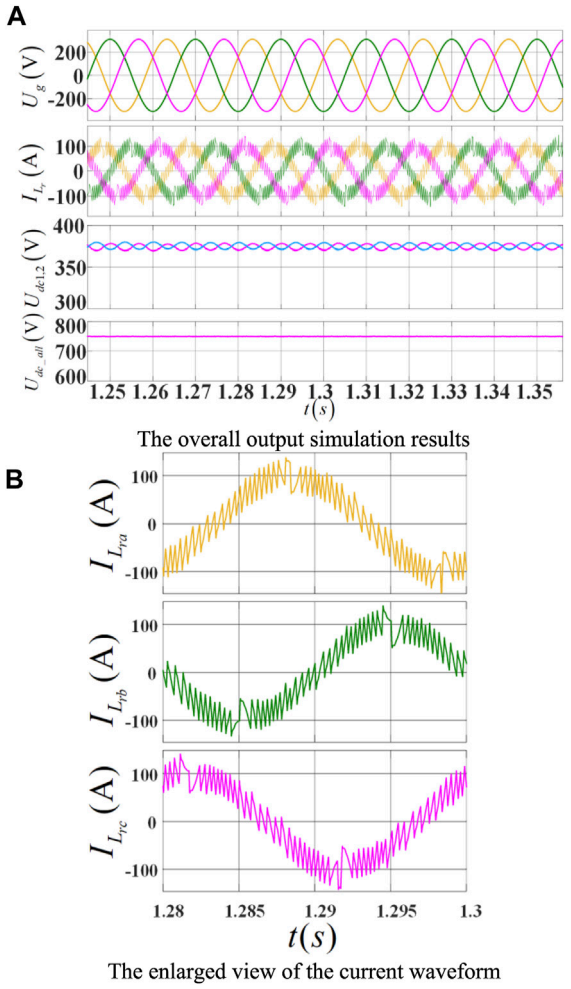


FIGURE 8
Inverter output simulation results under conventional digital hysteresis control. **(A)** The overall output simulation results, **(B)** The enlarged view of the current waveform.

and effective. Due to the changes in the control reference, hysteresis bandwidth, and hardware parameters as well as external disturbances in the actual control system, the interval between sampling points or the sampling rate, is bound to change constantly if all sampling points are located on the bandwidth boundary of the hysteresis control, as shown in Figure 2B. Therefore, simply using the traditional ideal fixed sampling rate as shown in Figure 2A cannot meet the requirements of the actual sampling interval changes, which poses a challenge to reduce the sampling rate while ensuring the control accuracy. Therefore, it is important to study how to improve the effectiveness of digital hysteresis control and how to reduce the equivalent sampling rate.

According to the analysis, it can be known that: at each sampling point, the time required for the current to reach the next bandwidth intersection position can be deduced from the actual sampled current value, as well as the commanded current given by the algorithm, the upper and lower limits of the hysteresis

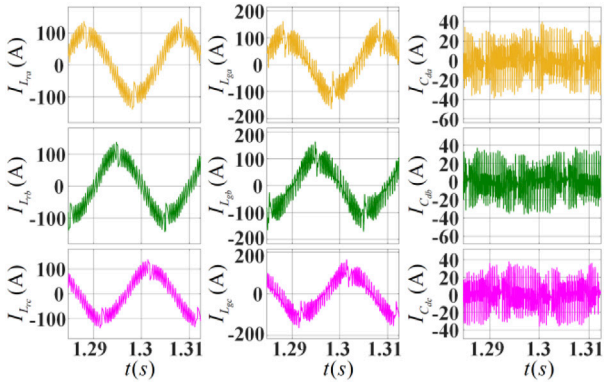

FIGURE 9
Waveform of LCL filter current of the three-level inverter under traditional digital hysteresis control algorithm.

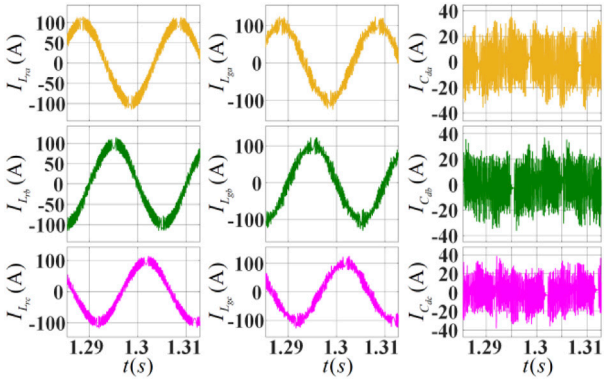

FIGURE 11
Inverter LCL filter current waveform under the proposed inductance-free digital hysteresis sampling time online prediction algorithm.

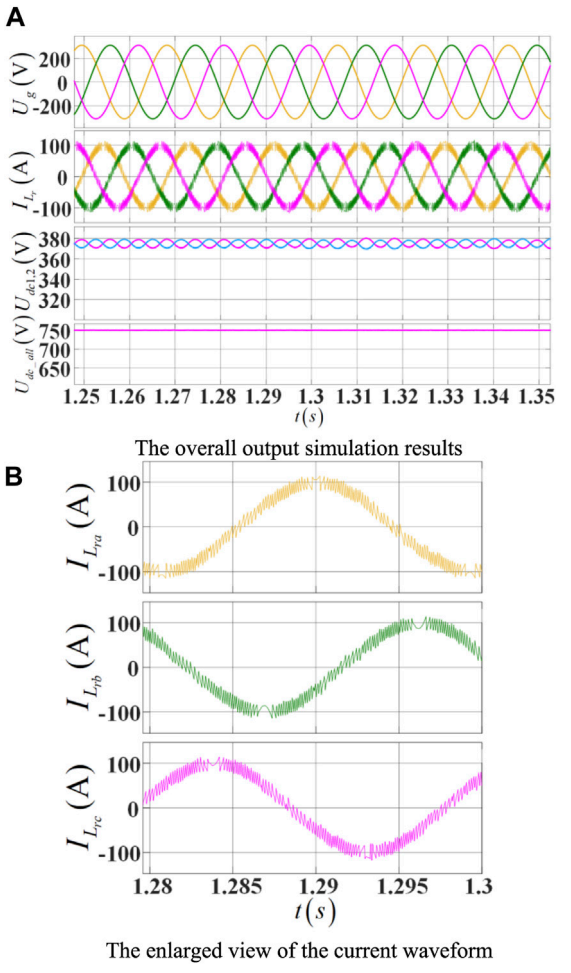


FIGURE 10
Inverter output results under the proposed digital hysteresis prediction algorithm. **(A)** The overall output simulation results, **(B)** The enlarged view of the current waveform.

bandwidth, and this time will be set as the next sampling period, then the ideal equivalent minimum sampling rate can be obtained in Eq. 1, as shown in Figure 3.

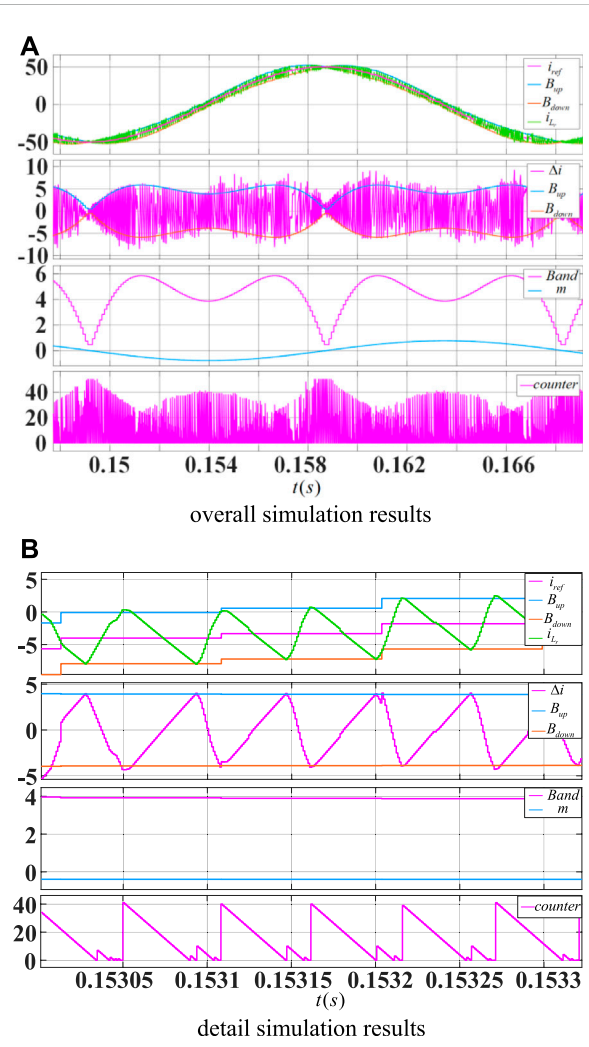


FIGURE 12
Simulation results of bandwidth versus error current and prediction time variation under the proposed digital hysteresis sampling time online prediction algorithm. **(A)** overall simulation results, **(B)** detail simulation results.

TABLE 3 Experimental main circuit parameters table.

| Main components | Parameters |
|---|---|
| DC Capacity $C_1$、 $C_2$ | 9840$uF$ |
| Converter side Inductor $L_r$ | 0.7 $mH$ |
| Grid side Inductor $L_g$ | 0.05 $mH$ |
| AC Filter Capacitor $C_d$ | 30 $uF$ |
| DC voltage $U_{dc}$ | 750 V |
| Grid voltage RMS $E_{grid}$ | 380 V |
| Grid frequency $f_{grid}$ | 50 Hz |
| Target switching frequency $f_s$ | 15 kHz |

A. experimental results of conventional digital hysteresis control.

$$\Delta T = t(n+1) - t(n) = \frac{B_{up}(n) - i_{L_r}(n)}{k_{i_{L_r}}(n)}. \tag{1}$$

Where $B_{up}(n) = i_{ref}(n) + H$, and H is the hysteresis bandwidth. $k_{i_{L_r}}(n)$ indicates the slope of current at sampling time $t(n)$.

As can be seen from the above equation, the slope of the current has a critical impact on the sampling rate.

The following is an example of a Type I and Type T three-level inverter.

From the single-phase topology of the three-level inverter, the series equivalent resistance $R_r$ of the inverter-side inductor $L_r$ is neglected, and the general LCL-type filter is usually designed with a grid-side inductor $L_g \ll L_r$, so the voltage drop on the grid-side inductor $L_g$ can also be neglected, which leads to:

$$L_r \frac{di_{L_r}(t)}{dt} = V_x(t) - E(t) \tag{2}$$

In Eq. 2, the $L_r$ represents the inverter-side inductor in Figure 4, the $V_x(t)$ represents the terminal voltage of the inverter, typically the PWM (pulse width modulation) voltage, and the $E(t)$ represents the grid voltage.

Then, according to the modulation law of the three-level switching state (Shen et al., 2011; Stefanutti and Mattavelli, 2006), the following Table 1 of switching states can be obtained.

In Table 1, $S_x$ $(x = 1a, 2a)$ represent the state of the switch in one arm at the bridge of the three-level inverter. $E_g$ represent the grid voltage. And the first row of Table 1 in orange color represents the positive level of the three level inverter, the last row in blue color represents the negative level, and the middle two rows in gray color represents the zero level of the three level inverter.

From this, it can be seen that:

$$k_{i_{L_r}} = \frac{di_{L_r}}{dt} = \begin{cases} \dfrac{S_{1a} \times \dfrac{U_{dc}}{2} - E_g}{L}, \left(E_g > 0\right) \\ \dfrac{(S_{2a} - 1) \times \dfrac{U_{dc}}{2} - E_g}{L}, \left(E_g < 0\right) \end{cases} \tag{3}$$

In Eq. 3, $k_{i_{L_r}} = \frac{di_{L_r}}{dt}$ indicates the slope of the current of the inverter-side inductor. The $S_{1a}$ and $S_{2a}$ represents the switching state of the first two of four switching devices in one arm of the inverter in Figure 4. And the $U_{dc}$ represents the total voltage of the DC capacity in inverter.

Thus, the conventional sampling time prediction algorithm for digital hysteresis control of three-level converter can be obtained as follows:

$$\begin{cases} \Delta T = t(n+1) - t(n) = \dfrac{B_{up}(n) - i_{L_r}(n)}{k_{i_{L_r}}(n)} \\ k_{i_{L_r}}(n) = \dfrac{S_0 \times \dfrac{U_{dc}}{2} - E_g}{L} \\ S_0 = \begin{cases} S_{1a}, E_g(t) > 0 \\ S_{2a} - 1, E_g(t) < 0 \end{cases} \end{cases} \tag{4}$$

where $S_0$ is the switch state corresponding to the moment of the sampling point. The $\Delta T$ is the period of the digital hysteresis control.

Combined with the above analysis, it can be seen that the sampling moment predicted by the traditional digital hysteresis control algorithm is closely related to the inductance $L$. However, in actual products, due

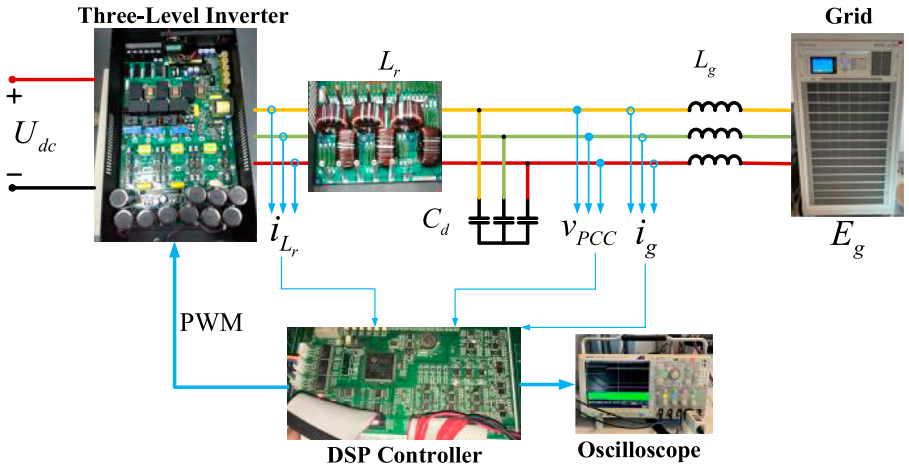


FIGURE 13
Configuration of the experimental setup.

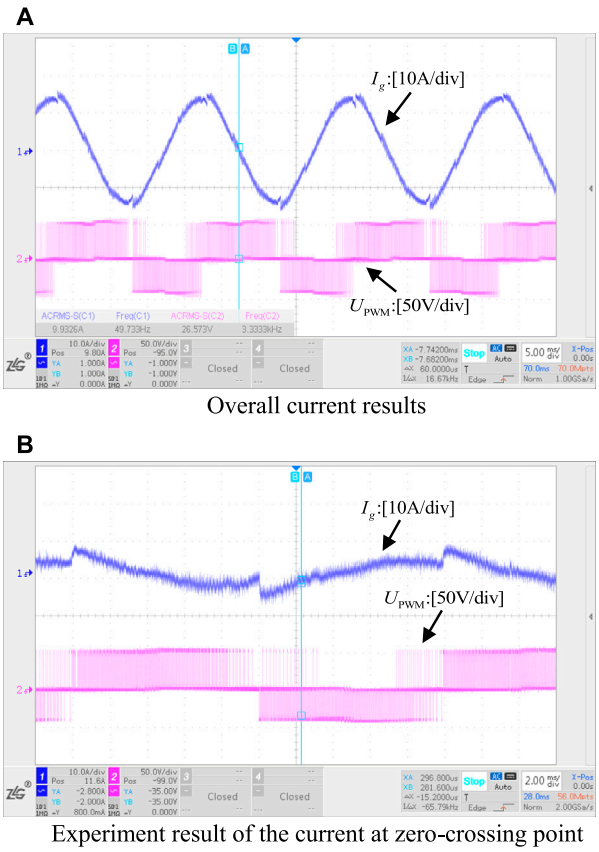


FIGURE 14
Output current and switch voltage of experiment results on conventional digital hysteresis control method. **(A)** Overall current results, **(B)** Experiment result of the current at zero-crossing point.

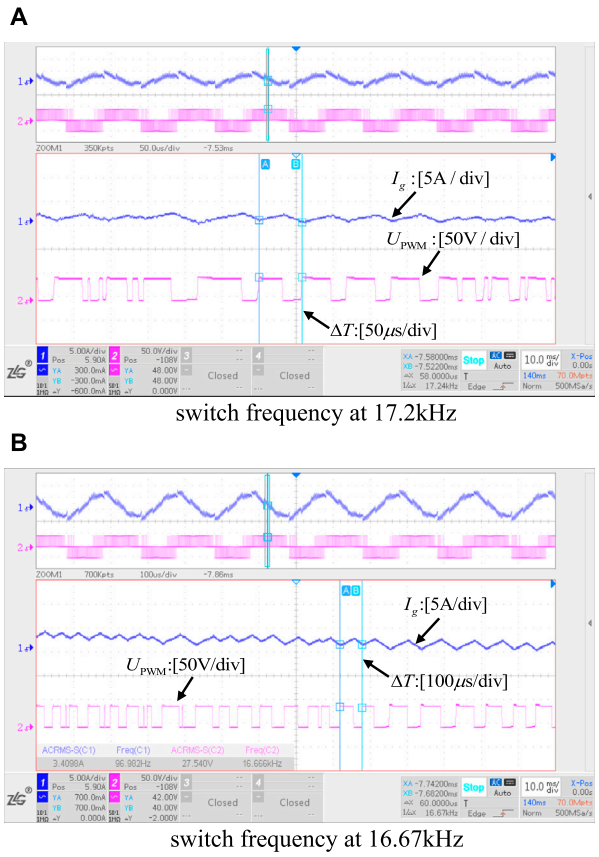


FIGURE 15
Different switching state of convention digital hysteresis control. **(A)** switch frequency at 17.2 kHz, **(B)** switch frequency at 16.67 kHz.

to cost and process limitations, the total amount of flux that the core of the inductor can hold is certain, and when the flux is saturated, it makes the inductance change drastically. Therefore, the corresponding inductance is different for various current output conditions. Usually, manufacturers design the nominal inductance according to the empty load current, which can cause the actual inductance to drop sharply to less than one-third of the nominal inductance when working at full load current. This brings inaccuracy to the digital hysteresis sampling time prediction. As shown in Figures 5, 6.

## 3 Online sampling time prediction algorithm based on inductance-free

From the previous analysis, it can be seen that how to accurately predict the sampling time when the actual inductor changes due to various current becomes a key step in reducing the equivalent sampling rate and improving the effectiveness of digital hysteresis control. Moreover, from the previous analysis, it is known that the predicted sampling rate varies due to a series of factors such as external disturbances in the sampling of controlled current, which inevitably cause changes in the control frequency (Ramchand et al., 2012; Shukla et al., 2011). Thus, it creates a big problem in the thermal loss of the converter, and the design of the LCL filter, especially the design of the inductance. Therefore, how to work with a relatively fixed switching frequency when both sampling time and inductance of the filer inductor change becomes a top priority. According to the literature (Davoodnezhad et al., 2014b), the bandwidth of the digital hysteresis control can be designed to change to ensure a fixed switching frequency when the sampling rate varies (Song et al., 2014; Zeng et al., 2004). Then, the bandwidth of the quasi-fixed frequency digital hysteresis control based on three-level converter with LCL filter can be expressed in Eq. 5 as follows:

$$H = \frac{U_{dc}}{2L \times f_s}|m|\,(1 - 2|m|), m = \frac{E_g(t)}{U_{dc}} \tag{5}$$

Where $U_{dc}$ indicates the total DC voltage value on the DC side of the three-level converter, $f_s$ indicates the desired fixed target switching frequency, $L$ indicates the total AC side filter inductance, and $m = \frac{E_g(t)}{U_{dc}}$ indicates the control modulation index at time $t$.

From the equation, it can be seen that the variation of the bandwidth in the hysteresis control can be inferred from the target expectation fixed switching frequency $f_s$. Moreover, the bandwidth $H$ is changed at a frequency of 2 times the grid frequency (the square function of the control modulation index, which is the same as the AC grid voltage $E_g(t)$). Since the switching frequency of the hysteresis control is typically in tens $kHz$, which is much larger than 2 times the grid frequency, the bandwidth can be approximated as constant within each switching cycle. Moreover, for the inverter, the frequency of the command signal it tracks is also the same as grid, which can also be considered approximately constant during each switching cycle.

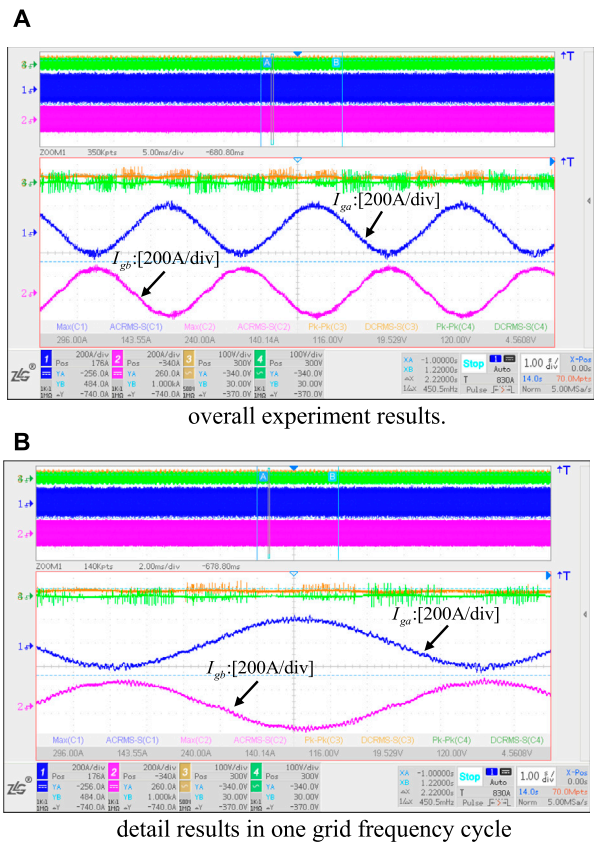


FIGURE 16
Output current waveform of proposed digital hysteresis control. **(A)** overall experiment results. **(B)** detail results in one grid frequency cycle.

So, assume: $H(k-1) \approx H(k)$, $i_{ref}(k-1) \approx i_{ref}(k)$, the upper and lower limits of the bandwidth: $B_{up} = i_{ref} + H$ and $B_{down} = i_{ref} - H$ can also be expressed as:

$$\begin{cases} B_{up}(k-1) \approx B_{up}(k) \\ B_{down}(k-1) \approx B_{down}(k) \end{cases} \tag{6}$$

Thus, when the sampling point is at the intersection of the current and the bandwidth, there is

$$\Delta T_{pre} = \frac{\left|B_{down}(k) - B_{up}(k-1)\right|}{\left|k_{i_{Lr}}\right|} = \frac{\left|B_{up}(k) - B_{down}(k-1)\right|}{\left|k_{i_{Lr}}\right|} = \frac{2H}{\left|k_{i_{Lr}}\right|} \tag{7}$$

By substituting Eqs (6), (7) into the previous Eq. 4, we can get:

$$\Delta T_{pre} = \begin{cases} \dfrac{2 \times \dfrac{U_{dc}}{2L \times f_s}|m|(1-2|m|)}{\left|\dfrac{S_{1a} \times \dfrac{U_{dc}}{2} - E_g}{L}\right|}, E_g(t) > 0 \\ \dfrac{2 \times \dfrac{U_{dc}}{2L \times f_s}|m|(1-2|m|)}{\left|\dfrac{(S_{2a}-1) \times \dfrac{U_{dc}}{2} - E_g}{L}\right|}, E_g(t) < 0 \end{cases} \tag{8}$$

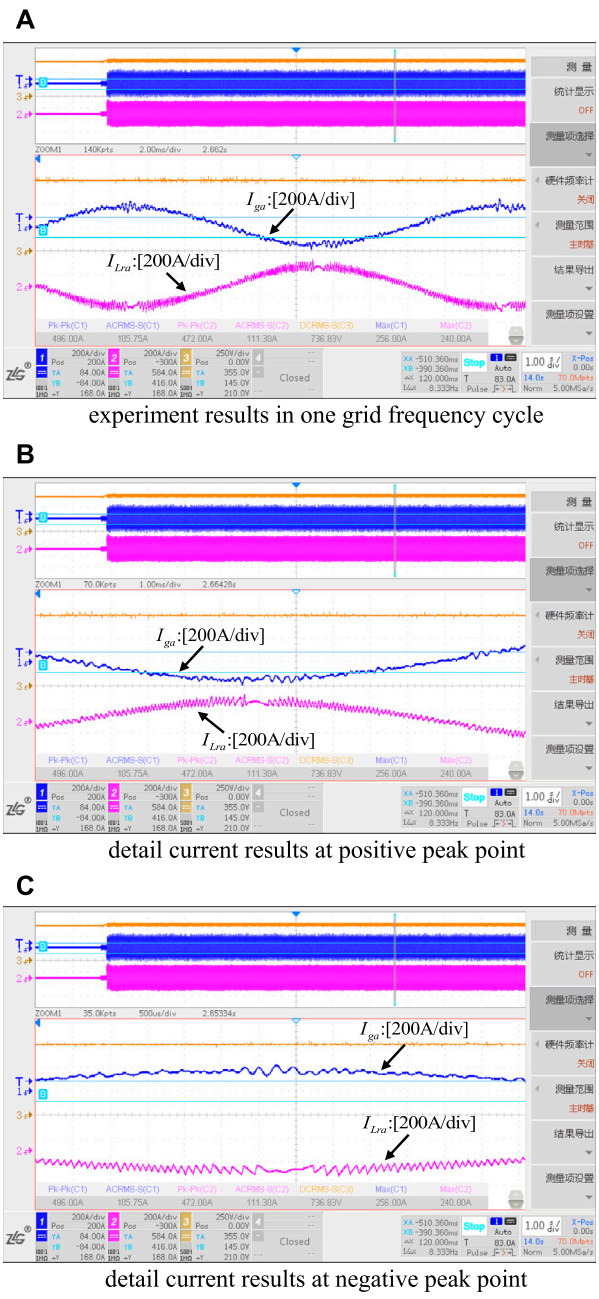


FIGURE 17
Inverter LCL filter current waveform under the proposed inductance-free digital hysteresis sampling time online prediction algorithm. **(A)** experiment results in one grid frequency cycle, **(B)** detail current results at positive peak point, **(C)** detail current results at negative peak point.

After simplification, Eq. 8 can be expressed as:

$$\Delta T_{pre} = 2T_s \frac{|m|(1-2|m|)}{|S_0 - 2m|} \tag{9}$$

Where $S_0 = \begin{cases} S_{1a}, E_g(t) > 0 \\ S_{2a} - 1, E_g(t) < 0 \end{cases}$.

As can be seen from Eq. 9, the predicted sampling time is only related to the desired switching period and the control modulation index function $m$, independent of parameters such as the inductor $L$.

Therefore, the problem of the nonlinearity between the inductance and the output current is solved for the prediction time at steady state.

The previous equation is derived to be effective when the sampling point is just at the intersection of the current and the bandwidth, and after analysis, it is also effective when the current at the sampling moment exceeds the upper or the lower limits of the bandwidth, which can be corrected to:

$$\Delta T_{pre} = 2T_s \frac{|m|(1-2|m|)}{|S_0 - 2m|}, |\Delta i(k)| \geq H \tag{10}$$

where $\Delta i(k)$ indicates the error current.

However, the sampling point is likely to deviate from the bandwidth because of the delay in the sampling process, the inertia of the system, and the actual presence of delay in the PWM control. Thus, at some moments when the current value is less than the hysteresis bandwidth, a correction to the prediction Eq. 10 is required:

From Figure 7, it can be seen that:

when $|\Delta i(k)| < H$, since $|\Delta i(k)| = |i_{ref}(k) - i(k)|$, we can get: $e(k) = H - |\Delta i(k)|$.

then, the correction of sampling period is $t_c = \frac{e(k)}{|k_{i_{L_r}}(k-1)|}$.

Due to $|k_{i_{L_r}}(k-1)| = \frac{|i(k)-i(k-1)|}{\Delta T_{pre}(k-1)}$, according to the above equations:

$$t_c = \frac{H - |\Delta i(k)|}{|i(k) - i(k-1)|} \times \Delta T_{pre}(k-1) \tag{11}$$

Therefore, $t_c$ is the correction formula when the error current is less than the band.

According to Eq. 10 and Eq. 11, the online prediction algorithm based on inductance-free sampling time can be expressed as

$$\Delta T_{pre}(k) = \begin{cases} 2T_s \frac{|m|(1-2|m|)}{|S_0 - 2m|}, |\Delta i(k)| \geq H \\ \frac{H - |\Delta i(k)|}{|i(k) - i(k-1)|} \times \Delta T_{pre}(k-1), |\Delta i(k)| < |H| \end{cases} \tag{12}$$

Where: $\begin{cases} \Delta i(k) = i_{ref}(k) - i(k) \\ S_0 = \begin{cases} S_{1a}, E_g(t) > 0 \\ S_{2a} - 1, E_g(t) < 0 \end{cases} \end{cases}$,

$S_x$ $(x = 1a, 2a)$ indicates the current switch status at the sampling moment, as described in Table 1.

# 4 Simulation analysis

In order to verify the above proposed control method, a simulation comparison analysis was conducted with a LCL type filter based on three-level neural-point-clamped inverter as an example, and the simulation parameters are listed in Table 2.

## 4.1 Simulation results of conventional three-level digital hysteresis control

The simulation results in Figure 8 show the three-phase grid voltage, three-phase inverter-side inductor current, three-level DC-side upper and lower bus capacitor voltage, and overall DC voltage ripple from top to bottom. It is evident that the traditional hysteresis control algorithm has a sudden change in inductor current at the zero-crossing point of the grid voltage, which causes the output waveform to change significantly, the total current harmonic distortion to increase, the hysteresis control error to exceed the bandwidth, and the control effect to be poor.

From left to right in Figure 9, the results of the three-phase grid-side inductor current, the three-phase inverter-side inductor current, and the AC-side filter capacitors are shown in that order. As can be seen from Figure 9, due to the limitation of sampling rate and control frequency, the error current exists in a large range near the command current than the bandwidth, and the overall digital hysteresis control is less effective.

## 4.2 The proposed digital hysteresis control based on online prediction simulation results

In Figure 10, from top to bottom, the grid voltage, the inverter output current, the upper and lower bus capacitor voltages on the DC side of the three-level inverter and the total DC voltage simulation results are shown. It can be seen from the simulation results that the output inverter current is better sinusoidal, the control effect is significantly improved, there is no obvious change in output current waveform at the zero-crossing point of the grid, the error of the hysteresis current control is reduced and limited within the hysteresis band.

From left to right in Figure 11, the results of the three-phase grid-side inductor current, the three-phase inverter-side inductor current, and the AC-side filter capacitors are shown in that order. As can be seen from Figure 11, the controlled inductor current is better sinusoidal, and the capacitor current is less ripple and there is a better control effect compared with the conventional digital hysteresis control method.

The simulation results in Figure 12 from top to bottom represent the reference current and the controlled current, the hysteresis bandwidth and the error current, the bandwidth and the counter needed to correct the period of sample time. From the simulation results, it can be seen that the controlled current is everywhere almost within the bandwidth and follows the reference current exactly with the proposed digital hysteresis sampling time online prediction algorithm. With the sample time correction algorithm, almost every sample point locates at the intersection of the bandwidth boundary exactly, and the current is controlled by the need sinusoidal reference.

# 5 Experimental verification

In order to further verify the theoretical feasibility of the proposed method and the accuracy of the simulation analysis, an experimental verification was conducted. The selected experimental equipment is a 100 kW type I three-level APF. The experimental parameters are shown in Table 3.

The instrumentations used in the experimental setup in Figure 13 are list as follows: the grid-tie inverter is a 100 kW Type I three-level NPC inverter. The inductors are custom-made magnetic core inductors with 1.5 mH at empty load. The controller is used with a DSP 28335 control board with maximum 16 ADC channels and 12 PWM channels. The Oscilloscope is a ZLG

3024PLUS 4 channel scope with 300 MHz bandwidth. And the grid is connected through an isolated transformer with 500 kV A.

### 5.1 Experimental results of conventional digital hysteresis control

The waveform in blue color in Figure 14 is the output inductor current and the red color is the inverter output PWM pulse voltage.

It is evident from the experimental results in Figure 14 that the conventional digital hysteresis control produces a poor output current waveform, with a noticeable current change at the grid zero-crossing point. As a result, there is little control effect and significant current distortion.

The switching process of the experimental waveform results in Figure 15 demonstrate how the sampled inductor current causes the traditional hysteresis control to be inaccurate. This results in frequent switching frequency adjustments and makes it challenging to adjust the output current within the hysteresis control bandwidth, both of which have an impact on the quality of the inverter's final output current.

### 5.2 Experimental results of proposed digital hysteresis control

The above Figure 16 shows the results of the grid-side output waveform obtained by the proposed digital hysteresis control method without inductance using online time prediction. The blue one is the phase A grid-side current and the red one is the phase B grid-side current (the direction of the current transformer is reversed in the experiment). It can be seen that with this control method, the harmonic of the output current is obvious reduced, the distortion of the current is greatly reduced, and the quality of the output current is significantly controlled.

The experimental findings of the inverter-side current switching procedure are displayed in Figure 17. In the experiment, the direction of the current transformer (shown in red) was reversed. The figure shows that there are no shocks in the current at the grid zero-crossing point, the overall inductor current is sinusoidal, and the inverter-side inductor current varies within the hysteresis bandwidth. The total power quality of the output current is efficiently managed and enhanced.

## 6 Conclusion

In this paper, a digital hysteresis control method for three-level inverter based on online prediction of sampling time without inductance is proposed. Through the sample time prediction and correction, the dependence on high sampling rate in traditional hysteresis control is reduced, while the accuracy is improved by keeping the error within the hysteresis band all the time. Furthermore, the impact of inductor parameter changing with different current is eliminated by cancelling the use of inductance during the control process. The effectiveness and robustness of the proposed control method are not only carried out by theoretical analysis and mathematical derivation, but also validated by simulation and experiment.

## Data availability statement

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

## Author contributions

CS: Writing–original draft, Writing–review and editing. LD: Writing–review and editing. SS: Funding acquisition, Writing–review and editing. YX: Writing–review and editing. ZQ: Writing–review and editing. CP: Writing–review and editing.

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## Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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