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Compensation characterization of the UPQC system under an improved nonlinear controller based on the MSTOGI-PLL device

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To solve the delay problem of a unified power quality conditioner (UPQC) system during the separation of the fundamental positive-order components and to better filter out the DC and harmonic components to realize accurate phase locking, a mixed second- and third-order generalized integrator phase-locked loop (MSTOGI-PLL) has been designed to replace the traditional synchronous reference frame phase-locked loop (SRF-PLL). Under the premise of adopting the new phase-locking device of MSTOGI-PLL, the active disturbance rejection control (ADRC) controller or the super-twisting algorithm (STA) sliding mode controller is used in the DC voltage control module instead of the traditional PI controller, and the suitability of the two nonlinear controllers with the MSTOGI-PLL device is investigated. First, the new MSTOGI-PLL device is designed, and the new phase-locking method is applied to make the UPQC realize accurate phase locking under the non-ideal situation of the grid voltage containing unbalance, DC component, harmonics, and so on. Based on the above foundation, the ADRC or STA controller is independently adopted to replace the PI controller to construct the UPQC system with the ADRC + MSTOGI phase-locking device and the second-order STA + MSTOGI phase-locking device. Finally, a simulation comparison is carried out in a Simulink simulation platform regarding the UPQC system under different phase-locking devices, and the simulation results demonstrate that MSTOGI-PLL can successfully filter out the DC component and resolve the phase-locking process delay issue. Additionally, the UPQC system with ADRC + MSTOGI-PLL exhibits superior immunity and response speed to the PI controller and the second-order STA controller.

KEYWORDS

mixed second- and third-order generalized integrator, active disturbance rejection control, super-twisting algorithm, unified power quality conditioner, control accuracy, response speed

1 Introduction

With the wide application of nonlinear power electronic devices, harmonics, unbalance, frequency fluctuations, and other problems are becoming more and more serious, and these power quality problems (Lin, 2014) will affect the normal operation of Chinese communications and financial, medical, and other systems. To address these issues, power quality regulation devices, such as static var compensator (SVC) (Tang et al., 2024), dynamic voltage restorer (DVR) (Gao et al., 2023), and active

power filter (APF) (Zhang et al., 2017), have emerged, which can only solve a single power quality problem. Based on the APF, Japanese scholars proposed the concept of a unified power quality conditioner (UPQC) (Fujita and Akagi, 1996), which combines the functions of DVR and APF and can compensate for multiple power quality problems simultaneously (Wei et al., 2019; Han et al., 2022; Elik and Ahmed, 2023; Lakhdar et al., 2023). How to control the UPQC to better compensate for power quality is currently a significant area of research among scholars.

Phase-locked loops are typically employed in the large-scale development of new energy production to phase lock the phase and frequency of the fundamental wave components of the grid to ensure synchronization with the grid side and an efficient and high-quality grid connection of inverters. When compensating for voltage and power flow in the series–parallel side of the UPQC, it is necessary to obtain accurate phase information on the grid side, and whether the phase-locking device can output accurate phase-locking results will directly affect the compensation effect of the UPQC. Currently, in UPQC systems, a low-pass filter (LPF) is usually used to eliminate the interference of the AC component in the dq coordinate system, but the use of an LPF with a lower cutoff frequency introduces a serious detection delay problem (Lv et al., 2012). For this purpose, a second-order generalized integrator (SOGI) can be used to solve the delay problem (Nasrollahi et al., 2022; Setiawan et al., 2023), but this phase-locking device is very sensitive to the frequency variation of the input signal, and the results will vary directly with the frequency of the input signal. The standard SOGI was reconfigured, and a better type I SOGI was created by (Li et al., 2024); however, the device is subject to the DC component and, hence, an amount of error. The drawbacks of a type I SOGI are addressed by Shi et al. (2022) by creating an enhanced type II SOGI, which is vulnerable to interference from the high-frequency component, by creating a negative feedback channel for the DC component. A synchronous reference frame phase-locked loop (SRF-PLL) can lock the phase quickly and accurately under an ideal voltage environment, but the SRF-PLL encounters inaccurate phase-locking in the presence of imbalances such as distortions and harmonics in the power grid (Kumar et al., 2022; Pan et al., 2023). To overcome the above defects, experts proposed a decoupled double synchronous reference frame PLL (DDSRF-PLL) (Achlerkar and Panigrahi, 2022; Su et al., 2022), and the low bandwidth filter in this phase-locked loop still causes some delay to the system. For this reason, this study proposes the use of a new mixed second- and third-order generalized integrator phase-locked loop (MSTOGI-PLL) filtering device, which effectively filters out the influence of the DC component in phase locking to optimize the control effect and accuracy of the system.

At present, a variety of controllers can be used to control the UPQC, and different controllers have different performances, which will directly affect the compensation effect of the UPQC. A proportional–integral–derivative (PID) controller is one of the most widely used and technically mature control methods (Liu and Wang, 2023; Zhou et al., 2023), but it is not suitable for controlling AC quantities because it generates steady-state errors in the control process and is prone to introducing noise quantities. Hysteresis loop control has a fast dynamic response, but it tends to cause the problem of unfixed switching frequency, which increases the design difficulty of the filtering link (Cheng et al., 2015; Patjoshi and Mahapatra, 2016; Patnaik and Panda, 2016; Ji et al., 2022; Li et al., 2022; Ai et al., 2023; Wang et al., 2023; Wei et al., 2023). Repetitive control, as a control method based on the principle of internal mode, can effectively eliminate the error caused by periodic disturbances; however, its dynamic response speed is not fast enough, and it is only suitable for occasions that do not require a high dynamic response speed of the system (Niroomand and Karshenas, 2017; Lan et al., 2022). Fuzzy control applied to the UPQC does not require an accurate mathematical model and is insensitive to internally caused disturbances and, thus, has good robustness, but it has the disadvantage of large errors in the regulation process, which makes it unsuitable for stand-alone use (Wu, 2022; Ye et al., 2022). The H∞ control UPQC has a small steady-state error, good robust performance, and is not susceptible to external interference, but the computational process is more complicated, and the response speed is slow (Li et al., 2015; Miquelez-Madariaga et al., 2022; Nezhad et al., 2022; Wang and Wang, 2022). Neural network control (NNC) overcomes the shortcomings of PI controllers that are susceptible to changes in external parameters and lead to a decrease in control performance, with strong learning ability, but the implementation is much more complex than that of the PI controller, and the dynamic response is slower (Patjoshi and Mahapatra, 2017; Liu et al., 2019). Sliding mode control applied to UPQC systems can cause a jitter vibration phenomenon, which affects the control effect, and also increases the switching loss and electromagnetic interference (Li, 2022). Higher-order sliding mode control is a new sliding mode control method that can retain the strong robustness of traditional sliding mode while effectively suppressing jitter vibration. Active disturbance rejection control (ADRC) was first proposed by Prof. Kyung-Ching Han in 1998. ADRC can consider all system uncertainties as unknown disturbances of the system, evaluate them by using an expanded state observer (ESO), and compensate for them by using nonlinear state error feedback (NLSEF) (Han, 1998). In this study, a UPQC will use an ADRC controller and second-order super-twisting algorithm (STA) controller instead of a PI controller to enhance the immunity and compensation of the system.

A novel MSTOGI-PLL device is developed to address the delay issue that results from the separation process of the positive-order components of the fundamental waveform in the UPQC control system. This device is built on an improved hybrid second- and third-order generalized integrator. Meanwhile, after replacing the SRF-PLL with a new MSTOGI-PLL device, the ADRC controller or second-order STA controller is used to replace the traditional PI controller in the shunt side of the UPQC to explore what kind of controller works with the MSTOGI-PLL in the UPQC system, which has better immunity and a compensation effect. The enhanced model is built in Simulink to confirm that the ADRC + MSTOGI-PLL device in the UPQC system is superior in terms of immunity, control accuracy, and reaction time.

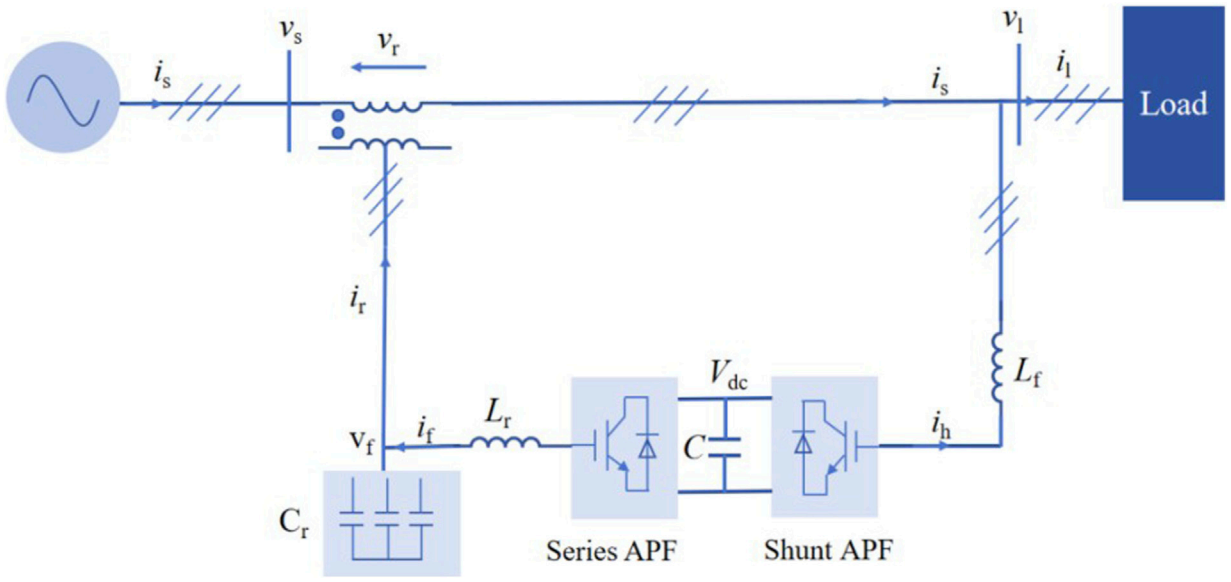

FIGURE 1
Unified power quality conditioner (UPQC) topological structure diagram of a three-phase, three-wire power system.

2 System structure

2.1 Topology of the UPQC in three-phase, three-wire power systems

A UPQC has a range of topologies, often classified as a single-phase or three-phase, three-wire or three-phase, four-wire system, based on the most widely used structure. It can also compensate for both current and voltage levels. Among them, a single-phase UPQC system is mainly used to compensate for single-phase systems (Lu et al., 2015; Xu et al., 2016; Phan and Lee, 2018; Genu et al., 2020; Meng et al., 2021; Liu et al., 2022), a three-phase, three-wire system is mainly considered for current imbalance, and a three-phase, four-wire system compensates for the neutral current. The UPQC system used in this study is a three-phase, three-wire power system, with the structure shown in Figure 1. On the left side, an APF is connected in series through a transformer with a ratio of 1, which is mainly used to compensate for the voltage and is equivalent to a voltage source, and on the right side, an APF is connected in parallel, which is mainly used to compensate for the current and is equivalent to a current source. The grid-side current is denoted as i_s, and the grid-side voltage is v_s. The load-side voltage is denoted as v_l, and the load-side current is i_l. i_f is the current flowing on the inductor L_r on the series APF side, and i_r is the current on the series transformer side. v_f is the three-phase output compensated voltage on the series APF side. i_h is the output compensated current on the shunt APF side, and v_r is the three-phase voltage on the series transformer side.

2.2 MSTOGI-PLL design

The UPQC control system compensates for voltage and current simultaneously, controlling the grid voltage as a stable fundamental positive-sequence component and the load current as a fundamental positive-sequence active component. When the grid is distorted, unbalanced, or has load side with unbalanced or nonlinear loads, the grid voltage, load voltage, and power flow will produce negative-sequence or harmonic components, and the generation of these components will bring errors to the compensation phase-locking detection link, which will affect the compensation accuracy and control effect of the UPQC. In a traditional UPQC control system, the SRF-PLL device is used, and the specific structure is shown in Figure 2.

Figure 2A shows that the grid-side voltage v_{sabc} is input into the coordinate converter to output the quantity $v_{s\alpha}$, $v_{s\beta}$, and $v_{s\alpha}$, and $v_{s\beta}$ is input into the SRF-PLL device to output the phase angle $\sin(\omega t)$ and $\cos(\omega t)$, which are in the same phase with the input voltage of the grid side. The specific coordinate conversion formula is shown in Eq. 1:

$$\begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \\ v_{s0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix}. \quad (1)$$

Figure 2B shows the internal structure of the SRF-PLL. w_c in Figure 2B is the cutoff frequency, where the magnitude of the cutoff frequency will be directly related to the filtering effect of the DC component in the network side; a smaller cutoff frequency can effectively extract the DC component, but a too small cutoff frequency will cause a delay in the detection process. Figure 2B shows that to obtain the synchronization phase angles $\sin(\omega t)$ and $\cos(\omega t)$, as shown in Eqs 2, 3 below, where $v_{s\alpha(\mathrm{fund})}$ and $v_{s\beta(\mathrm{fund})}$ in Eq. 2 are the values of the fundamental waveform positive-sequence components of the output in the αβ coordinate system.

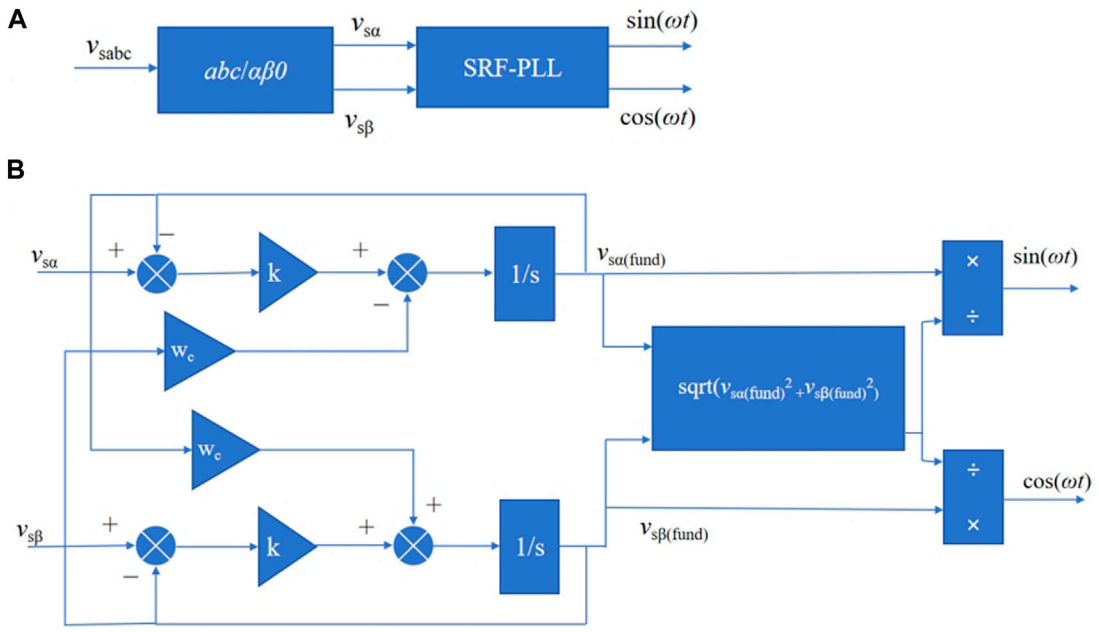

FIGURE 2
Synchronous reference frame phase-locked loop (SRF-PLL) specific structure diagram. **(A)** SRF-PLL input/output diagram. **(B)** Internal structure of SRF-PLL.

$$\sin(\omega t) = \frac{v_{s\alpha(fund)}}{\sqrt{\left(v_{s\alpha(fund)}^2 + v_{s\beta(fund)}^2\right)}}, \tag{2}$$

$$\cos(\omega t) = \frac{v_{s\beta(fund)}}{\sqrt{v_{s\alpha(fund)}^2 + v_{s\beta(fund)}^2}}. \tag{3}$$

The SRF-PLL can quickly and accurately lock the phase and frequency of the grid-side voltage under an ideal voltage, but the phase-locking accuracy of the SRF-PLL will be inaccurate under grid voltage distortion and harmonic imbalance, which affects the compensation performance of the UPQC. In order to provide the filter good output characteristics in both low- and high-frequency bands and to lock the phase accurately under the presence of grid distortion and harmonic imbalance, this paper adopts a new phase-locking device based on a second- and third-order generalized integrator, MSTOGI-PLL, which is capable of separating the DC and negative-sequence components efficiently.

When the power system experiences unbalanced disturbance, the symmetric component method is often used to decompose the voltage and power flow into positive-sequence, negative-sequence, and zero-sequence quantities. The Clark transform makes the zero-order component zero, and the detection of the fundamental waveform component is accomplished by separating the positive-order component. The symmetric component method used in the detection process is shown in Eq. 4. In Eq. 4, v_{sa}^+, v_{sb}^+, and v_{sc}^+ are the positive-sequence component values of the three-phase voltage on the grid side; v_{sa}, v_{sb}, and v_{sc} are the three-phase voltage values on the grid side; and a is the phase operator.

$$\begin{bmatrix} v_{sa+} \\ v_{sb+} \\ v_{sc+} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix}\begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix}. \tag{4}$$

The Park transformation is performed to transform the positive-sequence three-phase components into the $\alpha\beta$ coordinate system, as shown in Eq. 5, where $v_{s\alpha}^+$ and $v_{s\beta}^+$ are the positive-sequence components of the grid-side voltage in the $\alpha\beta$ coordinate system.

$$\begin{bmatrix} v_{s\alpha+} \\ v_{s\beta+} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_{sa+} \\ v_{sb+} \\ v_{sc+} \end{bmatrix}. \tag{5}$$

Bringing Eq. 4 into Eq. 5 and performing the Clark inverse transformation yield Eq. 6, where b in Eq. 6 is the time-domain phase-shift operator.

$$\begin{bmatrix} v_{s\alpha+} \\ v_{s\beta+} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 & -b \\ b & 1 \end{bmatrix}\begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix}. \tag{6}$$

Equation 6 is the formula involved in the fundamental positive-sequence calculator (FPSC) module, where the time-domain phase-shifting operator b serves to make the positive-sequence signal of the grid-side voltage into two mutually orthogonal quantities. The specific structure of the MSTOGI is shown in Figure 3A, where the part inside the dashed line box is the module for eliminating the DC component, which is eliminated by subtracting the generated v_3, and v_m and bv_m are two mutually orthogonal voltage outputs. ω_0 is the resonant frequency of the MSTOGI, and the frequency of the input signal v is ω_s. When $\omega_0 = \omega_s$, there is no DC in v_1, and the AC component is the same as the input signal v. v_2 contains DC and AC components, where the

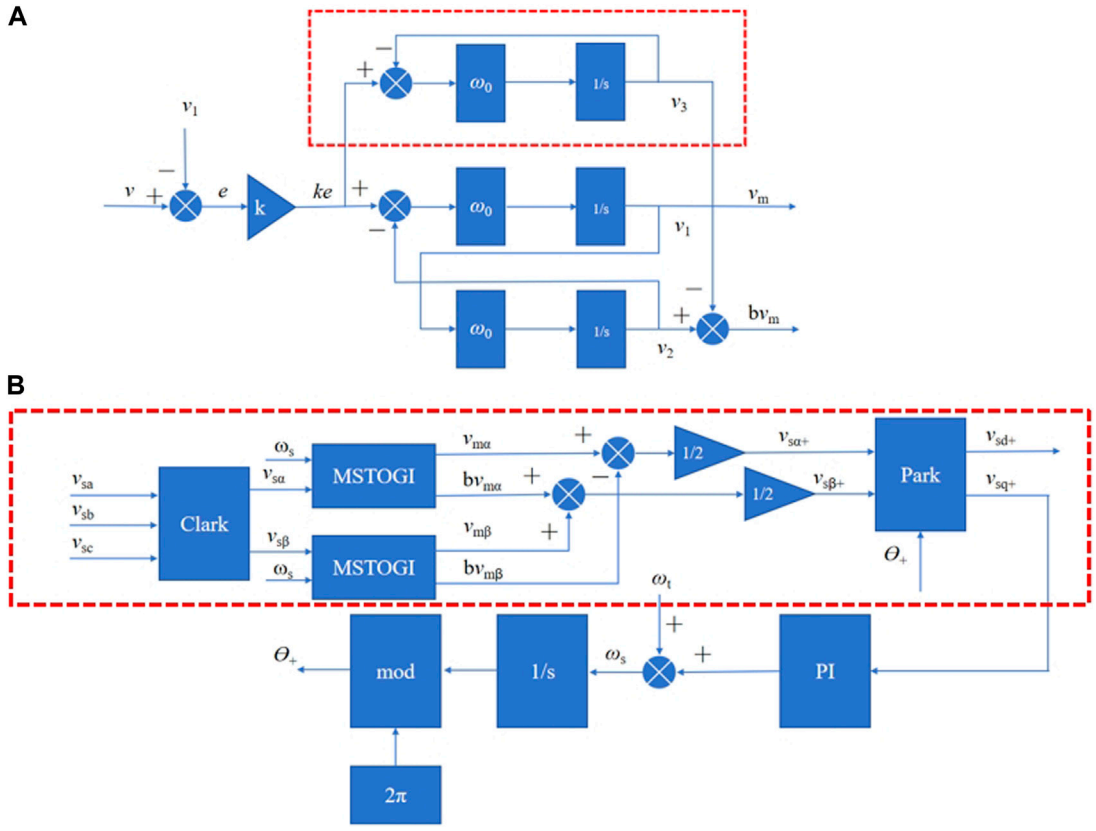

FIGURE 3
Mixed second- and third-order generalized integrator phase-locked loop (MSTOGI-PLL) specific structure diagram. **(A)** Specific structure diagram of MSTOGI. **(B)** MSTOGI-PLL specific structure diagram.

phase of the AC component lags the input signal v by an angle of 90°, and the amplitude and frequency of the AC component are the same as the v_1 quantity. v_3 contains only DC components of the same magnitude as those in v_2, and the elimination of DC components is specifically shown in Eq. 7.

$$\begin{cases} v_m = v_1 \\ bv_m = v_2 - v_3 \end{cases}. \tag{7}$$

The flowchart of the adopted MSTOGI-PLL device is shown in Figure 3B, where ωt is a variable value, and the introduction of this value is mainly used to speed up the detection of the phase-locked loop; if this quantity is not introduced, the detection of the phase-locked loop can only be accelerated by adjusting the PI controller, but this process will produce a large overshooting amount, which increases the instability of the control system. In this study, this value ωt is set to 100π after empirical testing. Θ_+ is the phase angle of the MSTOGI-PLL output. The red dotted box shows the specific structure of the MSTOGI-PLL.

Combined with Figure 3B, the values of the fundamental waveform positive-sequence components $v_{s\alpha}^+$ and $v_{s\beta}^+$ extracted for the network side are shown in Eq. 8.

$$\begin{cases} v_{s\alpha+} = \frac{1}{2}\left(v_{m\alpha} - bv_{m\beta}\right) \\ v_{s\beta+} = \frac{1}{2}\left(bv_{m\alpha} + v_{m\beta}\right) \end{cases}. \tag{8}$$

2.3 Design of the UPQC system with ADRC or second-order STA control on the shunt APF side

2.3.1 UPQC system design with ADRC on the shunt APF side

In the DC voltage control link of the UPQC, the PI controller is often used (as shown in Figure 4A), which is simple in construction and has a fast and smooth control process. At the same time, the PI controller also has some shortcomings: in the initial moment of control, it can easily cause overshooting, and for closed-loop control, it can easily become sluggish, resulting in integral saturation and oscillations. i_{cd} under the PI controller will be positively fed back to the current compensation module, and finally, the shunt module needs to be given by the amount of current compensation $i_{l\alpha,h}^*$, $i_{l\beta,h}^*$. Inaccuracies in the control process will make the output current compensation inaccurate and, thus, affect the compensation effect of the UPQC; therefore, in this study, the PI controller of the orange module is replaced with the ADRC nonlinear controller to enhance the accuracy of the system control and then explore the compensation effect of the UPQC system based on the new MSTOGI-PLL + ADRC.

The block diagram of the ADRC is shown in Figure 4B and consists of a tracking differentiator (TD), nonlinear state error feedback (NLSEF), and extended state observer (ESO). The variable $V_{dc(ref)}$ given in Figure 4B is the reference value of the

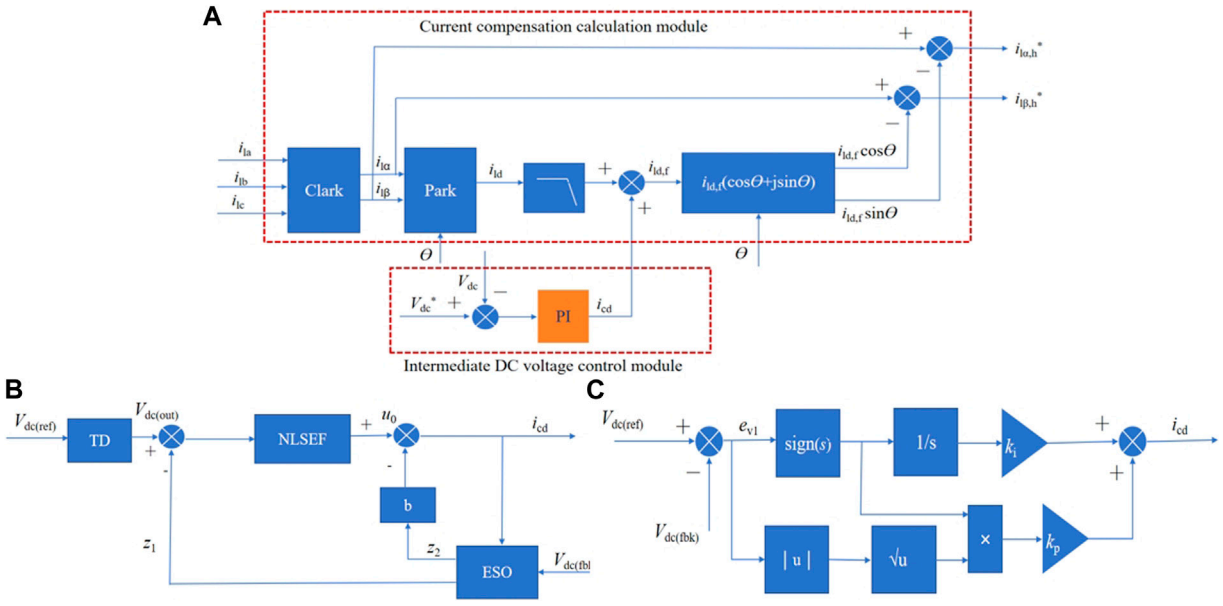

FIGURE 4
Shunt active power filter (APF)-side control block diagram. **(A)** Current compensation module. **(B)** Active Disturbance Rejection Controller schematic diagram. **(C)** STA controller specific structure.

DC module capacitor voltage, $V_{dc(fbk)}$ is the feedback value of the DC module capacitor voltage, and $V_{dc(out)}$ is the tracking output value of the intermediate DC voltage.

The intermediate DC voltage module, if controlled by PI, is shown in Eqs 9, 10. e_{v1} is the difference between the reference voltage and the actual value at the intermediate DC terminal. i_{cd} is the output current of the intermediate DC module, and $K_{p(DC)}$ and $K_{i(DC)}$ are the proportionality coefficients and integral coefficients of the PI controller, respectively.

$$e_{v1} = V_{dc(ref)} - V_{dc(fbk)}, \tag{9}$$

$$i_{cd} = K_{p(DC)} e_{v1} + K_{i(DC)} \int_0^t e_{v1} dt. \tag{10}$$

2.3.1.1 Design of the TD

The main function of the TD is to track and transition the reference value $V_{dc(ref)}$ of the intermediate DC voltage, as shown in Eq. 11, where *fal* is the *fal*(.) function, and the specific expression of the *fal* function is shown in Eq. 12. In Eq. 12, *e* is the amount of error, *a* is the exponential value, δ is the base of the exponential function, and *sign* is the signal function. The *fal* function is central to the ADRC controller, and its mathematical expression is based on the empirical knowledge of control engineering: mathematical fitting of a large error, small gain, small gain, and large error.

$$\begin{cases} e_0 = V_{dc(out)} - V_{dc(ref)} \\ V_{dc(out)} = \beta_0 fal(e_0, \alpha_0, \delta_0) \end{cases}, \tag{11}$$

$$fal(e, \alpha, \delta) = \begin{cases} |e|^{\alpha} sign(e), |e| > \delta \\ e/\delta^{1-\alpha}, |e| \le \delta \end{cases}. \tag{12}$$

In Eq. 12, δ is the filtering factor of the *fal* function, and an increase in δ can make the filtering effect better, but it also increases the tracking delay. *a* is usually taken between 0 and 1, and the smaller *a* is, the faster the tracking is, but the filtering effect will become worse. Therefore, when the parameters are selected, the values of δ and *a* need to be considered together. When $|e|>\delta$, the *fal* function acts as a nonlinear feedback, which can make the system quickly approximate the input signal. When $|e|\le\delta$, the expression of the *fal* function behaves as a low-pass filter.

2.3.1.2 Design of the ESO

In the ADRC controller, the ESO is mainly used to make observations on the uncertainty and disturbance of the system, as shown in Eq. 13. In Eq. 13, $u(t)$ is the control quantity, and in this study, $u(t)$ is the ADRC output value i_{cd}.

$$\begin{cases} e_2 = z_1 - V_{dc(fbk)} \\ z_1 = z_2 - \beta_2 fal(e_2, \alpha_2, \delta_2) + bu(t) \\ z_2 = -\beta_3 fal(e_2, \alpha_2, \delta_2) \end{cases}. \tag{13}$$

In Eq. 13, β_2 and β_3 are two parameters in ADRC that need to be set empirically. In the case of relatively large values of β_2 and β_3, it is favorable to improve the ESO tracking speed. However, too large values will cause the system to oscillate and overshoot. Usually, β_3 is 1~2 orders of magnitude larger than β_2.

2.3.1.3 Design of the NLSEF

The NLSEF mainly makes a difference for the reference signal output from the TD, the differential signal, and the state signal output from the ESO, and then, it combines these signals nonlinearly to obtain the error feedback control quantity. Specifically, it is shown in Eq. 14, where z_1 is the observed value of V_{dc}.

$$\begin{cases} e_1 = V_{dc(out)} - z_1 \\ u_0 = \beta_1 fal(e_1, \alpha_1, \delta_1) \end{cases}. \tag{14}$$

The disturbance compensation process of the final control output i_{cd} is shown in Eq. 15

$$i_{cd} = u_0 - bz_2. \tag{15}$$

2.3.2 Design of the UPQC system with the second-order STA on the shunt APF side

Sliding mode control is a kind of discrete nonlinear control, and traditional sliding mode control is prone to a vibration jitter phenomenon. The super-twisting sliding mode control applies the discrete control law to a higher order in the operation process, realizing the continuity of the control quantity in time, and, therefore, can effectively inhibit the generation of jitter vibration. The second-order STA control is denoted as a, which usually consists of two parts: a_1 is the continuous function on the sliding mode surface, and a_2 is the integral of the sliding mode surface in time, as shown in Eqs 16–19.

$$a = a_1 + a_2, \tag{16}$$

$$a_1 = -k_i|s|^{\rho} sign(s), \tag{17}$$

$$a_2 = k_p sign(s), \tag{18}$$

$$\text{sign}((s) = \begin{cases} 1, s > 0 \\ -1, s < 0 \end{cases}. \tag{19}$$

Equations 16, 17, in which k_i, k_p>0, are all positive gain parameters. $Sign(s)$ is the sign function, and ρ is the exponential term coefficient. Sliding mode controller jitter is caused by signal discontinuity, and the integral signal as a continuous signal will not have the problem of the emergence of discrete quantities. Eq. 18, as discontinuous high-frequency switching quantities, no longer has a direct impact on the control law a, but the form of the *sign* function is transformed into the form of a time integral in the STA control law, which results in a continuous control signal, eliminating the jitter phenomenon in the sliding mode control. In terms of the value of the formula, in order to realize the convergence of the system in finite time, ρ in Eq. 8 should satisfy $0 < \rho \leq 0.5$, and the value of ρ in this study is 0.5. The sliding mode variable s is shown in Eq. 20:

$$s = e_{v1} = V_{dc(ref)} - V_{dc(fbk).} \tag{20}$$

The final second-order STA control law is obtained as shown in Eq. 21. The specific form of the second-order STA controller is shown in Figure 4C.

$$I_{DC} = u = k_i|s|^{1/2} sign(s) + \int k_p sign(s)dt. \tag{21}$$

3 Simulation analysis

In this study, a new MSTOGI-PLL device is used to replace the conventional SRF-PLL device, and based on the use of the new phase-locking device, the compensation characteristics of the UPQC are investigated when two different nonlinear controllers are used in the DC voltage control module. It is mainly divided into three groups for comparison.

Group I: The UPQC system of MSTOGI-PLL + ADRC is compared to that of SRF-PLL + ADRC, focusing on which phase-locking device system is used for better compensation speed and effectiveness in the case of a common ADRC controller.

Group II: The UPQC system of MSTOGI-PLL + STA is compared to that of SRF-PLL + STA, which mainly investigates which phase-locking device system is used for better compensation speed and effect in the case of a common use of second-order STA controllers.

Group III: Comparative analysis between MSTOGI + PI in the UPQC system, MSTOGI-PLL + ADRC in the UPQC system, and MSTOGI-PLL + STA in the UPQC system mainly aims to study which controller adapted to the MSTOGI-PLL device can make the compensation effect of the system better in the case of all using the MSTOGI-PLL device.

TABLE 1 Relevant parameters of the system in the simulation.

Parameter	Value
V_s	380 V/50 Hz
L_r	3 mH
C	6,600 μF
L_f	3 mH
Load (R–L)	100 Ω–100 mH
C_r	3,300 μF
Transformer ratio	1:1

The MATLAB/Simulink module was used to compare and analyze the simulation of the research group, and the specific parameters used for the three-phase, three-wire UPQC system in the simulation are shown in Table 1.

3.1 Group I: UPQC system of MSTOGI-PLL + ADRC vs. UPQC system of SRF-PLL + ADRC

The grid-side voltage is 380 V/50 Hz, and the simulation time is 2 s. At the beginning of the simulation, the grid-side voltage is 380 V, and after 0.5 s, the grid-side voltage becomes 1.2 times the initial value, and after 1 s, the grid-side voltage decreases to 0.8 times the initial value, and the grid-side voltage recovers after 1.5 s. In Figure 5, V-Source is the grid-side three-phase voltage v_s, V-Load is the load-side three-phase voltage output v_l, I-Source is the grid-side three-phase current value i_s, and I-Load is the load-side three-phase current output value i_l. Figures 5A, C show the waveforms of the grid-side and load-side voltage and current values of the UPQC system. Figures 5B, D show the partial magnification diagrams of the simulation for the periods 0.4–0.6 s with localized zoomed-in graphs. The ADRC controllers used in the first group all have the same coefficients, $b = 500$, $\beta_0 = 40$, $\beta_1 = 1.6$, $\beta_2 = 2$, and $\beta_3 = 15$.

From the V-Source waveform graph, it can be seen that the variation in the measured voltage v_s at the net side follows the simulation settings. In terms of voltage compensation, the UPQC system with MSTOGI-PLL + ADRC can compensate for the voltage quantities for the disturbances in time, resulting in a stable output v_l at the load side. The UPQC system with SRF-PLL + ADRC produces significantly sharp peaks in the output v_l at the peak and valley points in terms of voltage compensation.

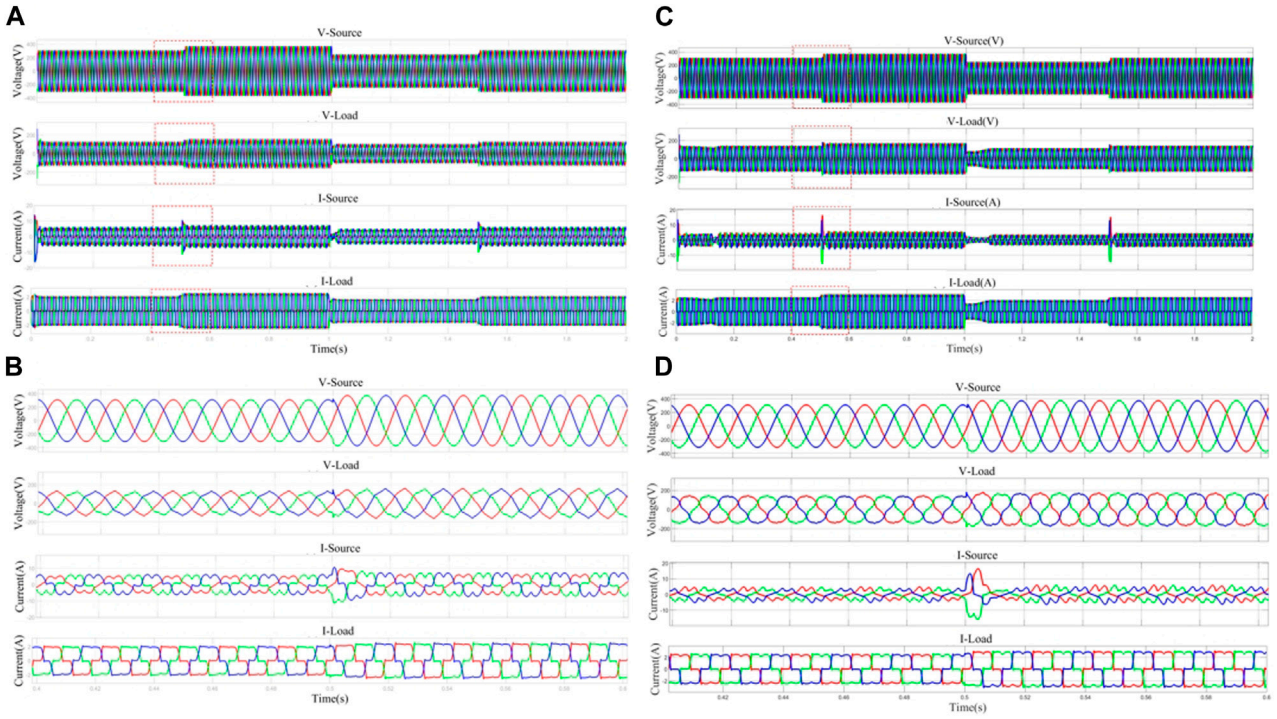

FIGURE 5
Voltage–current output plot of the same active disturbance rejection control (ADRC) controller using different filters. **(A)** Waveforms of network side and load side voltage and current values of UPQC system with MSTOGI-PLL+ADRC. **(B)** Localized amplified waveforms of grid-side and load-side voltage and current values of UPQC system with MSTOGI-PLL+ADRC. **(C)** Waveforms of grid-side and load-side voltage and current values of UPQC system with SRF-PLL+ADRC. **(D)** Localized amplified waveforms of grid-side and load-side voltage and current values of UPQC system with SRF-PLL+ADRC.

In terms of current compensation, the UPQC system with MSTOGI-PLL + ADRC showed distortion in the i_s output value due to the nonlinear load accessed by the load, which no longer maintains a sinusoidal waveform and oscillates at 0.5 s and 1.5 s of the voltage change. However, i_l was effectively compensated, and its output waveform resembled a sine wave and did not produce oscillating values with i_s, indicating that the system was able to effectively compensate for the amount of power flow, making the UPQC system stable. In contrast, the UPQC system with SRF-PLL + ADRC produces a sharp burr oscillation at 0.5 s and 1.5 s after v_s is subjected to grid-side interference with an amplitude of 15 A, and the output i_l waveform is more severely distorted than that of the UPQC system with MSTOGI-PLL + ADRC. It is shown that the UPQC system with MSTOGI-PLL + ADRC has better robustness when disturbances occur in the network-side system, the oscillation value of the network-side current i_s reduced by 50% when a sudden voltage change occurs, and the degree of voltage and current deformation of this system is minimized under the influence of nonlinear loads.

The Bode plots for the two filter inputs $v_{s\alpha}$ and the positive-sequence component of the fundamental waveform $v_{s\alpha+}$ after filtering the output are shown in Figures 6A, B. Figure 6A shows that the MSTOGI-PLL filter is a band-pass filter, which has large amplitude attenuation in both the high- and low-frequency bands, and can effectively filter out the DC component and high harmonics in the input signal. Therefore, the UPQC system with this filter is more stable. Figure 6B shows the SRF-PLL acts as a band-pass filter with a narrower range of bands to be filtered, and the insensitivity of this filter to attenuation in the low- and high-frequency bands indicates that the filter does not filter well for the DC component and the higher harmonic components in the grid.

Figures 6C, D show that, under the same premise of using an ADRC controller, the output $v_{s\alpha+}$ and $v_{s\beta+}$ of the UPQC system of MSTOGI-PLL + ADRC can follow the change in the grid-side voltage quantity v_s in time under the effect of the MSTOGI-PLL filtering device. On the other hand, the positive-sequence component voltage values $v_{s\alpha+}$ and $v_{s\beta+}$ output from the SRF-PLL + ADRC UPQC system in the αβ coordinate system have a large overshoot. At the moment of voltage perturbation, the UPQC system with SRF-PLL takes 0.16 s, 0.2 s, and 0.1 s to respond in time, respectively. It indicates that the MSTOGI-PLL device has a faster response and better robustness performance of the UPQC system, provided that the same controller is used.

3.2 Group II: UPQC system of MSTOGI-PLL + STA vs. UPQC system of SRF-PLL + STA

In the second set of simulation experiments, the v_s voltage perturbation is set as in the first set of experiments. Figures 7A, C show the waveforms of the network-side and load-side voltage and current values of the UPQC system with MSTOGI-PLL + STA and the UPQC system with SRF-PLL + STA. Figures 7B, D show the localized enlargement of the voltage and current values of the network side and load side of the two UPQC systems for

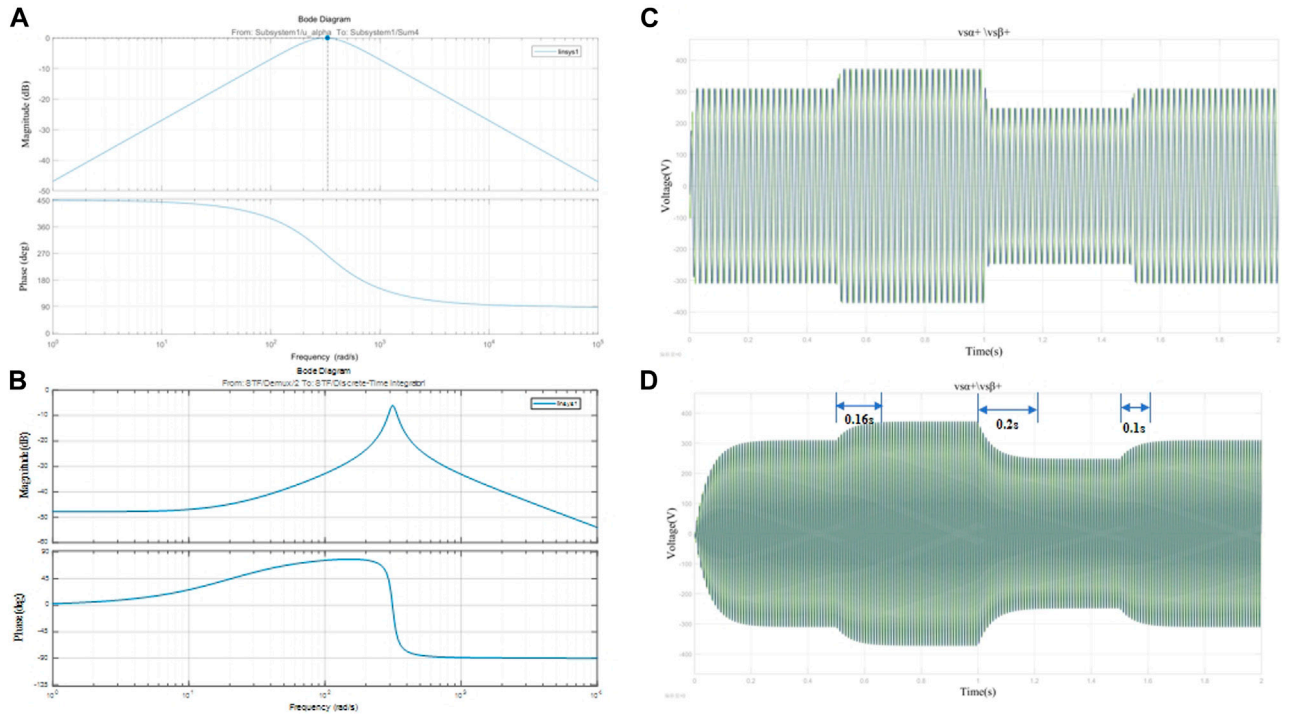

FIGURE 6
Bode plot and fundamental positive-sequence current component using different filtering devices. **(A)** MSTOGI-PLL Bode diagrams. **(C)** Positive-sequence vsβ+,vsβ+ volume response plots of the output of the UPQC system with MSTOGI-PLL+ADRC. **(B)** SRF-PLL Bode diagrams. **(D)** Positive-sequence vsβ+,vsβ+ volume response plots of the output of the UPQC system with SRF-PLL+ADRC.

simulation time 0.8–1.2 s. In the second set of experiments, the STA controller parameters were the same in both UPQC systems with a k_i value of 9 and a k_p value of 25.

The comparison of Figures 7A, C shows that when the STA controller is used and the phase-locking device adopts the MSTOGI-PLL or SRF-PLL, both the compensated voltage v_l and the amount of current i_l at the output of the UPQC system are affected by the amount of perturbation. At 0.5 s and 1.5 s when the perturbation was added, the i_s electric flow of both UPQC systems showed large fluctuations in amplitude, which shows that the STA controller is not ideal in resisting the perturbation. When used with the SRF-PLL device, Figures 7C, D show i_s at 1 s when the value of the v_s voltage decreases from 1.2 times to 0.8 times, followed by the phenomenon of a direct dropout in I-Source, a phenomenon that will bring harm to the power equipment in real life. Figures 7B, D show that both UPQC systems have effectively compensated for the voltage and current. The UPQC system with the SRF-PLL device produces large overshoots at the simulation moments 0, 0.5, 1, and 1.5 s and takes 0.2 s, 0.1 s, 0.2 s, and 0.1 s, respectively, to make the output value stable. It shows that the response speed and accuracy of the MSTOGI-PLL device are better than those of the SRF-PLL device.

When it comes to further separation of the positive-sequence components in the αβ coordinate system, Figures 8A, B show that the output of the base wave positive-sequence components $v_{sα+}$ and $v_{sβ+}$ of the UPQC system with MSTOG-PLL have achieved a fast response in the simulation moments of 0, 0.5, 1, and 1.5 s and the overshoot is small. The UPQC system with the SRF-PLL device produces larger overshoots at the simulation moments 0, 0.5, 1, and 1.5 s to the output. To stabilize fundamental waveform positive-sequence components $v_{sα+}$ and $v_{sβ+}$, more regulation time is needed, which indicates that the response speed and accuracy of the MSTOGI-PLL device are better than those of the SRF-PLL device, and it achieves the purpose of the design at the beginning.

3.3 Group III: Comparative analysis among the MSTOGI-PLL + PI UPQC system, MSTOGI-PLL + ADRC UPQC system, and MSTOGI-PLL + STA UPQC system

In the third set of simulations, the simulation time is 2 s. Extreme disturbance is added in this set of simulations, i.e., a large number of 3rd, 5th, and 7th harmonics are added to the net side throughout the whole process. The net side voltage of the system increases to 1.2 times of the original voltage value at the simulation moment of 0.5 s, and the value of the system voltage recovers at the simulation moment of 1 s. At the simulation moment of 1.2 s, the grid-side voltage value v_s decreases to 0 instantaneously and keeps the voltage 0 for 0.3 s, and the grid-side voltage value recovers at the simulation moment of 1.5 s. The compensation characteristics of the UPQC system using an MSTOGI-PLL device with different controllers are investigated in this extreme environment. Since the simulation environment was changed, some parameters of the controllers in this set of comparisons were readjusted, i.e., K_p = 0.2 and K_i =

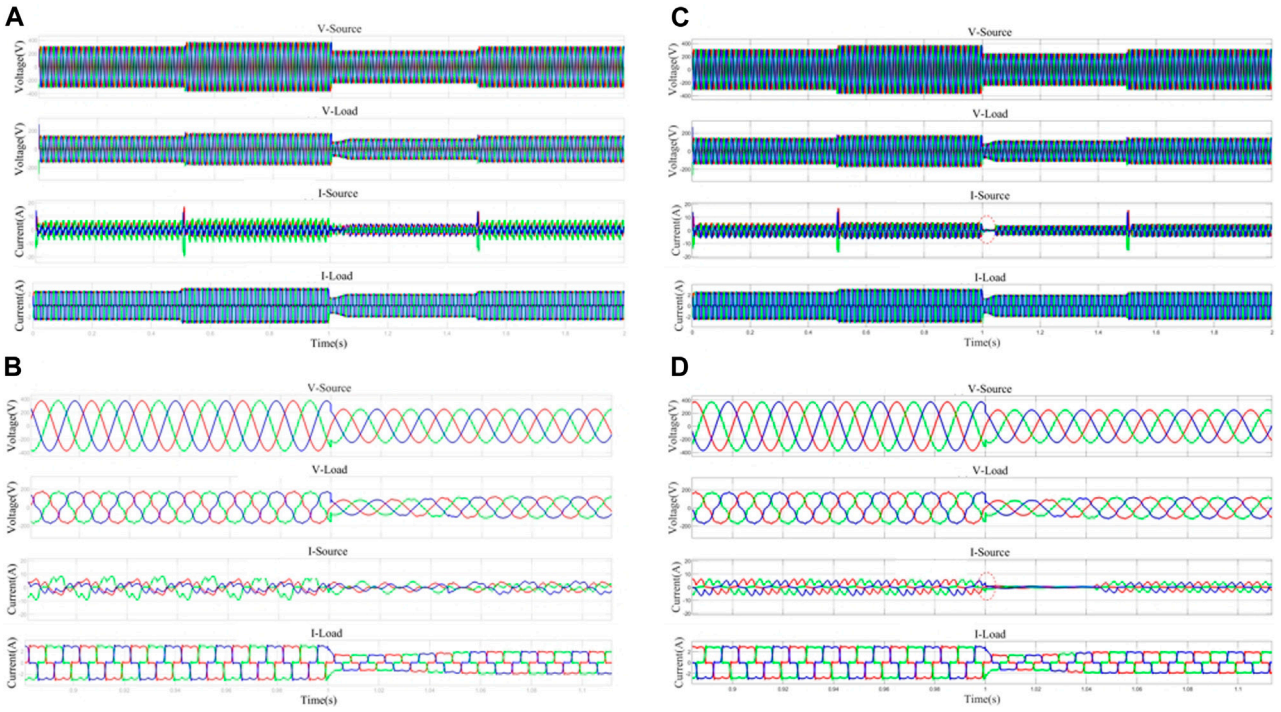

FIGURE 7
Voltage–current output plot of the same super-twisting algorithm (STA) controller using different filters. **(A)** Waveforms of network side and load side voltage and current values of UPQC system with MSTOGI-PLL+STA. **(B)** Localized enlarged view of grid-side and load-side voltage and current values of UPQC system with MSTOGI-PLL+STA. **(C)** Waveforms of network side and load side voltage and current values of UPQC system with SRF-PLL+STA. **(D)** Localized amplified waveforms of grid-side and load-side voltage and current values of UPQC system with SRF-PLL+STA.

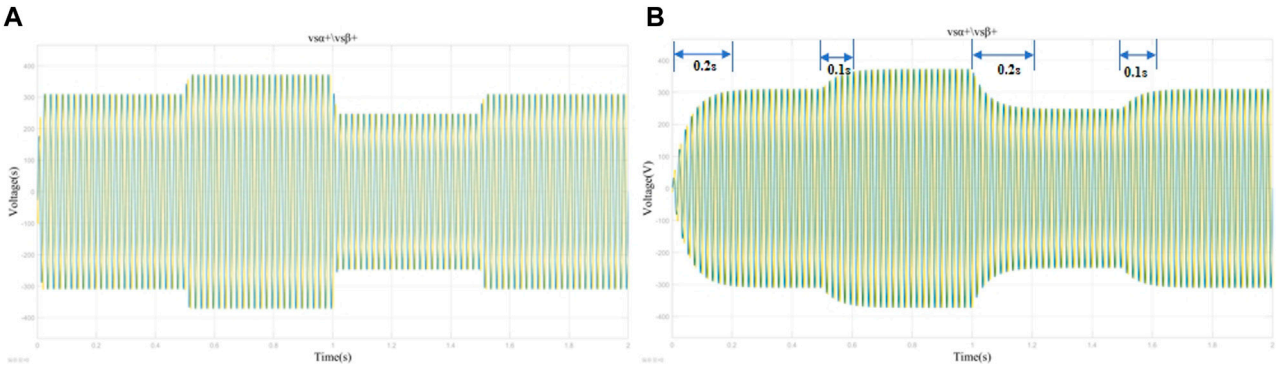

FIGURE 8
Output values of the fundamental positive-sequence components of the different filters using the STA controller. **(A)** Output positive order vsα+,vsβ+ volume response plots of UPQC system with MSTOGI-PLL+STA. **(B)** Output positive order vsα+,vsβ+ volume response plots of UPQC system with SRF-PLL+STA.

0.3 in the PI controller, $k_p = 6$ and $k_i = 30$ in the STA controller, and $b = 690$, $\beta_0 = 30$, $\beta_1 = 1.6$, $\beta_2 = 4$, and $\beta_3 = 40$ in the ADRC controller.

Figures 9A, C, E show the waveforms of the grid-side and load-side voltages of the UPQC system, and Figures 9B, D, F show the localized magnification of the grid-side and load-side voltages at the simulation moment of 1.9–2 s. Figures 9A, C, E show that when the grid voltage dips, the UPQC system with PI as the controller makes v_l gradually decrease to 0 in the whole period of 1.2–1.5 s. The whole process takes approximately 0.3 s, and the system voltage does not instantly decrease to 0, which indicates that the system has a certain degree of immunity to disturbances. v_l of the UPQC system with the STA as the controller did not decrease to 0 throughout the time period of 1.2–1.5 s, indicating that the UPQC system with the STA

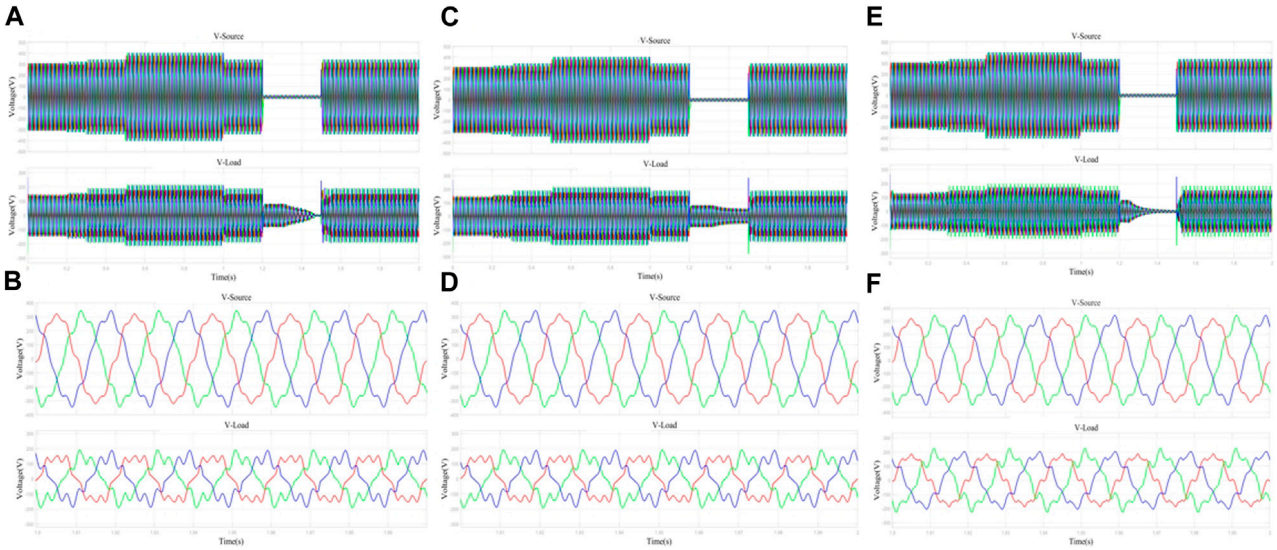

FIGURE 9
Network-side and load-side voltage outputs with different controllers of the same filtering device. **(A)** Network side and load side voltage waveforms of UPQC system with MSTOGI-PLL+PI. **(B)** Localized amplified waveforms of grid-side and load-side voltage of UPQC system with MSTOGI-PLL+PI. **(C)** Network side and load side voltage waveforms of UPQC system with MSTOGI-PLL+STA. **(D)** Localized amplified waveforms of grid-side and load-side voltages of UPQC system with MSTOGI-PLL+STA. **(E)** Network-side and load-side voltage waveforms of UPQC system with MSTOGI-PLL+ADRC. **(F)** Localized amplified waveforms of grid-side and load-side voltages of UPQC system with MSTOGI-PLL+ADRC.

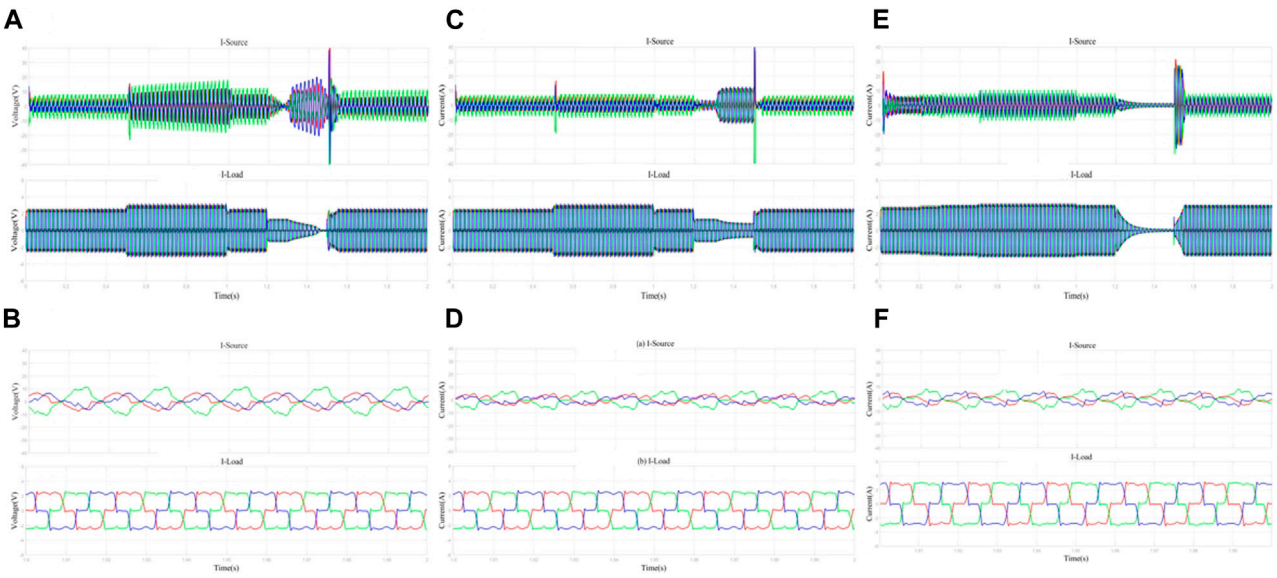

FIGURE 10
Network-side and load-side current outputs with different controllers of the same filtering device. **(A)** UPQC system network side and load side current waveforms for MSTOGI-PLL+PI. **(B)** Localized amplified waveforms of UPQC system grid-side and load-side current for MSTOGI-PLL+PI. **(C)** UPQC system network side and load side current waveforms for MSTOGI-PLL+STA. **(D)** Localized amplified waveforms of UPQC system grid-side and load-side currents for MSTOGI-PLL+STA. **(E)** UPQC system network side and load side current waveforms for MSTOGI-PLL+ADRC. **(F)** Localized amplified waveforms of grid-side and load-side currents of UPQC system with MSTOGI-PLL+ADRC.

as the controller has immunity to disturbances, but there is a delay in the control. In the UPQC system with ADRC as the controller, v_l gradually decreases to 0 in the period of 1.2–1.5 s, and the whole process takes approximately 0.2 s. The system has the ability of anti-interference and has optimal performance in terms of response speed and accuracy. Figures 9B, D, F show that in the time period 1.9–2 s, the system shows significant voltage distortion on the v_s side due to a large number of harmonic disturbances. On the compensation side, the output v_l of both the UPQC systems with PI and STA as controllers showed more severe distortion than the

UPQC system with ADRC as a controller. Its output v_l has a jagged deformation and dips in the peaks and troughs, and the deformation reaches a level of distortion compared to the v_s input. The UPQC system with ADRC as the controller also produces a deformation in the v_l value due to a large number of high harmonics; the deformation is not to the extent of distortion, and the output waveform can still be approximated as a sinusoidal waveform.

Figures 10A, C, E show the UPQC system net-side and load-side current waveforms, and Figures 10B, D, F show the UPQC system net-side and load-side current localized amplified waveforms at 1.9–2.0 s. Figures 10B, D, F show that the output i_l waveforms of all three UPQC systems achieve an approximate sinusoidal waveform in terms of current compensation. Figures 10A, C, E show that when the voltage decreases in the period 1.2–1.5 s, the UPQC system with PI as the controller has a gradual decrease in current i_l during this period and takes nearly 0.3 s to decrease to 0. The UPQC system with the STA as the controller does not experience a decrease in the current i_l to 0 during this period, and there is a delay in the control. The UPQC system with ADRC as the controller takes 0.2 s for the i_l value to decrease to 0 during this period, and when the voltage value recovers at the moment of 1.5 s, the UPQC system with ADRC as the controller i_l generates the least oscillation. During the whole control process from 0 to 1.2 s, the UPQC system with ADRC as the controller produces the smallest ups and downs in i_l at the moments of 0.5 s and 1 s, indicating that the UPQC control system with MSTOGI-PLL + ADRC has the optimal immunity and response speed. The UPQC system with ADRC as the controller also produces minimum oscillations. This set of simulations shows that the UPQC control system with MSTOGI-PLL + ADRC has optimal stability and response speed.

4 Conclusion

In this study, a new MSTOGI-PLL device is designed for the UPQC phase-locking module, and by applying the second third-order generalized integrators, a module channel is constructed to eliminate the DC component, which realizes the effective separation of the DC and the negative-sequence components and, at the same time, realizes the effective compensation of the voltage and current under the influence of the voltage transient increase, transient decrease, and the nonlinear loads in the UPQC system. Compared with the traditional SRF-PLL device, the MSTOGI-PLL device can filter harmonics efficiently in the high- and low-frequency bands. The SRF-PLL device is insensitive to high- and low-frequency harmonics during the phase-locking process, and the locking takes longer, and the result of the output voltage positive-sequence component is more prone to overshooting than that of the MSTOGI-PLL, which will then affect the response speed of the UPQC.

In the controller selection, this study for the new MSTOGI-PLL device selected two nonlinear controllers, ADRC and second-order STA controllers, to study their suitability for the phase-locking device. The comparative analysis showed that both the nonlinear controllers in conjunction with MSTOGI are capable of compensating for the voltage and current quantities in the case of transient voltage increase, transient decrease, and nonlinear loads. However, when fighting against voltage transient increase and decrease disturbances, the ADRC controller is more resistant to disturbances, so that the UPQC system does not produce sudden changes in the output quantity, and at the same time, there is no control delay. In extreme environments, the UPQC system of MSTOGI-PLL + ADRC demonstrates better robustness with minimal voltage and current distortion. In extreme environments, such voltage and current distortions with harmonic components can interfere with the logic relationships of digital appliances in the circuit and reduce the rate of power supply. Thus, in extreme environments oriented to the simultaneous existence of multiple disturbances, the UPQC control system with fast response speed and lower degree of distortion can better achieve the compensation of the power system, improve the stability of the power system, and provide new ideas and references for the future power quality optimization problems of the power system.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material; further inquiries can be directed to the corresponding authors.

Author contributions

YY: data curation, software, writing–original draft, and writing–review and editing. DL: writing–review and editing and investigation. YC: data curation, formal analysis, and writing–review and editing.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

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