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Input-parallel output-series Si-SiC hybrid inverter with fractional harmonic elimination

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This paper proposes an input-parallel output-series (IPOS) Si-SiC hybrid inverter with dual-frequency harmonic elimination modulation strategy. The proposed topology composed of two power conversion cells and a three-phase five-column medium-frequency step-down transformer, the low-frequency power conversion cell (LFPC-C, 1 kHz) leverages strong current-carrying capacity of silicon-based devices for dealing with the system main power, and the high-frequency power conversion cell (HFPC-C, 30 kHz) based on wide-bandgap semiconductor SiC devices is used to addressing the fractional harmonics compensation power. This topology combines the strong current carrying capability of Si devices with the low switching loss of SiC devices at high frequency and achieves high quality power conversion at low cost and low loss. Compared to existing "IPOP" Si-SiC hybrid inverters, this topology adopts a coupling step-down transformer on the output side of both LFPC-C and HFPC-C, which can effectively reduce current stress of HFPC-C SiC devices. Additionally, a dual-frequency harmonic elimination modulation strategy based on the topology is proposed to solve the fractional harmonics caused by the LFPC-C. The paper establishes a mathematical model according to the harmonic distribution characteristics of the LFPC-C and HFPC-C, and designs the system control schedules. Building upon the derivation of the voltage ripple model and the design of hardware parameters, Si IGBT and SiC MOSFET were selected for constructing a 7.5 kW prototype for testing, and the experimental results validate the feasibility of this topology and the accuracy of theoretical analysis.

KEYWORDS

fractional power processing, harmonic compensation, dual-frequency harmonic elimination modulation strategy, multiple quasi-proportional resonance control, recursive discrete fourier transform, SHEPWM, Si-SiC inverter

1 Introduction

SiC MOSFET devices, leveraging their superior material properties, have become a key factor in enhancing the efficiency and power density of inverters, especially in high-frequency applications (Millán et al., 2014). The efficiency of inverters can reach as high as 99.4% (Miyazaki et al., 2018). Currently, SiC MOSFET devices have been successfully applied in naval and equipment power supply (Jones et al., 2016; Anurag et al., 2022), microgrids (Burkart and Kolar, 2017), and MMC (He et al., 2022).

However, SiC devices are costly and have a smaller current capacity, resulting in their rated power being lower than Si devices at the same voltage level. As shown in Figure 1, at

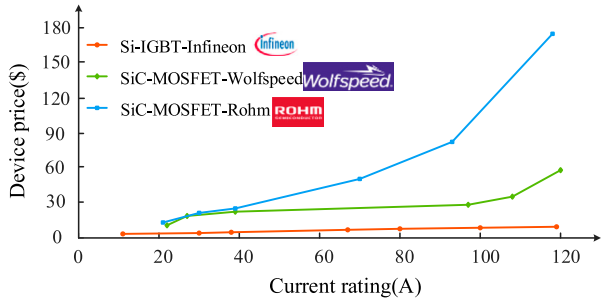

FIGURE 1
Price comparison between Si IGBT and SiC MOSFET from mainstream manufacturer.

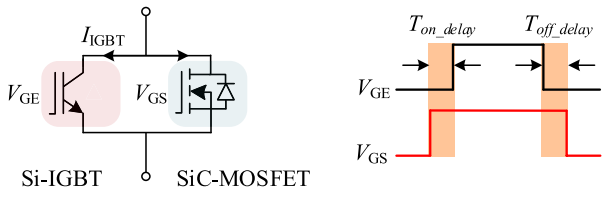

FIGURE 2
Si-SiC hybrid switch.

high currents, the current cost of SiC devices is significantly higher than that of Si devices. Therefore, it is necessary to maximize the advantages of SiC devices in high-power scenarios while reducing the cost of the inverter. Currently, to overcome the limitation of the low rated current of SiC devices, scholars are combining Si devices with SiC devices. This combination leverages the low switching loss characteristics of SiC devices and the strong current-carrying capacity and cost-effectiveness of Si devices. The design approach of using both types of devices together brings about good electrical power quality and efficiency at a cost lower than a full SiC device design. There are two solutions to address this: one is to parallel SiC devices with Si devices at the switch device level to form a Si-SiC hybrid switch (Rahimo et al., 2015; Song et al., 2015; Zhao and He, 2015; Zhang et al., 2018); the other is based on the principle of Fractional Power Processing (Di Gioia and Brown, 2015; Kundu et al., 2020) at the topology level, constituting a Si-SiC hybrid inverter.

The Si-SiC hybrid switch, as shown in Figure 2, can apply gate-source drive voltage to the SiC MOSFET and gate-emitter drive voltage to the Si-IGBT respectively. The turn-on delay and turn-off delay ensure zero voltage turn-on and turn-off of Si-IGBT, reducing switching losses and improving the efficiency and load capacity of the entire system (Li et al., 2020a). Reference (Deshpande and Luo, 2019) proposed an algorithm using dynamic junction temperature prediction to select the optimal Si-SiC current ratio, ensuring reliable operation of the hybrid switch. Reference (Li et al., 2020b) introduced an active gate delay control strategy based on an electro-thermal coupling loss model. This strategy dynamically adjusts and optimizes the gate delay time according to the operating conditions of the power converter, minimizing the working junction

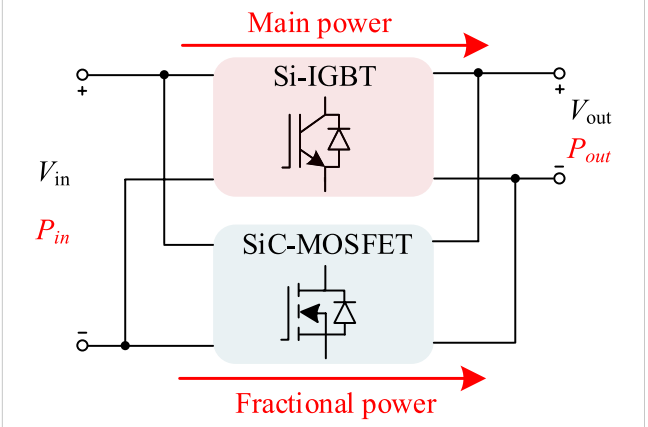

FIGURE 3
Si-SiC hybrid converter.

temperature difference between the two internal devices. Reference (Woldegiorgis et al., 2023) provided a comprehensive review and performance comparison of existing gate control strategies, gate driver designs, and packaging methods for Si-SiC hybrid switches. Design principles and guidelines were given for gate control strategies. However, significant progress in the commercial manufacture of Si-SiC hybrid switch modules has yet to be achieved.

Currently, most Si-SiC hybrid converters based on the Fractional Power Processing (FPP) principle consist of two parallel parts, as shown in Figure 3: one part comprises Si IGBT devices operating at low frequency to handle the main power, while the other part consists of SiC MOSFET devices operating at high frequency to process only a small portion of the total power. Both parts are connected in parallel on the input and output sides, forming an input-parallel and output-parallel structure. The Si-SiC hybrid converter divides the power processing path into two parallel paths. By setting the switching information of the S IGBT and SiC MOSFET devices, the continuous energy signal is converted into two discrete energy signals with different numerical values. These signals are then reconstructed and combined into the final continuous energy output through passive components (Kundu et al., 2021; Wang et al., 2022). Compared to topologies with all SiC MOSFET devices, this kind of topology achieves a reduction in circuit cost while maintaining almost the same efficiency and power quality. Based on intelligence particle swarm optimization (PSO), reference (Zhang et al., 2023) propose a novel adaptive power-sharing and switching frequency control, it can reduce the power losses of the Si-SiC hybrid converter through a simple fitness function. Reference (Endres and Ackva, 2015) proposes a combination topology where the converter composed of Si-IGBT devices carries the main load current, while the converter composed of SiC MOSFET devices is used for ripple current compensation. A common-mode current suppression strategy for this combined topology is also proposed. Reference (Judge and Finney, 2019) verifies that the parallel hybrid converter significantly increases the effective switching frequency at the megawatt power level, reducing the need for external filters and increasing the current control bandwidth of the converter. References (Wu et al., 2022; Wu et al., 2019) design a ripple compensation direct digital control

strategy that attenuates low-frequency current ripple to a small level and increases the frequency of the output current ripple, thereby reducing the volume and weight of the filter. Reference (Zhang et al., 2022) summarizes the characteristics of the input-parallel and output-series hybrid topology based on the FPP principle and proposes a hybrid bridge arm design method based on current harmonic elimination. The proposed design method can be implemented in various converters and has been validated in a bidirectional DC/DC converter. Unlike the "input-parallel and output-series "structure in the aforementioned references, the converter proposed in reference (Liu et al., 2022) has a parallel DC input and a series AC output through a transformer on the AC side, forming a "input-parallel and output-series" structure, aimed at harmonic control of the inverter output voltage.

Based on the concept of Fractional Power Processing (FPP), this paper introduces a hybrid Si-SiC three-phase inverter composed of Si IGBT and SiC MOSFET devices, following the "input-parallel and output-series" topology structure. The low-frequency power conversion cell (LFPC-C) consists of Si IGBT devices and LC filters to handle the main power output. The high-frequency power conversion cell (HFPC-C) is composed of SiC MOSFET devices and LC filters, designed to compensate for the harmonics generated in the LFPC-C. The outputs of the LFPC-C and HFPC-C are connected in series through a three-phase five-column intermediate voltage transformer, reducing the current stress on SiC MOSFET in the HFPC-C. This topology leverages the strong conduction capabilities of Si IGBT and the low switching losses of SiC MOSFET during high-frequency operation. The proposed hybrid modulation strategy and coordinated control method, "LFPC-C open-loop, HFPC-C closed-loop" reduce the complexity of the control system. Hardware design methods are also presented based on the frequency characteristics of the LFPC-C and HFPC-C.

The rest of this article is organized as follows. Section 2 introduces the topology principle and dual-frequency harmonic elimination modulation strategy. In Section 3, it derives the frequency-domain mathematical model and proposes the control method. Section 4 analyzes its hardware characteristics, proposes a voltage ripple analysis model, and outlines the design principles for the filter and three-phase five-column medium-frequency step-down transformer. In Section 5, the feasibility of the topology is validated through the experimental setup. Finally, Section 6 concludes this article.

2 Topology of proposed inverter and harmonic elimination methods

2.1 Topology of proposed inverter

The proposed hybrid Si-SiC three phase inverter topology, as shown in Figure 4, consists of a low-frequency power conversion cell (LFPC-C),a high-frequency power conversion cell (HFPC-C) and a three-phase five-column medium-frequency step-down transformer. The input side is parallel and shared by a common DC source, and the outputs are coupled in series through the transformer. The LFPC-C employs Si IGBT devices as switching devices denoted as S1 ~ S6, operating at a low switching frequency to deal with the main power of the proposed three-phase inverter. The HFPC-C uses SiC MOSFET devices as switching devices denoted as Q1 ~ Q6, operating at a high switching frequency to handle fractional power. The transformer turns ratio is denoted as k, with the primary side parallel-coupled to the output filtering capacitor of the HFPC-C and the secondary side series-coupled and connected to the LFPC-C.

This topology realizes power sharing in two power conversion cells. Under the same DC side voltage, this topology reduces the switching losses of Si IGBT devices in the LFPC-C. Additionally, the step-down transformer ensures that the working current in the HFPC-C is less than the output current in the LFPC-C, reducing the current stress on SiC MOSFET devices and lowering on-state losses in the HFPC-C. The switching losses are concentrated on SiC MOSFET devices, and leveraging their excellent characteristics helps reduce the system's overall switching losses.

2.2 Dual-frequency harmonic elimination modulation strategy

The LFPC-C is responsible for the energy output of the system. However, due to its operation at a low frequency, it can lead to lower electrical energy quality in the final output of the system. Therefore, the HFPC-C needs to compensate and eliminate some of the harmonics present in the LFPC-C t to enhance the overall electrical energy quality of the system. The final output voltage of the system is composed of the voltage in the LFPC-C and the voltage on the secondary side of the transformer. The voltage in the LFPC-C is composed of the fundamental voltage and the harmonic voltage, while represents the output voltage of the HFPC-C. The relationship between these variables can be expressed as follows

$$\begin{cases} V_{out} = u_h - v_{SiC} \\ u_h = u_h^{(1)} + u_h^{(h)} \\ v_{SiC} = V_{SiC}/k \end{cases} \tag{1}$$

The bridge arm output characteristics of the LFPC-C significantly impact the overall system performance. Specific Harmonic Elimination Pulse Width Modulation (SHEPWM) technology can eliminate particular harmonics, and the switching angles can be calculated through computations. SHEPWM operates at a low switching frequency, which helps in reducing the switching losses of the Si-IGBT devices. When using traditional SHEPWM to eliminate harmonics in the mid to low frequency range, it results in a large number of switching angles and necessitates a higher switching frequency. By serially connecting the HFPC-C and the transformer to the output circuit of the LFPC-C, certain harmonics in the bridge arm output of the LFPC-C can be eliminated. This approach ensures a reduction in the switching frequency of Si-IGBT devices in the LFPC-C, thus reducing switching losses while maintaining the total amount of eliminated output harmonics. In the HFPC-C, a Hybrid Sinusoidal Pulse Width Modulation (Hybrid SPWM) is employed. Hybrid SPWM refers to modulating the waveform, which is not a single-frequency sine wave but is determined by the superposition of multiple harmonic waves.

The collaborative elimination of mid to low-frequency harmonics by the LFPC-C and the HFPC-C involves segmenting the mid to low-frequency harmonics. Two technical approaches can be considered based on the harmonic distribution characteristics in the LFPC-C:

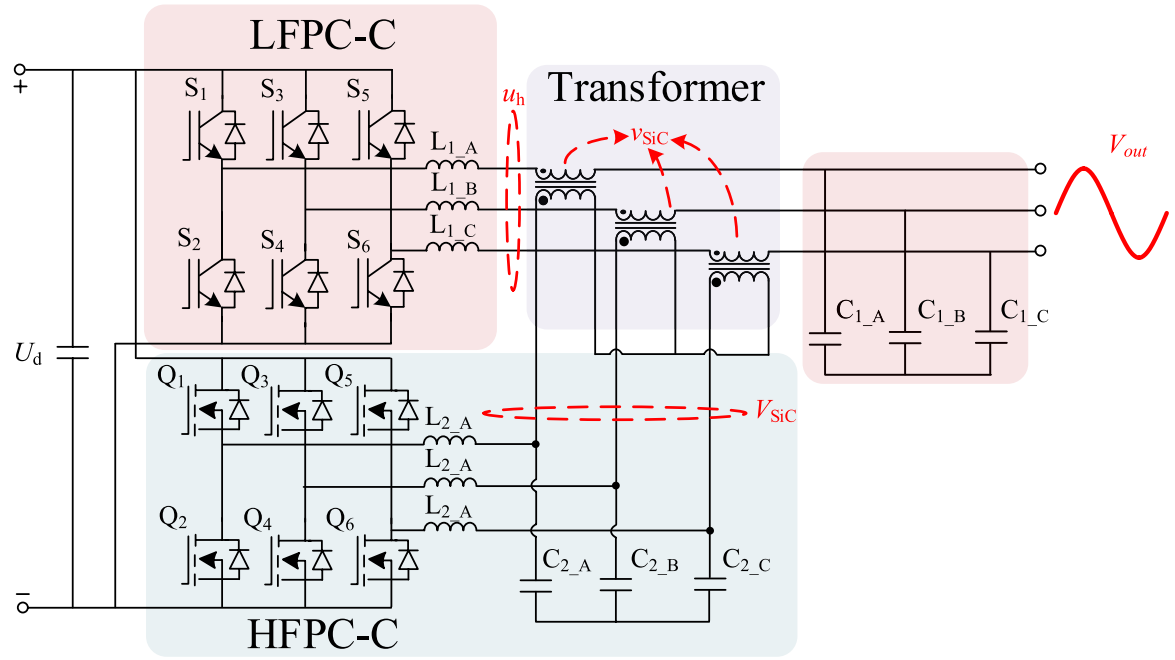

FIGURE 4
The proposed hybrid Si-SiC three phase inverter topology.

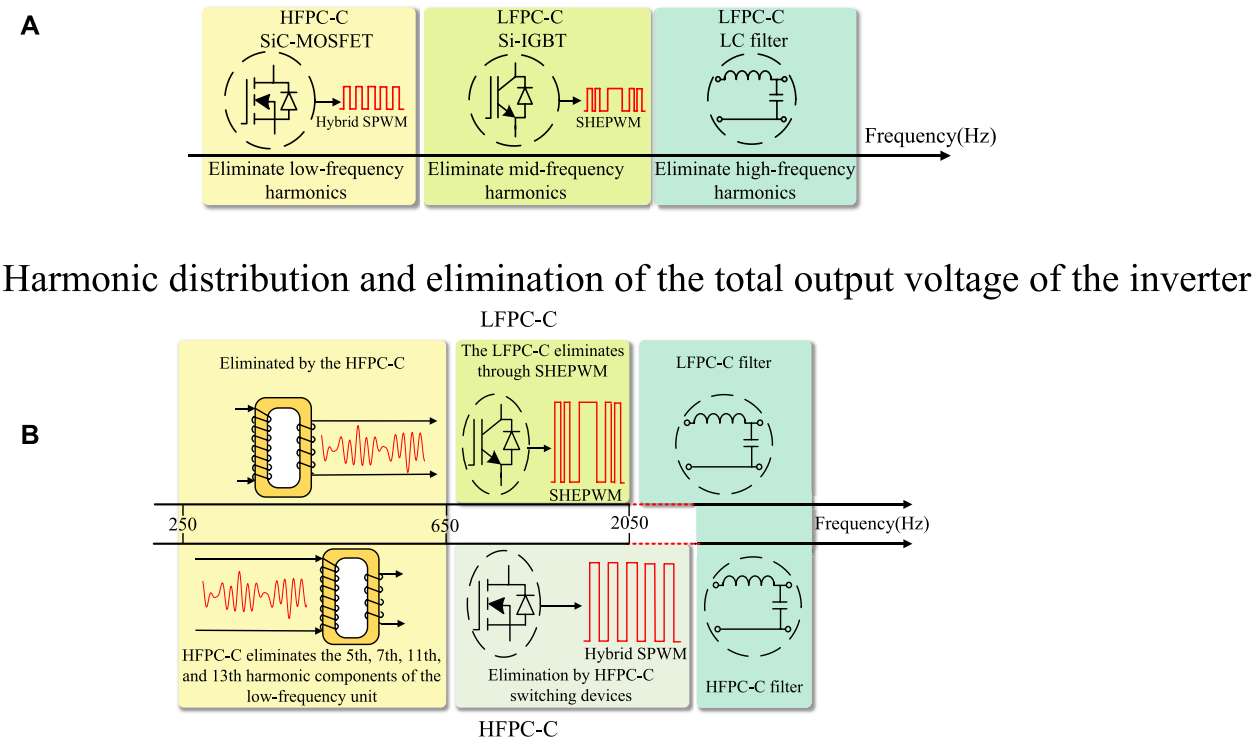

FIGURE 5
Harmonic distribution and elimination of the inverter.

Method 1: The LFPC-C eliminates mid-frequency and high-frequency harmonics, while the HFPC-C eliminates low-frequency harmonics.

Method 2: The LFPC-C eliminates low-frequency and high-frequency harmonics, and the HFPC-C eliminates mid-frequency harmonics.

According to the residual harmonic distribution characteristics of SHEPWM (Cheng, 2021), both methods merely shift the harmonic energy to other frequency bands. However, when employing Method 2, where the LFPC-C eliminates low-frequency and high-frequency harmonics, and the mid-frequency harmonics are eliminated by the HFPC-C, it results in the HFPC-C handling harmonics excessively. The equivalent harmonic frequency within one power cycle can reach several kilohertz, demanding higher requirements for the control system and switching frequency of SiC MOSFET devices in the HFPC-C, thus increasing the switching losses of SiC MOSFET devices. Therefore, Method one is adopted, where the LFPC-C eliminates mid-frequency and high-frequency harmonics while the HFPC-C eliminates low-frequency harmonics. As illustrated in Figure 5A, the LFPC-C is responsible for system energy output, using SHEPWM to remove mid-frequency harmonics. The low-frequency harmonics are eliminated by the HFPC-C, and the high-frequency harmonics are eliminated by the LFPC-C's filter. The HFPC-C compensates and eliminates low-frequency harmonics in the LFPC-C.

When employing the first technical approach, the specific division of mid to low-frequency harmonics and the modulation degree of the hybrid modulated waves m_x in the HFPC-C, as well as the selection of transformer turns ratio k, pose constraints. The effective division and treatment of mid to low-frequency harmonics in the LFPC-C and determining the appropriate modulation degree in the HFPC-C are essential for achieving effective harmonic elimination. Additionally, the choice of transformer turns ratio is crucial as it impacts the coupling between the high-frequency and LFPC-C, thereby influencing the overall harmonic elimination performance and system efficiency. Careful consideration and proper optimization of these parameters are necessary to ensure optimal performance in mitigating harmonics and achieving efficient energy conversion in the system.

The low-frequency harmonics to be eliminated in the LFPC-C represent a modulation signal composed of multiple harmonics for the HFPC-C. In SHEPWM modulation, once the fundamental modulation degree and switching angles are determined, the remaining harmonic superposition waveform becomes fixed. The LFPC-C uneliminated low-frequency harmonic family can be represented as $u_h^{(h\_low)}$.

When a three-phase inverter is connected to a balanced load on the output side, The third harmonic and its multiples cancel each other out in the line-to-line voltage, hence we only need to focus on eliminating 6k±1 harmonics (k = 1, 2, 3, ...).

In a three-phase half-bridge configuration, peak value of the output phase voltage U_{phm} is:

$$U_{phm} = 0.5 m_{SiC}(t) U_d \tag{1a}$$

The variable $m_{SiC}(t)$ represents the modulation index for the hybrid sinusoidal carrier modulation in the HFPC-C. The expression for the hybrid modulated wave $m_{SiC}(t)$ is:

$$m_{SiC}(t) = m_5 \sin(5\omega t + \theta_5) + \cdots + m_i \sin(i\omega t + \theta_i) \tag{2}$$

The transformer is a crucial coupling component connecting the LFPC-C and the HFPC-C. Through its turns ratio k, a relationship between Eqs 1, 2 is established, yielding the following correlation

$$k \le \frac{m_{SiC}(t) U_d}{2 u_h^{(h\_low)}} \tag{3}$$

The modulation index of the HFPC-C and the transformer turns ratio constrain each other. If the turns ratio k is chosen to be too large, it can lead to over-modulation in the HFPC-C. This over-modulation can introduce harmonics from other frequency bands into the output voltage of the LFPC-C, thereby degrading the quality of the output waveform. On the other hand, if the turns ratio k is chosen to be too small, it can cause the current in the HFPC-C to approach the output current in the main circuit, increasing the current cost of SiC MOSFET devices.

The LFPC-C in this paper is responsible for eliminating harmonics from the 17th to the 41st order. Meanwhile, the HFPC-C compensates and eliminates the fifth, seventh, 11th, and 13th order harmonics.

The bridge arm output voltage waveform of the LFPC-C using SHEPWM is shown in (Supplementary Figure S1).

The output waveform in Figure 6 is symmetric about a 1/4 period, and it can be represented using a Fourier series as follows

$$u(\omega t) = \sum_{n=1,17\cdots}^{41} a_n \sin n\omega t \tag{4}$$

In the equation, a_n represents the amplitude of harmonics. The expressions for the fundamental and the 17th to 41st harmonic components are as follows:

$$\begin{cases} a_1 = \dfrac{2V_d}{n\pi} \sum_{i=1}^{10} (-1)^{i+1} \cos n\alpha_i = \mathrm{U}_1 \\ a_{17} = \dfrac{2V_d}{n\pi} \sum_{i=1}^{10} (-1)^{i+1} \cos n\alpha_i = 0 \\ a_{19} = \dfrac{2V_d}{n\pi} \sum_{i=1}^{10} (-1)^{i+1} \cos n\alpha_i = 0 \\ \vdots \\ \vdots \\ a_{41} = \dfrac{2V_d}{n\pi} \sum_{i=1}^{10} (-1)^{i+1} \cos n\alpha_i = 0 \end{cases} \tag{5}$$

In the equation, α_i represents the switching angle. The modulation ratio m is defined as (Dong et al., 2024)

$$m = \frac{U_1}{U_d/2} \tag{6}$$

The HFPC-C employs hybrid sinusoidal pulse width modulation technique, where the modulation wave is composed of fifth, seventh, 11th, and 13th harmonic sinusoidal waves. The expression is:

$$\begin{aligned} m_{SiC}(t) = {} & m_5 \sin(5\omega t + \theta_5) + m_7 \sin(7\omega t + \theta_7) \\ & + m_{11} \sin(11\omega t + \theta_{11}) + m_{13} \sin(13\omega t + \theta_{13}) \end{aligned} \tag{7}$$

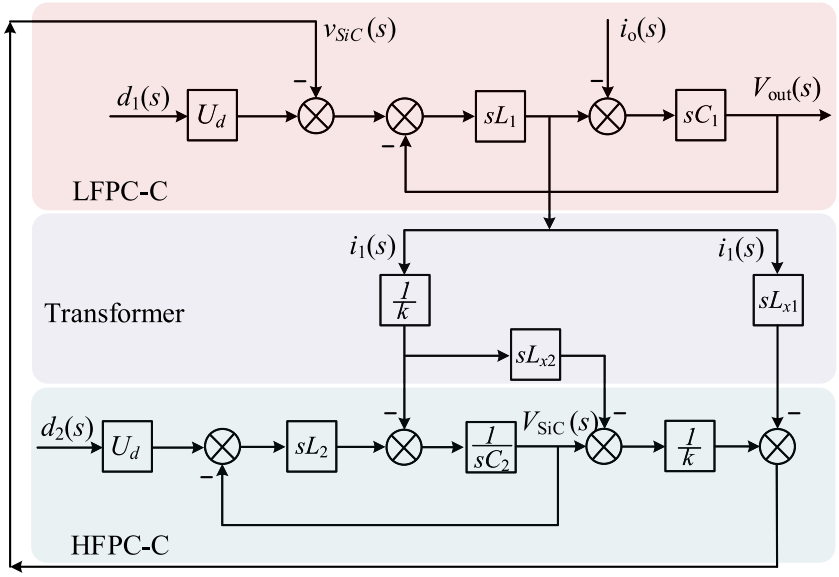

FIGURE 6
Mathematical model in frequency domain.

Taking the modulation index m = 0.97 as an example, the schematic diagram of the modulated wave and the triangular carrier wave for the HFPC-C is shown in (Supplementary Figure S2).

3 Mathematical model and control methods of the proposed inverter

In this section, based on the time-domain coupling relationship of the 2 cells mentioned above, a frequency-domain mathematical model is established. Frequency domain analysis of the system is conducted, and a control method for the system is proposed.

3.1 Mathematical models

The mathematical model is as shown in Figure 6, and there are two switch degrees of freedom, denoted as $d_1(s)$ and $d_2(s)$, in the overall control circuit. and L_{x1}、 L_{x2} respectively refer to the leakage inductance on the secondary and primary sides of the transformer.

The relationship between $V_{SiC}(s)$, $d_2(s)$ and $i_1(s)$ can be deduced from the block diagram.

$$V_{SiC}(s) = \frac{U_d}{1 + L_2C_2s^2}d_2(s) + \left(\frac{L_2s}{1 + L_2C_2s^2} - L_{x2}s\right)\frac{i_1(s)}{k} \quad (8)$$

$H(s)$ can be represented as:

$$H(s) = \frac{\frac{L_2s}{1+L_2C_2s^2} - L_{x2}s}{k} \quad (9)$$

and

$$v_{SiC}(s) = \frac{V_{SiC}(s)}{k} + sL_{x1}i_1(s) \quad (10)$$

The relationship between $v_{SiC}(s)$, $d_2(s)$ and $i_1(s)$ can be derived as follows:

$$v_{SiC}(s) = \frac{U_d}{k(1 + L_2C_2s^2)}d_2(s) + \left(\frac{H(s)}{k} + L_{x1}s\right)i_1(s) \quad (11)$$

If the secondary-side leakage inductance is attributed to the LFPC-C filter inductance, $L_1^{'} = L_1 + L_{x1}$, If we consider $v_{SiC}(s)$ as an input for the LFPC-C, we can create an equivalent system diagram.

Let $d_2(s)$ and $i_o(s)$ be 0 separately, and determine the relationship between $V_{out}(s)$ and $d_1(s)$

$$V_{out}(s) = \frac{U_d d_1(s)}{1 + \frac{C_1H(s)}{k}s + L_1^{'}C_1s^2} \quad (12)$$

Let $d_1(s)$ and $i_o(s)$ be 0 separately, and determine the relationship between $V_{out}(s)$ and $d_2(s)$

$$V_{out}(s) = \frac{-U_d d_2(s)}{k(1 + L_2C_2s^2)\left(1 + \frac{C_1H(s)}{k}s + L_1^{'}C_1s^2\right)} \quad (13)$$

Let $d_1(s)$ and $d_2(s)$ be 0 separately, and determine the relationship between $V_{out}(s)$ and $i_o(s)$

$$V_{out}(s) = -\frac{L_1^{'}s + \frac{H(s)}{k}}{1 + L_1^{'}C_1s^2 + \frac{H(s)C_1}{k}s}i_o(s) \quad (14)$$

Finally, we can obtain the following expression:

$$V_{out}(s) = G(s)\left[U_d\left(d_1(s) - \frac{d_2(s)}{k(1 + L_2C_2s^2)}\right) - \left(L_1^{'}s + \frac{H(s)}{k}\right)i_o(s)\right] \quad (15)$$

$G(s)$ can be expressed as

$$G(s) = \frac{1}{1 + L_1^{'}C_1s^2 + \frac{H(s)C_1}{k}s} \quad (16)$$

3.2 Integrated coordinated control method

From Eqs 13, 14, it can be seen that the circuit has two degrees of freedom, $d_1(s)$ and $d_2(s)$. The choice of closed-loop control target is also related to the level of control difficulty. If the overall output voltage V_{out} of the system is chosen as the closed-loop target voltage, we need to consider not only $d_2(s)$ but also the impact of $d_1(s)$. Here, $d_1(s)$ represents the SHEPWM modulation of the LFPC-C, which has drawbacks such as real-time complex computation and poor dynamic adjustment performance. Having two input variables significantly increases the difficulty of closed-loop control.

Since the control objective is to compensate for the secondary-side voltage of the transformer, fundamentally, the closed-loop control aims to control the secondary-side voltage of the transformer. Therefore, in designing the closed-loop control circuit, the effect of the LFPC-C current on the HFPC-C can be considered as a disturbance. We propose a coordinated control method, "LFPC-C open-loop, HFPC-C closed-loop". In this approach, the LFPC-C uses open-loop SHEPWM control to adjust the voltage by only adjusting the fundamental modulation ratio, reducing the control difficulty for the HFPC-C. The HFPC-C achieves precise voltage regulation, compensating for the limitations of SHEPWM.

When processing the fifth, seventh, 11th, and 13th harmonic components in the HFPC-C and extracting the control system's reference signal, the following two points need to be considered:

1) The physical sampling point is located between the inductance of the LFPC-C and the secondary side of the transformer. The sampled voltage still contains the uneliminated high-frequency harmonics, which are not the target of the HFPC-C tracking control.
2) Regarding the selected fifth, seventh, 11th, and 13th harmonic components frequency domain characteristics: zero gain and zero phase shift.

Considering the above two points, Recursive Discrete Fourier Transform is used to meet the aforementioned requirements. The expression is as follows:

$$G^i_{RDFT} = \sum_{i=5、7、11、13} \frac{2}{N} \frac{\left(1-z^{-N}\right)\left(1-z^{-1}\cos 2\pi\frac{i}{N}\right)}{\left(1-z^{-1}e^{j2\pi\frac{i}{N}}\right)\left(1-z^{-1}e^{-j2\pi\frac{i}{N}}\right)} \tag{17}$$

Amplitude-frequency response and phase-frequency response of $G^i_{RDFT}(s)$ is shown in (Supplementary Figure S3).

The above equation yields the reference signal v_{ref} for the closed-loop control of the HFPC-C, which is then compared with the output voltage v_{SiC} of the transformer secondary side, and obtain the error signal Δv.The control loop consists of voltage and current double loops. Due to the presence of multiple harmonic voltages in the output voltage and the need for high precision, a multiple Quasi-Proportional Resonant (QPR) voltage outer loop is employed to process the error signal Δv, the transfer function is given by:

$$G_{QPR}(s) = K_{pv} + \sum_{i=5、7、11、13} \frac{2K_{iv}w_c s}{s^2 + 2w_c s + w_i^2} \tag{18}$$

ω_i is the angular frequency of the 5th to 13th harmonic components, ω_c is the damping coefficient. K_{iv} is the resonance coefficient, K_{pv} is the proportional coefficient.

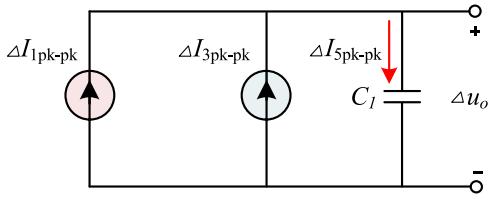

FIGURE 7
Equivalent circuit of LFPC-C ripple current source.

Obtaining the current inner-loop reference signal i_{ref}, sampling the capacitor current to obtain i_c, The inner loop adopts proportional control of the capacitor current to improve

The response speed. Controlling the inner loop with the capacitor current as the control target can increase system damping, suppress resonance, and reduce the difficulty of voltage outer loop control.

$$G_i(s) = K_i \tag{19}$$

The transfer function of the closed-loop control for the HFPC-C is

$$G_v(s) = \frac{K_i U_d}{L_2 C_2 s^2 + C_2 K_i U_d s + 1} G_{QPR}(s) \tag{20}$$

The overall control policy is shown in Supplementary Figure S4.

4 Key parameters design of proposed inverter

4.1 Voltage ripple analysis

When considering voltage compensation by the HFPC-C for the LFPC-C, it is necessary to establish a steady-state voltage ripple model. The primary side of the series-coupled transformer is connected in parallel across the filtering capacitor of the HFPC-C. Neglecting the fundamental component in the circuit, the ripple in the primary-side voltage is equivalent to a voltage source ΔU_2 on the secondary side, As shown in (Supplementary Figure S5), there are two voltage sources in the LFPC-C circuit, and the corresponding ripple currents are shown in Figure 7, the ripple current generated by the output voltage U_{Si} and the inductance L_1 in the LFPC-C bridge arm is denoted by ΔI_{3pk-pk} (Mao et al., 2009), and its expression is as follows:

$$\Delta I_{1pk-pk} = \frac{U_d T_{s1}}{L_1}\left[1 - D_{Si}(t)\right] D_{Si}(t) \tag{21}$$

In the equation, T_{s1} represents the switching period, $D_{Si}(t)$ denotes the average duty cycle. Due to the adoption of SHEPWM modulation in the LFPC-C, by calculating for different switching signal sequences, $D_{Si}(t)$ for one complete switching action can be obtained.

$$D_{Si}(t) = \frac{\sum_{i=1}^{N-1}(\alpha_{i+1} - \alpha_i)}{2\pi} T_s \tag{22}$$

ΔI_{3pk-pk} represents the ripple current generated in the LFPC-C circuit under the excitation of ΔU_2, and its expression is:

$$\begin{cases} \Delta I_{3\,pk-pk} = \dfrac{\Delta U_2}{z} \\ z = w_x L - \dfrac{1}{w_x C} \end{cases} \tag{23}$$

The total ripple current ΔI_{5pk-pk} in the LFPC-C is constituted by the two equivalent ripple current sources ΔI_{1pk-pk} and ΔI_{3pk-pk}:

$$\Delta I_{5pk-pk} = \Delta I_{1pk-pk} + \Delta I_{3pk-pk} \tag{24}$$

The expression for the total output ripple voltage ΔU_o is given by:

$$\Delta U_o = \frac{T_{s1}^3 U_d (\omega_x L_1 C_1 - 1)\left[2\pi - \left(\sum_{i=1}^{N-1} \alpha_{i+1} - \alpha_i\right)\right]\left(\sum_{i=1}^{N-1} \alpha_{i+1} - \alpha_i\right) + 4\pi^2 L_1 C_1 \omega_x \Delta U_2}{32 L_1 C_1 f_{s1} \pi^2 \left(\omega_x^2 L_1 C_1 - 1\right)} \tag{25}$$

The ripple analysis for the HFPC-C is illustrated in Figure 10.

The parameter ΔI_{2pk-pk} is determined by the output voltage U_{SiC} of the HFPC-C bridge arm, the inductance L_2, and the amplitude m_{SiC} of the non-sinusoidal fundamental modulation wave. The expression is as follows:

$$\Delta I_{2pk-pk} = \frac{U_d T_{s2}}{L_2} (1 - m_{SiC}|\sin \omega t|) m_{SiC}|\sin \omega t| \tag{26}$$

The ripple in the output current of the LFPC-C bridge arm is represented by ΔI_{5pk-pk}, and it can be equivalently modeled as ΔI_{6pk-pk} on the primary side of the series-coupled transformer.

$$\Delta I_{6pk-pk} = \frac{\Delta I_{5pk-pk}}{k} \tag{27}$$

The total ripple current ΔI_{4pk-pk} in the HFPC-C is formed by the combination of the two equivalent ripple current sources ΔI_{2pk-pk} and ΔI_{6pk-pk}.

$$\Delta I_{4pk-pk} = \Delta I_{2pk-pk} + \Delta I_{6pk-pk} \tag{28}$$

The ripple voltage on the filter capacitor of the HFPC-C is represented by ΔU_1

$$\Delta U_1 = \frac{\Delta I_{4pk-pk}}{8 C_2 f_{s2}} \tag{29}$$

Based on $\Delta U_2 = \Delta U_1/k$, ΔU_2 can be determined as follows:

$$\Delta U_2 = \frac{k U_d T_{s2} (\omega_x{}^2 L_1 C_1 - 1)(1 - m_{SiC}|\sin \omega t|)}{8 L_2 C_2 f_{s2} k^2 \left(\omega_x^2 L_1 C_1 - 1\right) - \omega_x C_1} m_{SiC}|\sin \omega t| \tag{30}$$

Substituting into Eq. 26, ΔU_o is determined as follows:

$$\begin{cases} \Delta U_o = \dfrac{Y \bullet [8 L_2 C_2 f_{s2} k^2 (\omega_x^2 L_1 C_1 - 1) - \omega_x C_1] + 4\pi^2 L_1 C_1 \omega_x k U_d T_{s2} (\omega_x{}^2 L_1 C_1 - 1)(1 - m_{SiC}|\sin \omega t|) m_{SiC}|\sin \omega t|}{[32 L_1 C_1 f_{s1} \pi^2 (\omega_x^2 L_1 C_1 - 1)] \bullet [8 L_2 C_2 f_{s2} k^2 (\omega_x^2 L_1 C_1 - 1) - \omega_x C_1]} \\ Y = T_{s1}^3 U_d (\omega_x L_1 C_1 - 1)\left[2\pi - \left(\sum_{i=1}^{N-1} \alpha_{i+1} - \alpha_i\right)\right]\left(\sum_{i=1}^{N-1} \alpha_{i+1} - \alpha_i\right) \end{cases} \tag{31}$$

Supplementary Figure S7, Figure 8 in Additional files illustrates the ratio of output voltage ripple to DC voltage on the direct current (DC) side based on Eq. 31 for different parameters chosen for L_1 and L_2.

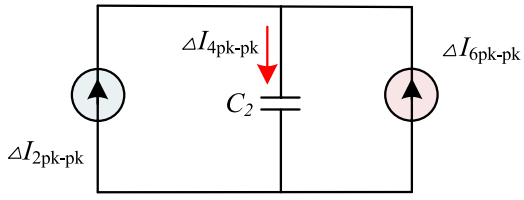

FIGURE 8
Equivalent circuit of ripple current source in HFPC-C.

4.2 Design of second-order filters for LFPC-C and HFPC-C

As shown in Figure 5B above, the filters in the low-frequency and HFPC-C filter different ranges of harmonics. Additionally, the compensation of voltage ripples in the HFPC-C and the final circuit output ripples in the LFPC-C, as analyzed in the previous section, are closely related to the selection of passive components L_1、L_2、$C_1$and C_2 in the circuit. Considering the constraints mentioned above, frequency domain constraints also need to be taken into account.

For the LFPC-C, as shown in Figure 5B above, the harmonics from the 5th to the 13th order are eliminated through the HFPC-C, and the harmonics from the 17th to the 41st order are already eliminated through SHEPWM. The remaining harmonics in the high-frequency range are eliminated through a second-order low-pass LC filter. The cutoff frequency f_{Si} of the second-order filter should be set in the mid-frequency range, specifically between 650 Hz and 2050 Hz:

$$\begin{aligned} f_{Si} &= \frac{1}{2\pi\sqrt{L_1 C_1}} \\ 650Hz &< f_{Si} < 2050Hz \end{aligned} \tag{32}$$

Simultaneously, to prevent resonance peaks in the LFPC-C filter and to amplify the fifth, seventh, 11th, and 13th harmonics, increasing the compensation difficulty for the HFPC-C, requirements are imposed on the damping coefficient of the filter ζ:

$$\begin{aligned} \zeta &= \frac{1}{2R_1}\sqrt{\frac{L_1}{C_1}} \\ \zeta &\le 0.7 \end{aligned} \tag{33}$$

The HFPC-C compensates for the highest harmonic frequency at 650 Hz. The selected switching frequency is 30 kHz, and the upper limit for the filter cutoff frequency f_{SiC} is set to 3000 Hz, with a lower limit of 1000 Hz. This setting ensures that the highest compensating harmonic (650 Hz) can pass through without attenuation, providing an allowance:

$$\begin{aligned} f_{SiC} &= \frac{1}{2\pi\sqrt{L_2 C_2}} \\ 1000Hz &< f_{SiC} < 3000Hz \end{aligned} \tag{34}$$

4.3 Design of three-phase five-column medium-frequency step-down transformer

Due to the non-sinusoidal periodic components of the input terminal voltage injected into the transformer, which is a

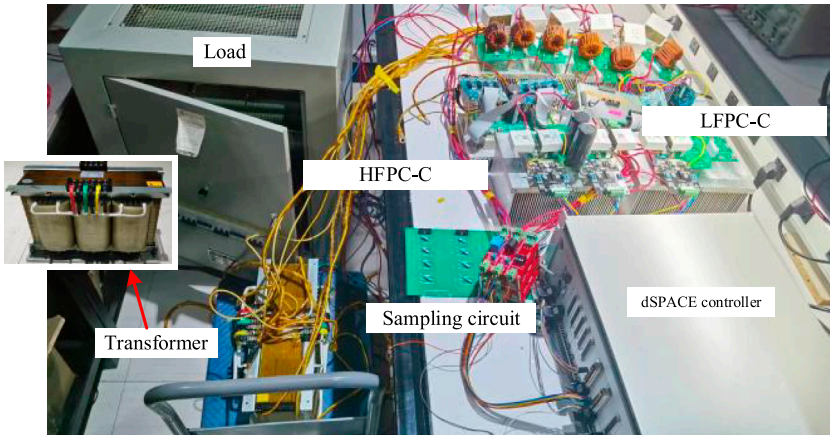

FIGURE 9
Experimental prototype.

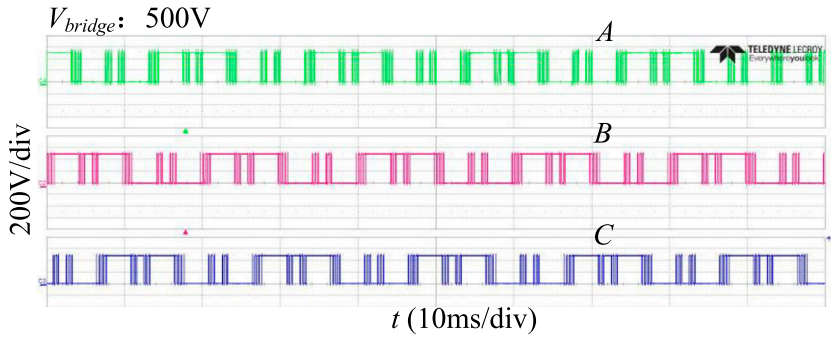

FIGURE 10
LFPC-C bridge arm output voltage.

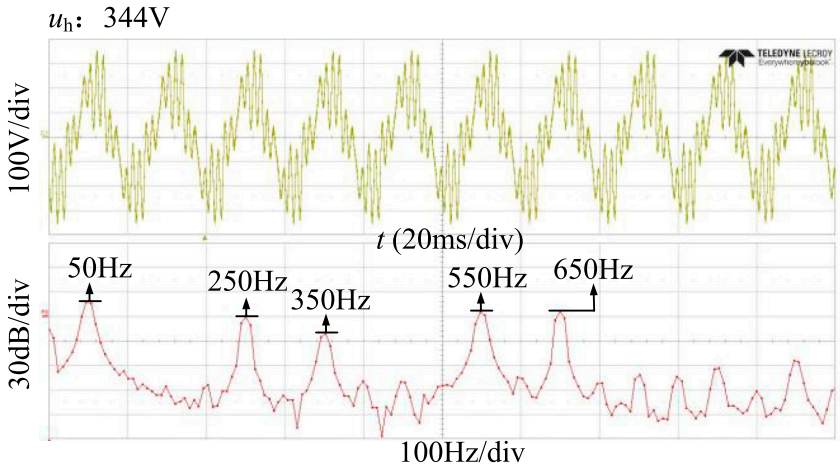

FIGURE 11
The voltage u_h between the inductor of the LFPC-C and the inlet end of the secondary side of the transformer.

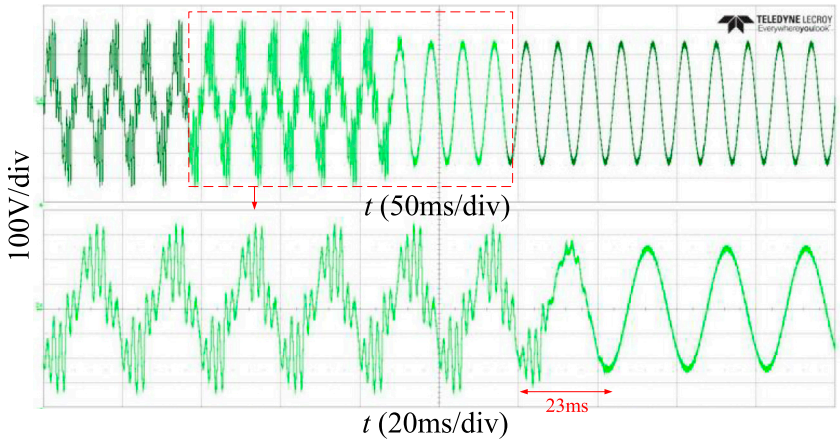

FIGURE 12
Dynamic response of HFPC-C compensation.

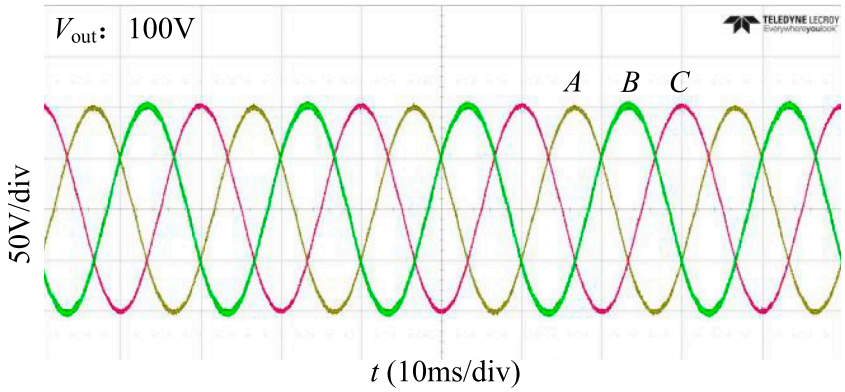

FIGURE 13
When m = 0.4, the final output voltage V_{out} waveform of Inverter.

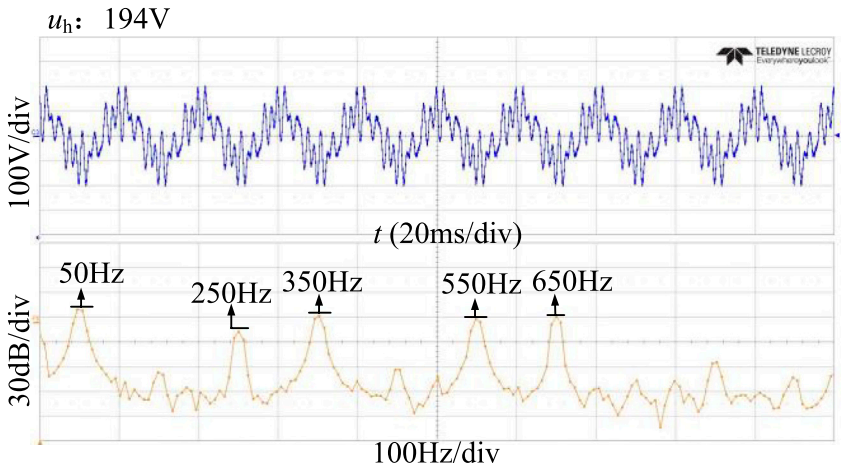

FIGURE 14
The voltage u_h between the inductance of the LFPC-C and the transformer.

superposition of fifth, seventh, 11th, and 13th harmonic voltages, a three-phase five-column medium-frequency transformer is used. This ensures that the high-order harmonic flux can circulate smoothly, and harmonics can flow in the independent magnetic circuits of the three-phase five-column medium-frequency transformer (Leung et al., 2010). When the circuit operates normally, the highest harmonic frequency allowed to pass through is 650 Hz. This necessitates the transformer to have a relatively high passband. Additionally, due to the higher frequency of voltage polarity conversions, losses will increase. Therefore, thin silicon steel sheets are used for the transformer core. Thin silicon steel offers advantages such as high saturation magnetic flux density, ideal loss performance, and low noise. Transformer model is displayed in (Supplementary Figure S9). The length of the transformer is 45cm, the height is 25 cm and the width is 19 cm.

To ensure minimal voltage distortion, it is crucial to maintain the magnetic flux of the transformer in a non-saturated state and operate within the linear region (Li et al., 2011). The magnetic flux density B_i corresponding to each frequency component is:

$$B_i = \frac{U_i}{4.44 f_i N A_c} \tag{35}$$

U_i and f_i represent the effective values and frequencies of each component, N is the turns of the transformer, and A_c is the effective magnetic area of the magnetic circuit. According to the superposition principle, the composite flux density $B_{\max}$ at its maximum can be obtained as follows:

$$B_{\max} = B_5 + B_7 + B_{11} + B_{13} \tag{36}$$

5 Experimental validation

Based on the proposed inverter and control method in this paper, a laboratory prototype with a power rating of 7.5 kW was set up in this section. The experimental setup, as shown in Figure 9, includes a dSPACE controller, a LFPC-C, a HFPC-C, a load, a transformer, and a sampling circuit. The parameters and values used in the experiment are listed in Additional files (Supplementary Table 1).

The output voltage of the LFPC-C bridge arm is shown in Figure 10. It can be observed from Additional files (Supplementary Figure S10) that the bridge arm output voltage V_{bridge} conforms to the SHEPWM modulation principle proposed in Section 2.2, as referenced in Additional files (Supplementary Figure S11).

During steady-state operation, the waveforms of the final output voltage V_{out} and output current I_1 for the LFPC-C, as well as the current I_2 for the HFPC-C, are shown in Additional files (Supplementary Figure S11). Additionally, I_2 and I_1 represent the currents on the primary and secondary sides of the transformer. It can be observed from Additional files (Supplementary Figure S12) that the current in the HFPC-C is approximately half of the current in the LFPC-C.

Figure 11 presents the Fourier Transform (FFT) analysis of u_h. Experimental results demonstrate that the harmonics in the LFPC-C circuit without compensation include a significant amount of 5th to 13th harmonics

Additional files (Supplementary Figure S13) shows the three phase voltage at the primary side of the transformer. Through FFT decomposition, it can be observed that the voltage contains harmonics at 250 Hz, 350 Hz, 550 Hz, and 650 Hz.

Figure 12 verifies the dynamic performance of the system. From the figure, it can be observed that the transient duration for the compensation of the LFPC-C by the HFPC-C is 23 m, demonstrating the rationality of the harmonic extraction and control design.

Supplementary Figure S14 displays the Fourier Transform (FFT) analysis of the output voltage V_{out}. The total harmonic distortion of the output voltage is approximately 1.02%.

Supplementary Figure S15 shows the waveforms of total output voltage, output current, and transformer primary and secondary side voltages for phase A.

Figure 13 depicts the voltage waveform at a low modulation index of m = 0.4, with a peak value of 100V.

Figure 14 and (Supplementary Figure S15) represent the FFT of u_h and the primary side voltage V_{SiC} of the transformer when m = 0.4. The sequence from Figures 13, 14, (Supplementary Figure S16) demonstrate that the proposed inverter can operate effectively under low modulation ratios.

6 Comparative analysis

To demonstrate the efficiency of the proposed converter, a theoretical comparison was made between the proposed converter, a hybrid switch converter, and an Si-IGBT converter. Considering high-power applications, the theoretical converter's DC voltage was set to 800 V, and the efficiency curves are shown in Additional files (Supplementary Figure S17).

From (Supplementary Figure S17), it can be observed that the highest efficiency of the converter proposed in this paper is 98.3%. As the load percentage exceeds 50%, the efficiency of the proposed converter is even higher, demonstrating its advantages under high-power conditions.

From (Supplementary Figure S18), it is evident that under full load conditions, the switching losses of the low-frequency unit Si-IGBT account for only 4% of the total losses. Device losses are primarily concentrated in conduction losses. On the other hand, the device losses of the high-frequency unit SiC-MOSFET account for only 22% of the total losses.

7 Conclusion

In this article, based on fractional power processing, a "input-parallel and output-series" hybrid three-phase inverter consisting of Si IGBT and SiC MOSFET devices is proposed. The LFPC-C is formed by Si IGBT devices, and it employs SHEPWM modulation along with the HFPC-C to eliminate low-frequency and mid-frequency harmonics. This approach allows Si IGBT to handle the main power with minimal switching losses. The HFPC-C consists of SiC MOSFET devices, enabling it to accurately compensate for the LFPC-C low-frequency harmonics while operating with low switching losses. Three-phase five-column medium-frequency step-down transformer reduces the current flowing through the HFPC-C to approximately half of the inverter's output current, minimizing the current stress on SiC

MOSFET devices. This topology leverages the strong conduction capability of Si IGBT and the low switching losses of SiC MOSFET in high-frequency states to reduce device losses in high power conversion applications. Additionally, the proposed "LFPC-C open-loop, HFPC-C closed-loop" coordinated control method simplifies the control system. The ripple voltage analysis model, based on circuit characteristics, guides the passive component design. Task allocation for filtering and transformer components is determined according to the circuit's requirements for harmonics elimination and compensation. Furthermore, a 7.5 kW experimental prototype is constructed to validate the feasibility of this proposed topology.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material, further inquiries can be directed to the corresponding author.

Author contributions

QY: Writing–original draft, Writing–review and editing. CL: Writing–original draft, Writing–review and editing, Conceptualization, Data curation, Formal Analysis, Funding acquisition, Investigation, Methodology, Project administration, Resources, Software, Supervision, Validation, Visualization. RL: Writing–original draft, Writing–review and editing, Conceptualization, Data curation, Formal Analysis, Funding acquisition, Investigation, Methodology, Project administration, Resources, Software, Supervision, Validation, Visualization. ZP: Writing–original draft, Writing–review and editing, Conceptualization, Data curation, Formal Analysis, Funding acquisition, Investigation, Methodology, Project administration, Resources, Software, Supervision, Validation, Visualization. DG: Writing–original draft, Writing–review and editing, Conceptualization, Data curation, Formal Analysis, Funding acquisition, Investigation, Methodology, Project administration, Resources, Software, Supervision, Validation, Visualization. TM: Conceptualization, Data curation, Formal Analysis, Funding acquisition, Investigation, Methodology, Project administration, Resources, Software, Supervision, Validation, Visualization, Writing–original draft, Writing–review and editing. XS: Writing–original draft, Writing–review and editing, Conceptualization, Data curation, Formal Analysis, Funding acquisition, Investigation, Methodology, Project administration, Resources, Software, Supervision, Validation, Visualization.

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Conflict of interest

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Supplementary material

The Supplementary Material for this article can be found online at: https://www.frontiersin.org/articles/10.3389/fenrg.2024.1375888/full#supplementary-material

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