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Innovative model predictive control for HVDC: circulating current mitigation and fault resilience in Modular Multilevel converters

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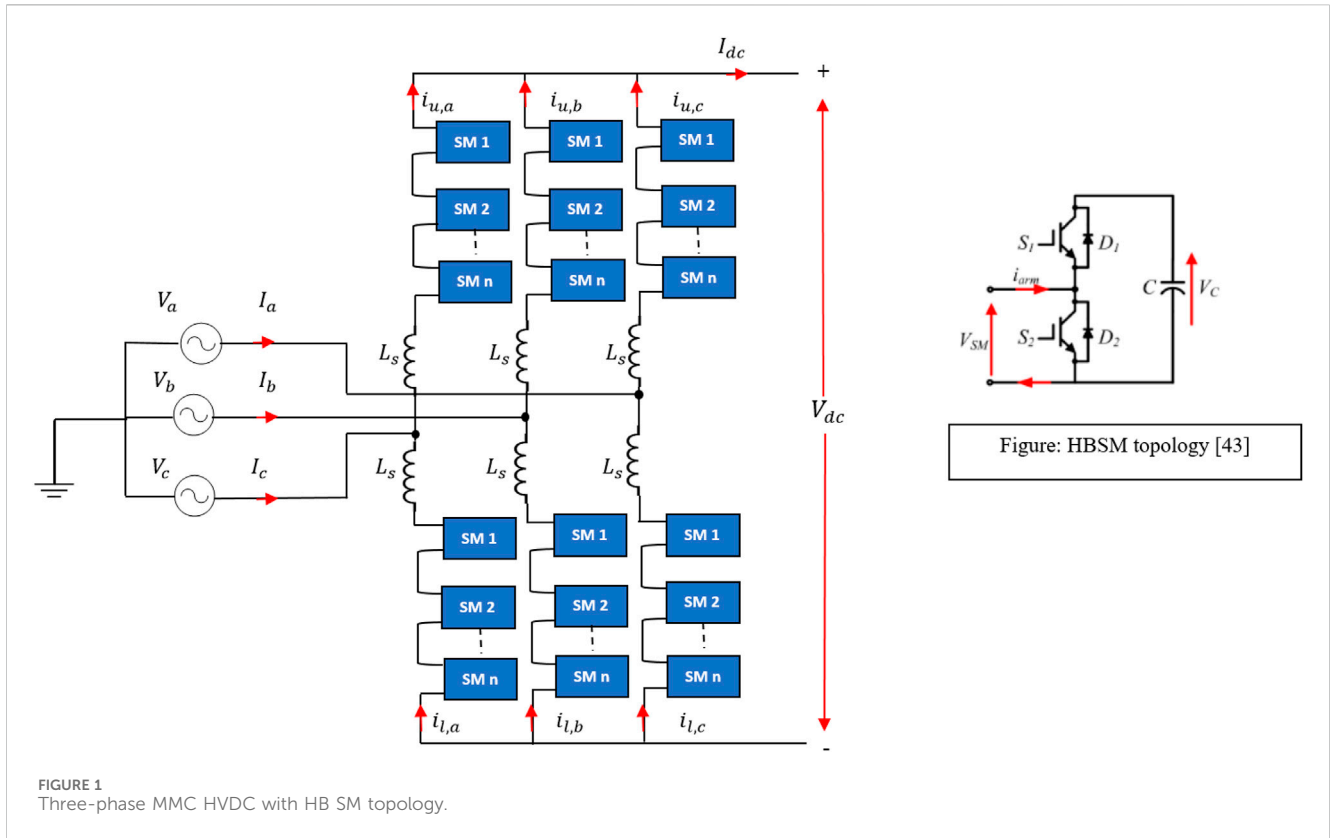
This study presents an advanced Model Predictive Control (MPC) technique designed to mitigate Circulating Current (CC) in HVDC systems equipped with Modular Multilevel Converters (MMC). This MPC strategy eliminates the need for traditional PI regulators and pulse width modulation, improving system dynamics and control accuracy. It excels in managing output currents and mitigating voltage fluctuations in sub-module capacitors. Moreover, the paper introduces a novel communication-free Fault Ride-Through (FRT) method that makes a DC chopper redundant, enabling rapid recovery from disturbances. To reduce the computational burden of standard MPC algorithms, an aggregated MMC model is proposed, significantly decreasing the computational complexity. Simulation studies validate the new MPC algorithm's capability in regulating AC side current, reducing CC, and ensuring capacitor voltage stability under varying conditions. The findings indicate that the proposed MPC controller outperforms traditional PI and PR-based methods, offering enhanced dynamic response, decreased steady-state error, and lowered converter losses, which contribute to smoother DC link voltages. Future research will focus on system scalability, renewable energy integration, and empirical validation through hardware-in-the-loop testing.

KEYWORDS

Modular Multilevel converter, HVDC, CC suppression schemes, capacitor voltage, Model Predictive Control (MPC)

1 Introduction

An alternative system was required due to the rising demand for safe and dependable energy transmission, as well as the limitations of AC systems in bulk power transfer. Owing to the rapid advancement of electronic devices, DC systems have proven to be a viable alternative. Since then, numerous projects have been developed, and some are currently under construction. The expansion of HVDC initiatives has opened the doors to the potential creation of expansive HVDC networks, often termed as HVDC super-grids,



linking multiple HVDC infrastructures (Gomis-Bellmunt et al., 2019; Raju et al., 2019; Ansari et al., 2020). These continental-scale super-grids are seen as a vision of the future, with expectations of becoming a reality in the span of the next decade and a half (Soomro et al., 2022).

Converters in HVDC systems transform AC into DC. The two main types of converter configurations are voltage source converters (VSCs) and line-commutated converters (LCC). LCC-based HVDC transmission has been in operation for a long time and is considered a mature technology. The primary drawback of LCC is that it cannot be used in isolated systems and requires additional reactive power to switch the semiconductors (Heath et al., 2021; Jiang et al., 2023). The drawbacks of LCC were overcome by VSCs. Since VSC technology uses IGBTs rather than thyristors. A VSC-based HVDC system provides independent control of active and reactive power and allows for bidirectional power flow (Soomro et al., 2021). Among VSCs, researchers have devoted significant attention to the Modular Multilevel Converter (MMC), as shown in Figure 1, due to its advantages, such as modularity, scalability, increased efficiency, decreased total harmonic distortion (THD), and fault-blocking capacity (Ali et al., 2020; Jia et al., 2023; Shi et al., 2023). The leading manufacturers of MMC technology include Siemens, EPRI, ALSTOM, and ABB, representing the latest generation of VSCs.

AC faults, both symmetrical and asymmetrical, on the grid side of an MMC-HVDC system can lead to disruptions in the DC link, primarily due to disparities in power flow between the sending and receiving converters (Ye et al., 2021; Chandio et al., 2023). These discrepancies can compromise the efficiency and stability of the MMC-HVDC setup. Current standards for the electrical grid stipulate that power delivery to consumers must remain stable

and consistent, even in the event of various AC faults (Zhou et al., 2019; Jiang et al., 2020; Ye et al., 2021; Zhou et al., 2022b). Therefore, there is a significant need for the development of an autonomous and resilient AC FRT strategy that maintains steady DC link voltages without ripples. In addition to stabilizing the DC link voltage, a robust AC FRT strategy ensures that internal dynamics, such as CC and capacitor voltage ripple, remain within safe limits during and after fault conditions.

Within MMC, unregulated CC may result in a range of adverse outcomes such as increased power losses, overheating of components, instability in voltage, harmonic interference, and a decrease in the reliability of the entire system (Kadandani et al., 2021; Huang et al., 2022; Li et al., 2022; Priya and Ponnambalam, 2022; Zhang et al., 2023). An examination of existing research underscores the necessity for comprehensive control approaches that effectively mitigate CC and concurrently address capacitor voltage ripple concerns.

2 Comparison with previous research

The study of transient behaviors in HVDC systems under a variety of AC and DC fault conditions remains a vibrant field of investigation (Silva et al., 2014; Song et al., 2021; Wu et al., 2021). A HVDC system is deemed robust when it possesses the ability to handle AC FRT and maintains control over its internal dynamics. Current research on HVDC systems primarily focuses on DC voltage stability (Li et al., 2021; Shadlu, 2022). Protection against DC side faults has always been a major concern. Conversely, for AC faults, various researchers have proposed different control schemes.

The impetus for addressing these challenges is the stringent requirement of FRT capabilities for the safe operation of the grid during faults, aiming to minimize power outages. During symmetrical and asymmetrical faults, overvoltage on the DC side may cause serious damage to DC cables. In such conditions, imbalances in DC voltage and power can be corrected through rapid control measures. To maintain DC bus voltage and power flow in HVDC systems during faults, various strategies have been suggested in the literature; however, they require additional circuit components (Bahrani et al., 2015; Luo et al., 2019).

The primary issue with MMC-HVDC transmission systems is that both their active power transfer and reactive power generation capabilities are significantly reduced when the AC voltage at the point of common coupling drops during a major on one of the AC sides. This leads to an imbalance between the DC and AC sides; specifically, the power on the DC side may exceed the actual active power that can be transferred to the AC side. As a result, the DC link voltage rises due to the energy trapped on the DC side being absorbed by the DC link capacitors, thereby increasing the voltage stress on the converter switches and the coupling transformer. To counter the effects of this trapped energy and to prevent damage to the DC link capacitors and converter switches from over-voltage, HVDC systems employ DC Choppers (Li et al., 2019; Qi et al., 2021; Zhou et al., 2022a; Liu et al., 2022; Wang et al., 2022; Jia et al., 2023). Control methods to mitigate transient voltage dips (AC FRT) for HVDC systems based on MMC were proposed in (Hoehn et al., 2019; Muhammad et al., 2022). The objective in the event of a grid dip was to utilize the internal energy stored in MMC to continuously power passive loads. However, these studies were limited to testing voltage sag faults; other fault conditions, such as symmetrical and asymmetrical faults, were not evaluated for system stability. Moreover, issues with CC and capacitor voltage ripple were not addressed. This same FRT methodology has been adapted for MTDC systems in (Ansari et al., 2022). A significant drawback of the FRT proposed in (Hoehn et al., 2019; Ansari et al., 2022; Muhammad et al., 2022) is the requirement for larger capacitors, which increases the overall cost and weight of the converter station. Some proposed FRT mechanisms, designed to connect AC grids, depend on communication links. For instance, the research in (Adam et al., 2010) revealed that the active power target for the slave terminal is determined by the Point of Common Coupling (PCC) voltages measured at both ends of the DC link. Thus, should there be an AC fault on either side of the DC link, the active power reference is correspondingly diminished. Although the use of a communication link can enhance DC voltage control, it also introduces extra expenses and the potential for communication disruptions.

A variety of strategies to quell CC and address capacitor voltage ripple concerns have been introduced by scholars. Nonetheless, much of this research is narrowly centered on individual MMC units rather than on the MMC-HVDC system as a whole. For instance, strategies like Reduced Switching Frequency have been suggested for capacitor voltage ripple reduction and CC mitigation in (Tu et al., 2011). Techniques for mitigating CC in MMC using a Dual Synchronous Reference Frame (DSRF) were explored in (Samajdar and Tanmoy, 2022). In (Uddin et al., 2019), a Sliding Mode Control tactic employing a second-order super-twisting algorithm was introduced for CC mitigation, indicating that SMC

has a quicker response compared to the PR controller. Moreover, a backstepping controller for regulating CC and stabilizing leg voltages was employed in (DinWaqar et al., 2019). Despite these advancements, the research presents notable shortcomings. In particular, the absence of an integrated MMC-HVDC system approach and a thorough assessment of how robust the proposed control strategies are across various AC fault scenarios might restrict the practicality and efficacy of these methods in real-world, variable conditions.

In the event of asymmetrical fault such as L-G fault, managing sub-module (SM) capacitor voltage ripple and suppressing CC becomes notably more complex. During an asymmetrical AC fault, both capacitor voltage ripple and CC can become substantial, potentially surpassing established safety thresholds, which may trigger converter tripping and result in stability issues. A series of studies (Wang et al., 2018; Wang et al., 2020a; Wang et al., 2020b; Wang et al., 2021) have introduced techniques for controlling internal dynamics within MMC models, addressing concerns like capacitor voltage ripple and CC in scenarios involving unbalanced grids to ensure their operation remains within acceptable limits. However, while these existing studies have primarily focused on mitigating CC and minimizing capacitor voltage ripple issues during unbalanced AC (asymmetrical) faults, they have fallen short in a critical aspect: the evaluation of the resilience of their proposed control strategies across various AC fault scenarios, encompassing both symmetrical and asymmetrical faults. This research gap could restrict the adaptability of these strategies to a wide range of real-world situations.

The Adaptive Proportional Integral (API) controller is suitable for applications where adaptability and parameter tuning are important. It is useful in systems with moderate complexity and varying operating conditions (Ishfaq et al., 2019). However, API controllers may face challenges in highly non-linear and uncertain systems such as MMC-HVDC. Integral Back Stepping (IBS) controllers are ideal for applications that require robustness against parameter variations and uncertainties. They can be used in complex MMC-HVDC systems with a high degree of nonlinearity. However, IBS requires a more complex design process compared to MPC and Sliding Mode Controller (SMC). In the case of MMC-HVDC systems, the dynamics can be highly nonlinear, and designing an IBS controller may involve intricate mathematical derivations and multiple backstepping steps, making it harder to implement (DinWaqar et al., 2019).

The choice between SMC and MPC for suppressing circulating currents in MMC-HVDC systems should be based on a careful analysis of the application's requirements and constraints. While MPC offers optimal control and adaptability, SMC provides robustness and fast response. Depending on the specific needs and priorities of the application, either control strategy could be suitable for effectively suppressing circulating currents and ensuring the stability and performance of MMC-HVDC systems.

In this research paper, we introduce a control strategy based on MPC that addresses both CC suppression and the mitigation of capacitor voltage ripple. Utilizing MATLAB/Simulink for simulation, the research demonstrates that the MPC-based controller introduced here outperforms traditional PI and PR approaches in managing CC. It exhibits a faster dynamic response, minimizes steady-state discrepancies, and effectively

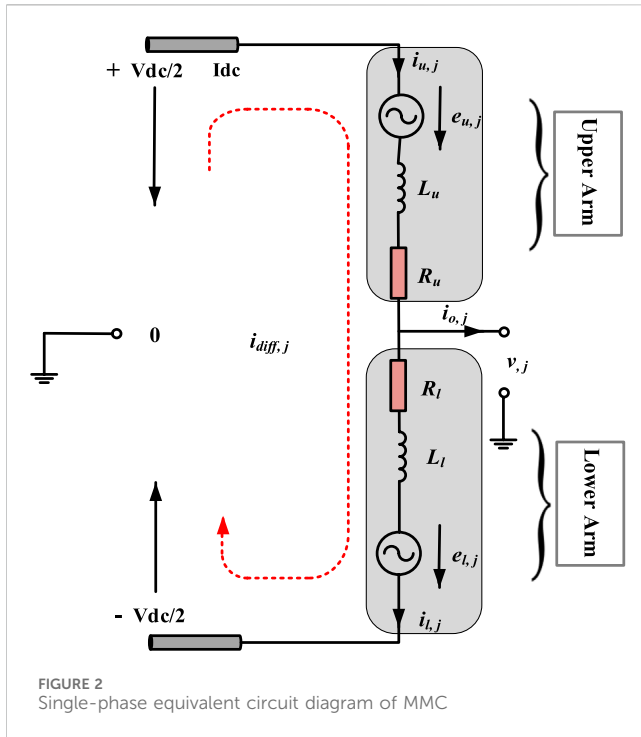


FIGURE 2 Single-phase equivalent circuit diagram of MMC

reduces conversion losses. Additionally, the method maintains consistent capacitor voltages throughout the MMC's various arms, ensuring exceptional functionality even when system faults occur, thus preserving converter stability. This research also presents an improved FRT strategy that functions independently of a DC chopper and does not depend on communication links for operation. This suggested FRT approach enables rapid fault recovery and effectively keeps DC link and capacitor voltages within safe limits. Moreover, the conventional MPC algorithm demands the evaluation of all potential switching states within each control interval, a process that is both laborious and time-intensive. For instance, in the case of having $N = 10$ submodule modules (SMs), the number of combinations is determined by the Binomial Coefficient $3C_{2N}^N = 554268$, with each phase having $C_{2N}^N = 184756$ possible combinations. Consequently, employing traditional MPC remains impractical, even with state-of-the-art microprocessors. Nonetheless, the manuscript presents an aggregated model of the MMC which negates the requirement for voltage sorting among capacitors, thereby considerably decreasing the count of anticipated states, the hardware needs for sorting, and the computational intricacy.

3 Proposed MPC for MMC-HVDC system

The phase equivalent circuit depicted in Figure 2 lays the groundwork for the mathematical modeling of the MMC. The different currents flowing through the MMC are described as follows:

$$i_{u,j} = i_{diff,j} + \frac{i_{o,j}}{2} \quad (1)$$

$$i_{l,j} = i_{diff,j} - \frac{i_{o,j}}{2} \quad (2)$$

$$i_{o,j} = i_{u,j} - i_{l,j} \quad (3)$$

$$i_{diff,j} = \frac{1}{2}(i_{u,j} - i_{l,j}) \quad (4)$$

The CC, as defined in Eq 5, consists of a direct current component along with various harmonic components. In this representation, the current flowing through the upper arm is indicated by $i_{u,j}$, while $i_{l,j}$ signifies the current in the lower arm. The symbol $i_{o,j}$ is used to denote the output current.

$$i_{diff,j} = \frac{i_{dc,j}}{3} + i_{ch,j} \quad (5)$$

MPC has emerged as a prominent advanced control strategy in the context of HVDC MMC operations. This method is distinguished by its predictive nature, employing a model of the system to anticipate future trends of the variables under control. Utilizing these projections, the controller determines the most favorable gate signals for the MMC switches to ensure they function under optimal conditions. Figure 3 provides an in-depth view of the control block diagram for the proposed MPC method applied to an MMC-HVDC system. The primary aims of the MPC include maintaining the AC current within desired parameters and minimizing the CC. The algorithm attains these goals through a sequence of tasks, which include forecasting the behavior of controlled variables across the spectrum of potential switching states, evaluating the associated cost function for each of these predictions, and ultimately selecting the switching state that leads to the lowest-cost function.

The cost function evaluates every anticipated state during the control interval, identifying the most favorable switching states to minimize the cost. The algorithm's cost function is constructed as illustrated in Eq 6. Typically, MPC method incorporates weighting factors to amalgamate various subsets of the cost function into a single cost function.

$$k_m = \lambda_1 K_1 + \lambda_2 K_2 \quad (6)$$

The aim of tracking the AC current is to keep the AC current of the Modular Multilevel Converter (MMC) aligned with a predetermined reference value. The cost function for the AC current tracking is delineated as follows.

$$K_1 = |i_{kref}(t + T_s) - i_k(t + T_s)| \quad (7)$$

A further crucial goal of the MPC is to limit the CC to its reference value to enhance the system's efficiency. The formula for the CC, along with the cost function pertaining to it, has been formulated in the study (Soomro et al., 2023) and is expressed in Eqs 8, 9, respectively.

$$i_{kdiff}(t + T_s) = \frac{T_s}{2L'} [V_{dc} - u_{kn}(t + T_s) - u_{kp}(t + T_s)] + i_{kdiff}(t) \quad (8)$$

$$K_2 = |i_{kdiff-ref}(t + T_s) - i_{kdiff}(t + T_s)| \quad (9)$$

The subsets of the cost function, denoted as K_1 and K_2 , are determined by applying Eqs 7, 9. Following this, the algorithm computes the cost function K_m for each potential switching state, opting for the state that yields the lowest K_m . The selected switching

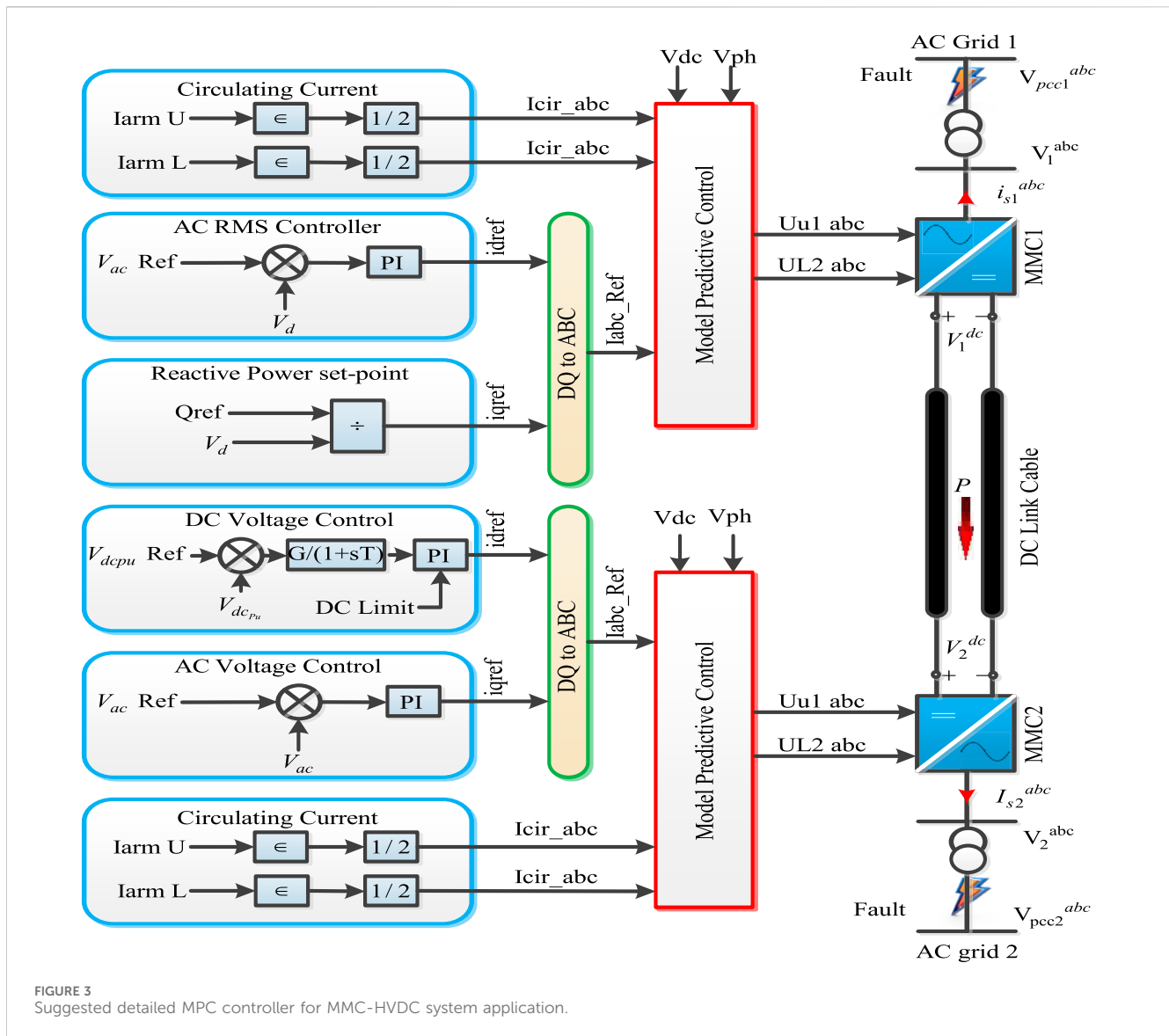


TABLE 1 Specifications for the suggested model predictive control-enabled MMC-HVDC system.

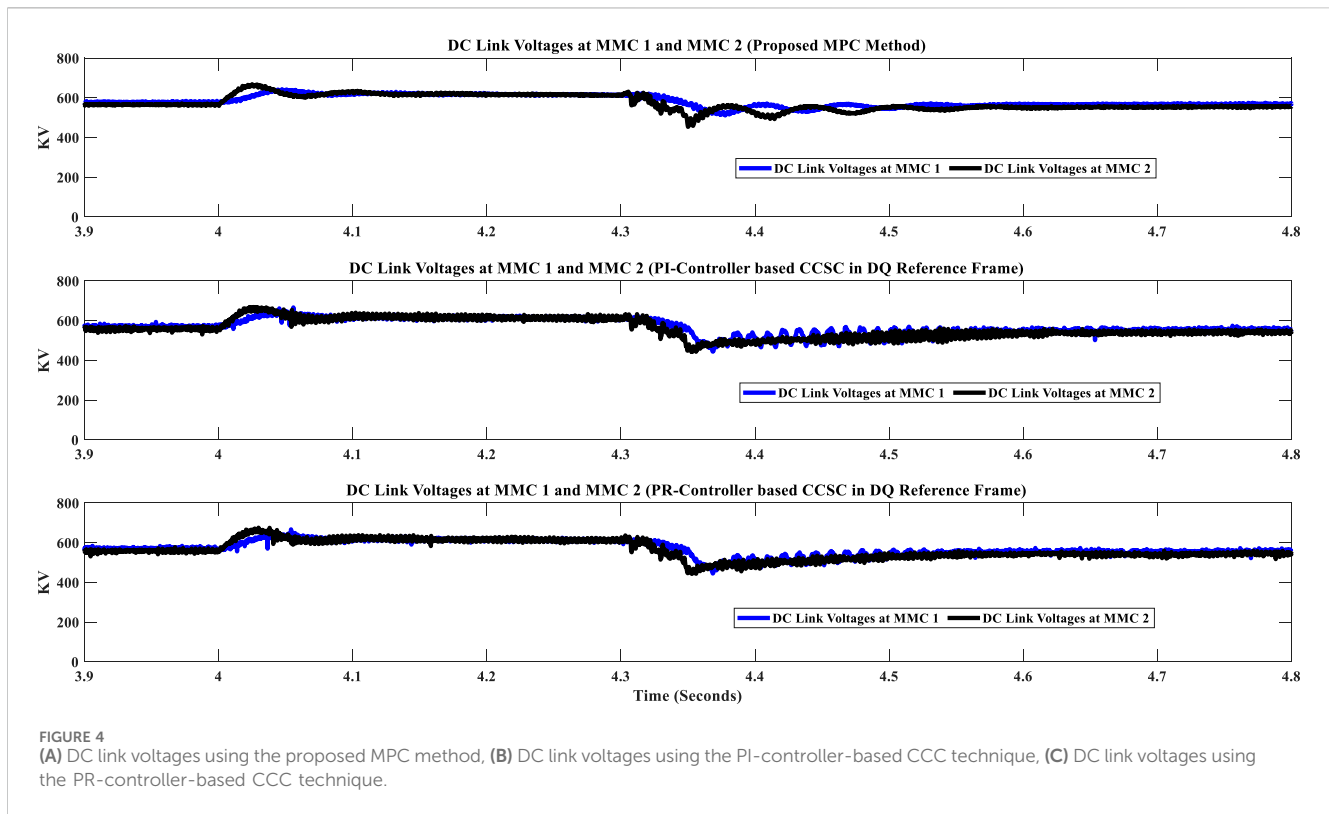
Specifications	Measurement
Rated Power of MMC	950 MVA
Operational AC voltage for MMC	370 kV
Set point for Active Power	850 MW
Nominal DC voltage	580 kV
Inductance per arm	50 mH
Count of sub modules per arm	76
Voltage ratio of MMC transformer	370 kV/230 kV
Standard Frequency	50 Hz
Peak DC voltage rating	1.1 PU
Minimum permissible DC voltage	0.7 PU

states are then implemented on the Sub modules, and as a result, the algorithm consistently monitors the AC current and restricts the CC. Table 1 lists the parameters for the proposed system under consideration.

4 Results discussions

A proficient FRT strategy should effectively manage a variety of fault conditions. To evaluate the effectiveness of the suggested strategy, it considers different fault categories such as three-phase to ground (LLL-G), single line-to-ground (SLG) faults, line-to-line (LL), and double-line-to-ground (LLG) faults. Nevertheless, the scope of this document is restricted and cannot encompass every conceivable scenario. Therefore, this portion of the paper will detail an exhaustive examination of two specific fault scenarios.

- In Scenario 1, a three-phase to ground (LLL-G) fault takes place in AC grid 2, initiating at 4 s and being rectified by 4.3 s.



- Scenario two presents a single line-to-ground (SL-G) fault in AC grid 1, beginning at 3 s and concluding at 4.3 s.

4.1 Outcomes from simulations of scenario one employing the suggested MPC-based MMC for HVDC transmission

To assess the performance of the suggested FRT technique, a symmetrical LLL-G fault is executed on the AC side of the MMC converter station 2. This section presents the simulation findings for both converter stations. The duration of the fault spans a total of 0.3 s, beginning at $t = 4$ s and anticipated to be resolved by $t = 4.3$ s. The efficacy of the FRT mechanisms is dependent on the pre-fault direction of power transmission through the HVDC link. For this scenario, we posit that the positive direction of power is from MMC station one to MMC station 2. When a fault occurs in AC grid two and the pre-fault power flow is positive, the resulting surplus power in the DC link may lead to DC overvoltage. Figure 4 presents the simulation outcomes for DC link voltages at the terminals of both Modular Multilevel Converters (MMCs) using the proposed MPC approach, alongside a comparative analysis with conventional Proportional-Integral (PI) and Proportional-Resonant (PR) controllers in their CC suppression capabilities (CCC). The MPC-based CCC demonstrates a stabilization effect on the DC link voltages, which is evident in Figure 3A. This method achieves a reduction in ripple components within the DC link voltages at MMC one and MMC two without the necessity for an auxiliary controller. In contrast, Figure 4B, C) reveal that the CCC techniques utilizing PI and PR controllers fail to adequately

mitigate CC, leading to noticeable fluctuations in the DC link voltages.

Figure 5C illustrates that during the fault interval, the phase voltages at terminal 2, linked to MMC 2, plummet to zero. In contrast, as depicted in Figure 5B, the phase voltages at MMC 1, which is associated with AC grid 1, remain largely unaffected, even in the event of a fault at AC Grid 2, serviced by MMC 2. The power output of MMC two is observed to fall to zero concurrent with the voltage drop at terminal 2. The AC FRT strategy proposed here demonstrates robust performance, quickly reducing the output power of MMC one to zero upon detecting the maximum DC voltage threshold, as presented in Figure 5A. Throughout the entire fault duration, the phase voltages connected to MMC two drop to zero, and Figure 5E illustrates that the MMC 2 converter station contributes minimal current to the fault. Consequently, the proposed AC FRT strategy effectively minimizes di/dt stress on the power semiconductor devices. Furthermore, Figure 5D reveals that during the entire fault, MMC1 station promptly reduces its current output to zero, preventing power imbalances and DC overvoltage. In addition, a closer examination of the Figure 5 demonstrates that the power quality and total harmonic distortion (THD) of phase voltages and AC side currents for both MMC one and MMC two align with IEEE standards, showcasing improved performance.

The proposed MPC method not only achieves optimized AC FRT capabilities but also addresses CC and capacitor voltage ripple challenges. The implemented CCC strategy effectively diminishes the CC intensity as evidenced in Figure 6A. The differential current registers at 0.5 per unit (PU), staying below the 10% threshold of the nominal current as stipulated by grid regulations. The efficacy of this

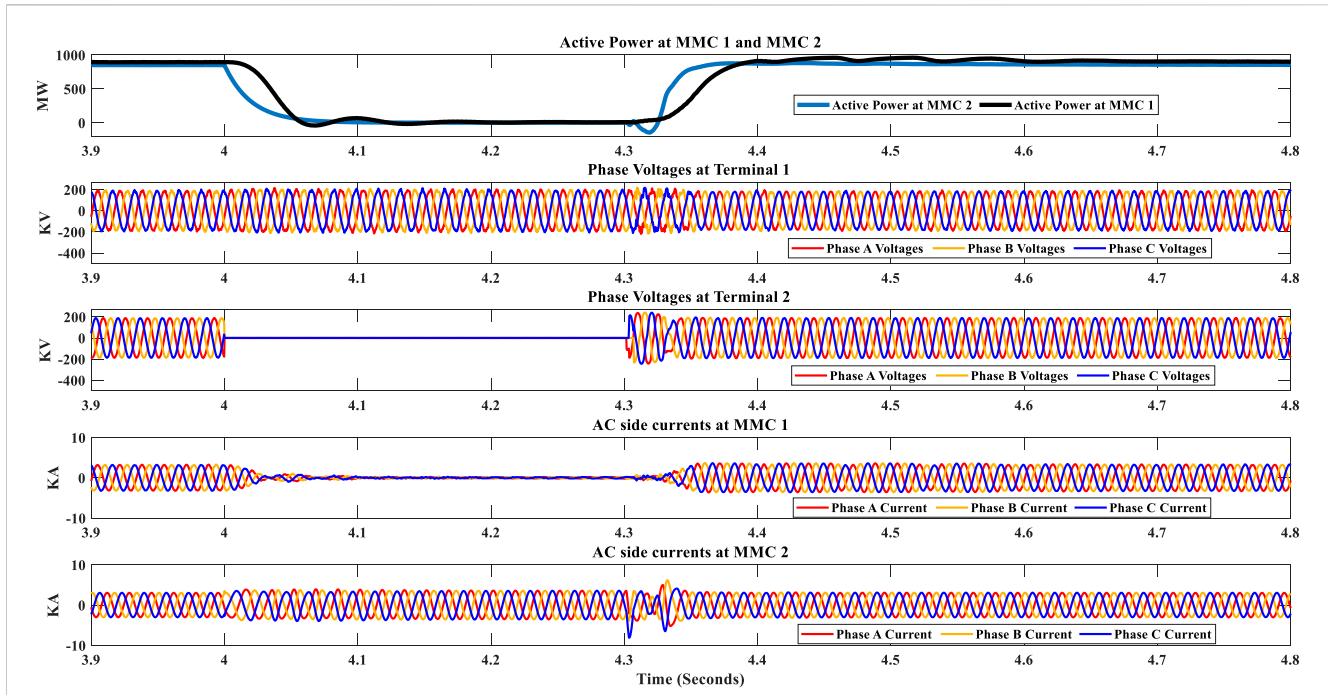


FIGURE 5 (A) Active Power, (B) Phase Voltages at Terminal 1 (C) Phase voltages at Terminal 2 (D) Currents on the AC side of MMC one (E) Currents on the AC side of MMC two.

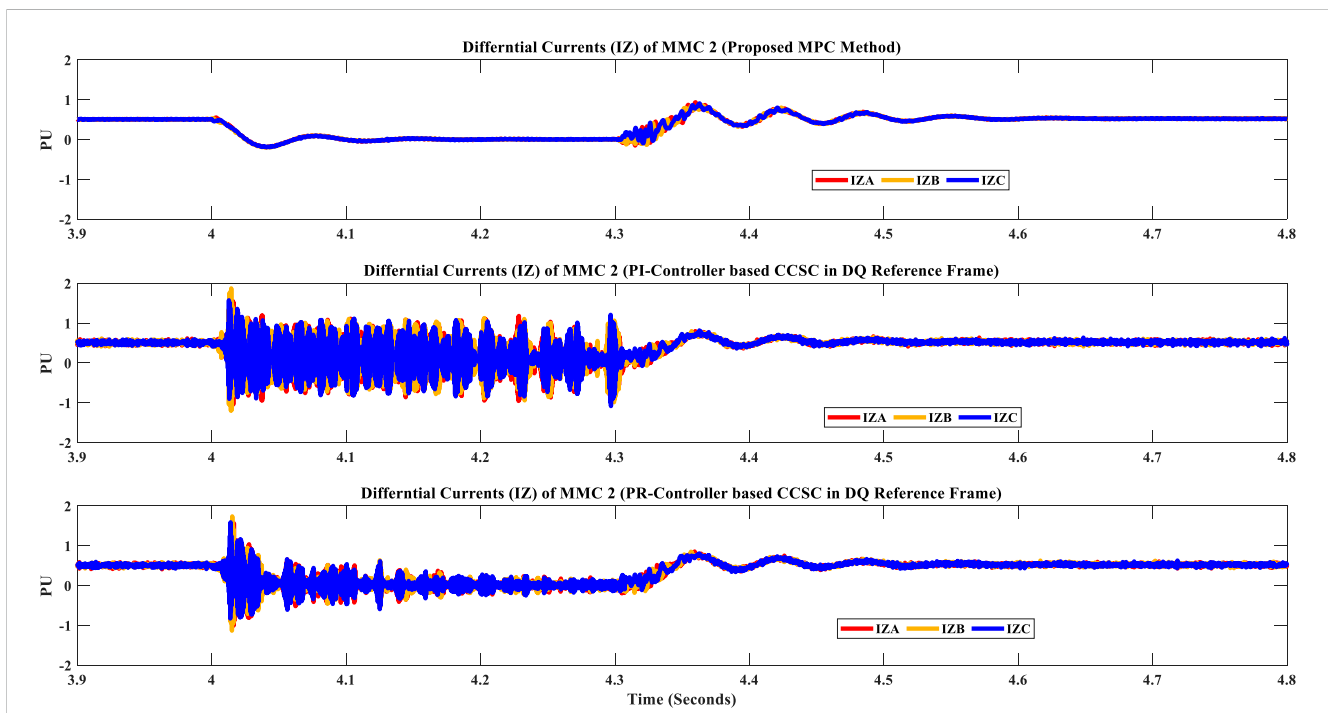
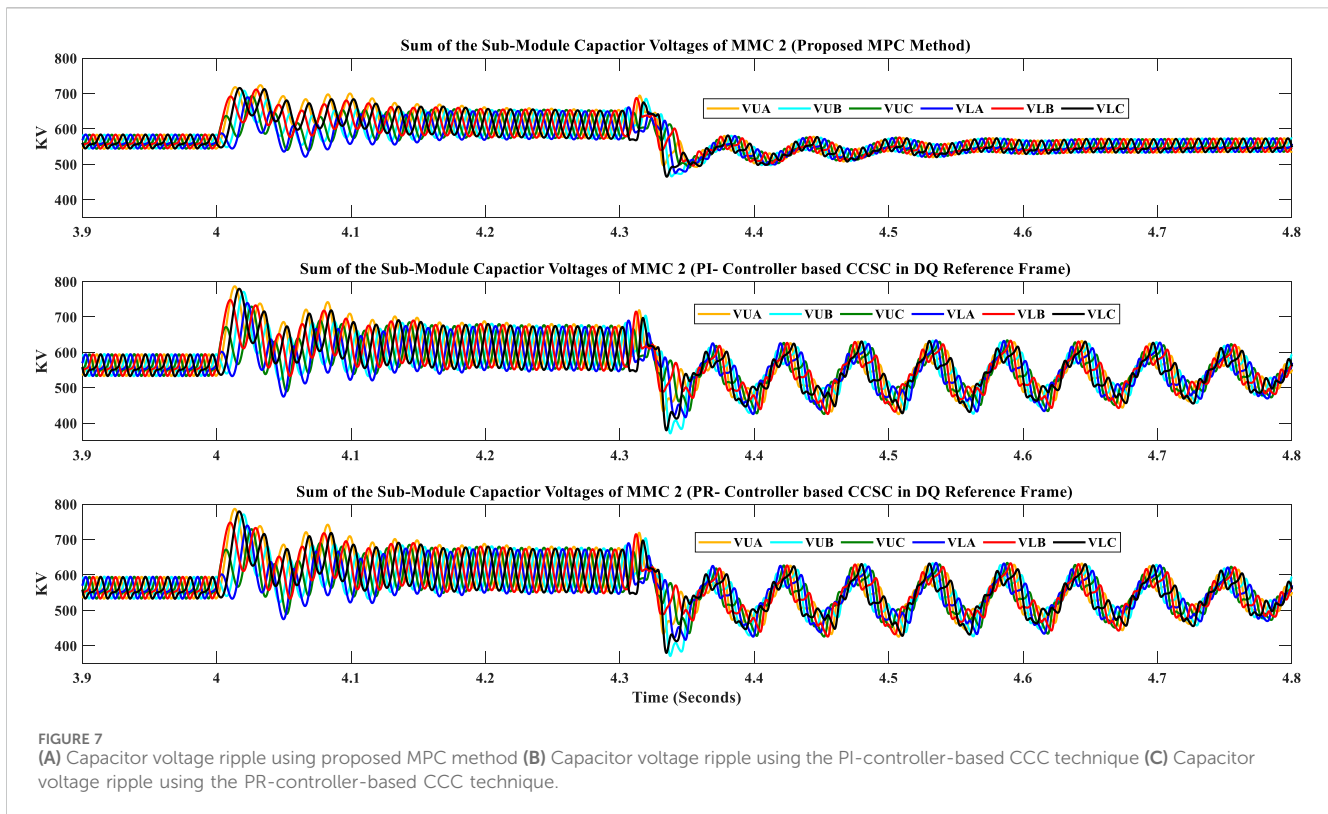


FIGURE 6 (A) Differential Currents using proposed MPC method (B) Differential current using the PI-controller-based CCC technique (C) Differential current using the PR-controller-based CCC technique.

MPC based controller is benchmarked against the traditional PI and PR CCC techniques through simulations, showcasing superior performance in terms of faster dynamic reactions and minimized

steady-state deviations. The advantages of the proposed MPC approach are not just confined to faster response times but also sustained in steady-state operation. The CC values under the



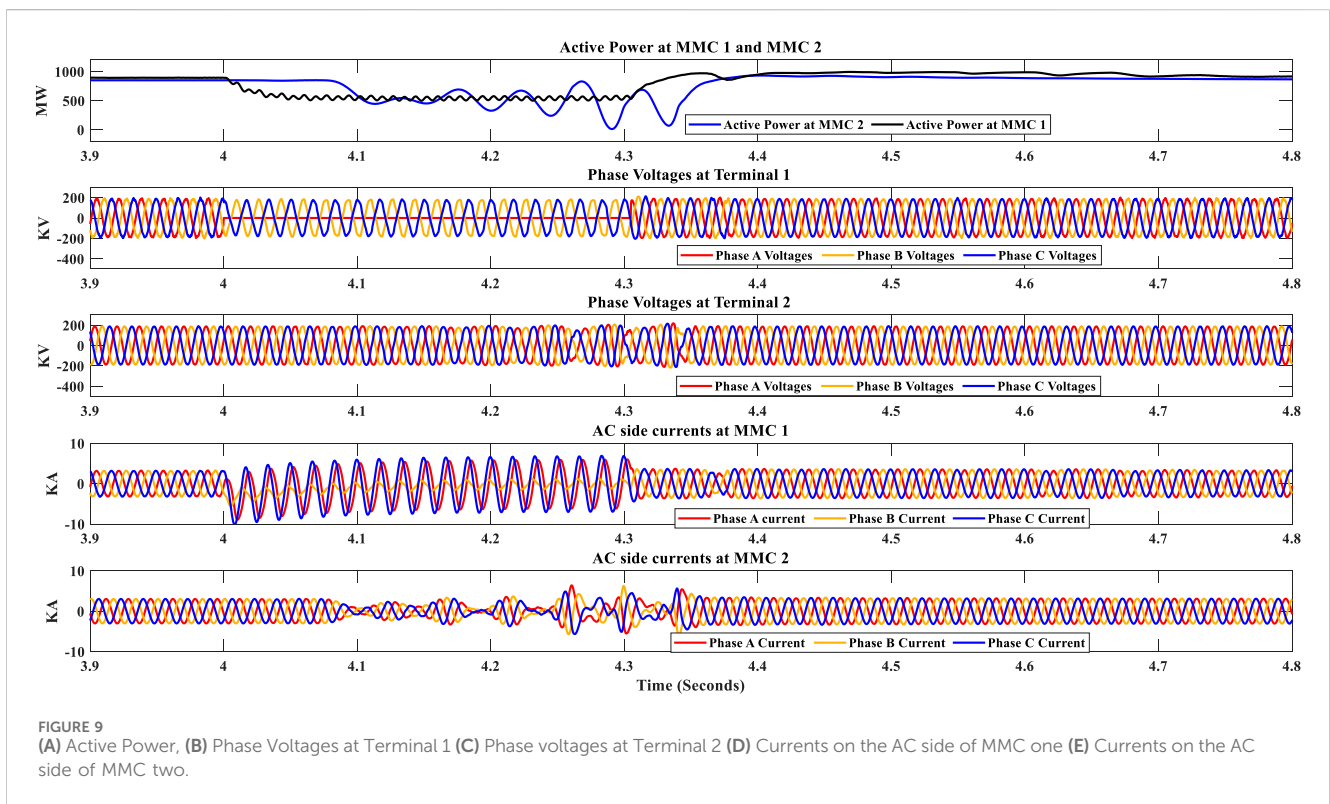
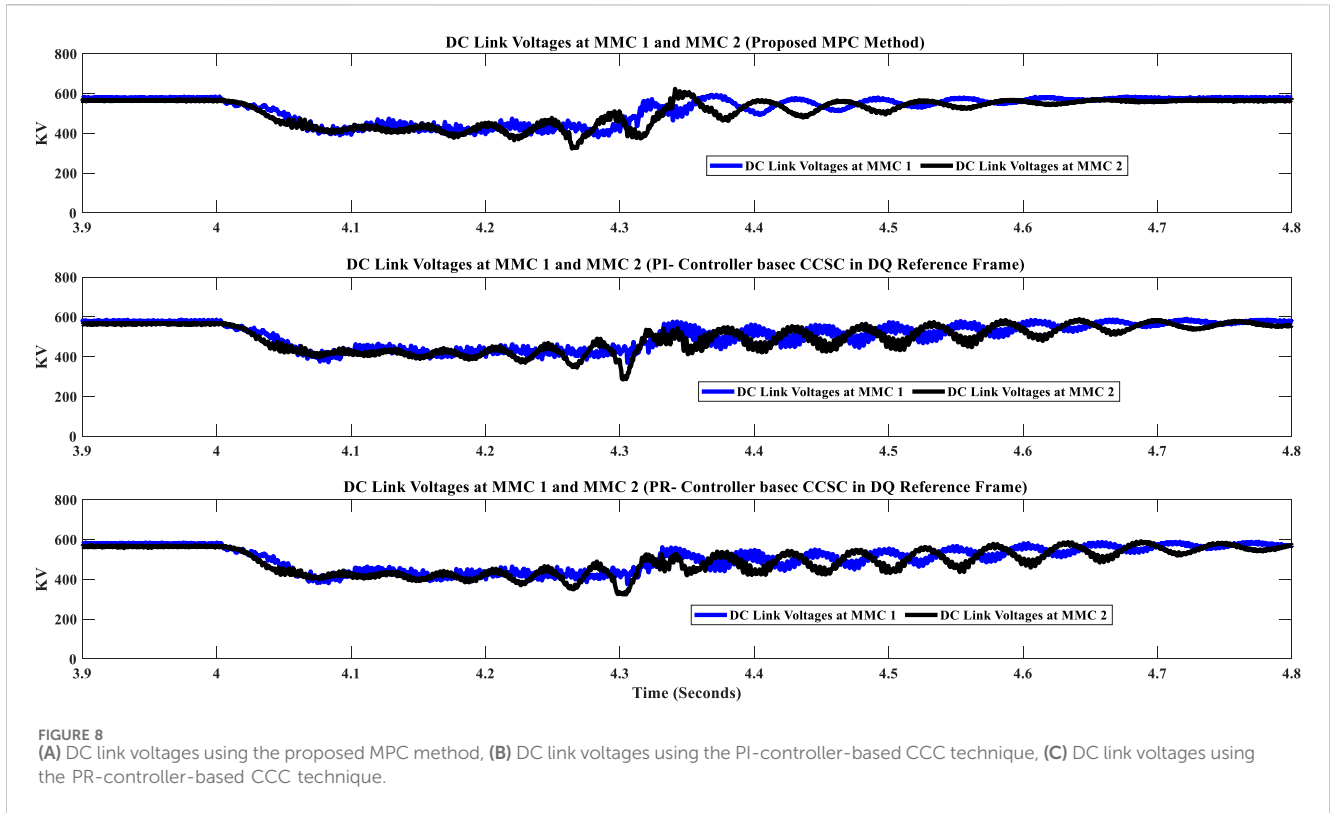
proposed MPC method align precisely with the target value, unlike the PI and PR methods, which do not fully suppress the second harmonic current as shown in Figure 6B, C. This inefficiency in the traditional methods leads to increased losses and strains on converter components. In summary, Figure 6 unequivocally illustrates the superiority of the proposed MPC method over the PI and PR methods, especially under fault conditions. Whereas the latter methods exhibit a compromised performance during faults—where the differential current spikes to 1.9 PU when a fault is introduced at the 4-s mark—the new method maintains better control, underscoring its enhanced efficiency in managing CC.

Figure 7A illustrates that the proposed technique effectively curtails CC while simultaneously resolving capacitor voltage ripple concerns. Throughout the occurrence of a fault, the MMCs’ capacitor voltage ripple remains within designated safety margins, averting any potential for converter shutdowns. In addition, capacitor voltages maintain equilibrium with a noticeable reduction in capacitor voltage ripple both during and subsequent to the fault event. In contrast, Figure 7B, C depict the behavior of capacitor voltages under the control of PI and PR-based CCC controllers. These traditional CCC approaches prioritize the mitigation of circulating but do not adequately address capacitor voltage ripple reduction. As a result, the voltage ripple across capacitors under these methods exhibits comparably higher magnitudes. The methodology put forth in this paper, as opposed to the PI and PR-based strategies, guarantees that the voltage across capacitors in both the upper and lower arms of the MMC remains consistently well-managed, as can be seen in Figure 7.

4.2 Outcomes from simulations of scenario two employing the suggested MPC-based MMC for HVDC transmission

Building on the parameters set in scenario 1, we operate under the presumption that MMC one is the origin of positive power flow towards MMC 2. The resilience of the advanced HVDC system is evaluated here by introducing an SLG fault at AC Grid 1. In the event of Grid one failing, and with pre-fault power flow being positive, the result is a drop in DC link voltage due to insufficient power, leading to under-voltage conditions. The simulation outcomes pertaining to the DC link voltages at the MMC one and MMC two stations are presented in Figure 8. Post-fault, the DC link voltages at both MMC stations remain closely aligned with the target values with minimal variance, as Figure 8A demonstrates. This highlights the effectiveness of the newly suggested MPC approach. Conversely, the PI and PR-based control methods exhibit significant deviations, and the DC link voltages present notable irregularities, indicating a less effective suppression of CC with the conventional PI and PR-based CCC strategies.

Within a HVDC setup, an SLG fault precipitates a voltage dip at the AC side of the MMC, leading to an immediate decline in the MMC’s capacity to transfer power, as depicted in Figure 9A. The devised FRT methodology is crucial to synchronize the operations of both MMC terminals to safeguard against SM capacitor overvoltage and to maintain power equilibrium post-SLG fault. The system’s stability during FRT is hinged on its ability to emulate the pre-fault active power levels closely. As evidenced in Figure 9B, Phase A’s voltage, which is linked to MMC 1, drops to zero at the fault’s peak, causing a marginal increase in the AC currents of MMC 1, as indicated in Figure 9D. Meanwhile, the phase voltages tied to MMC two experience minimal disruption, highlighted in Figure 9C. Figure 9E reveals that the AC



currents for MMC one and MMC two remain within acceptable ranges amid the fault, and they promptly return to their intended magnitudes once the fault is resolved. Post-fault, the phase voltages and AC currents

for both MMC stations are observed to be sinusoidal, with diminished THD, aligning with established grid codes—this is particularly noticeable in Figure 9.

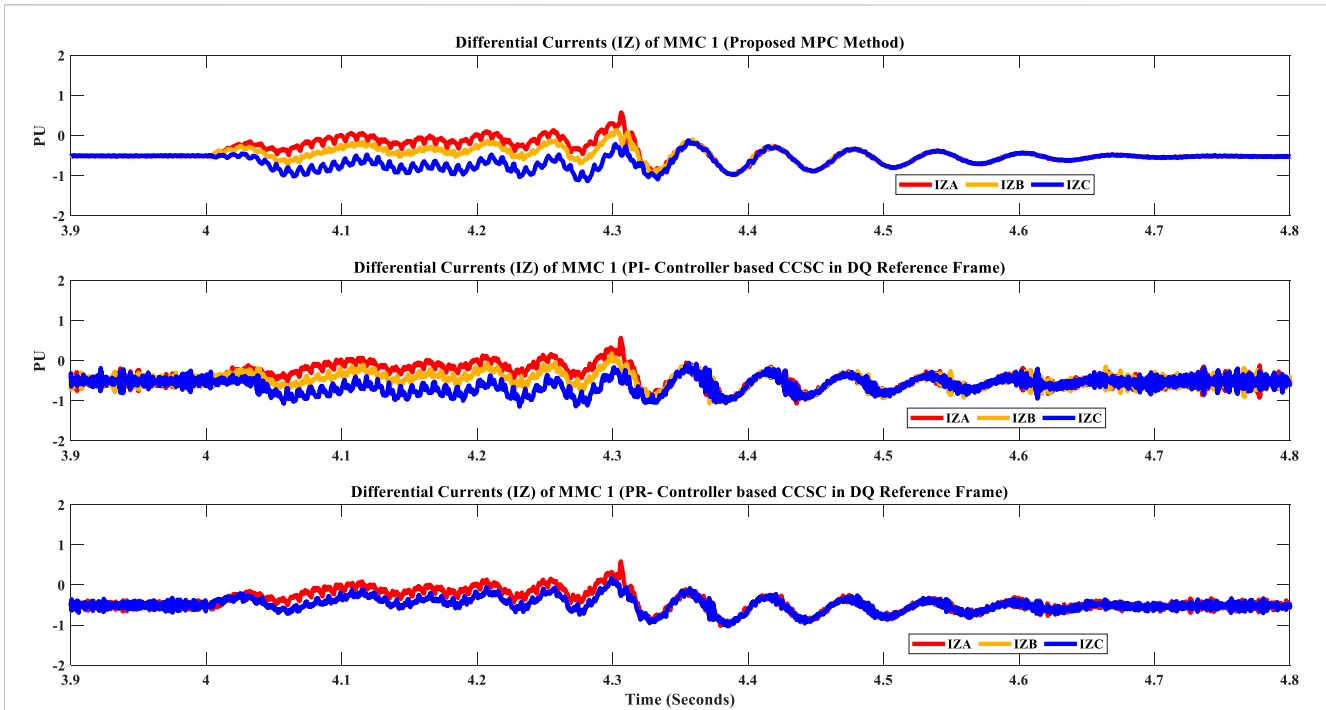


FIGURE 10 (A) Capacitor voltage ripple using proposed MPC method (B) Capacitor voltage ripple using the PI-controller-based CCC technique (C) Capacitor voltage ripple using the PR-controller-based CCC technique.

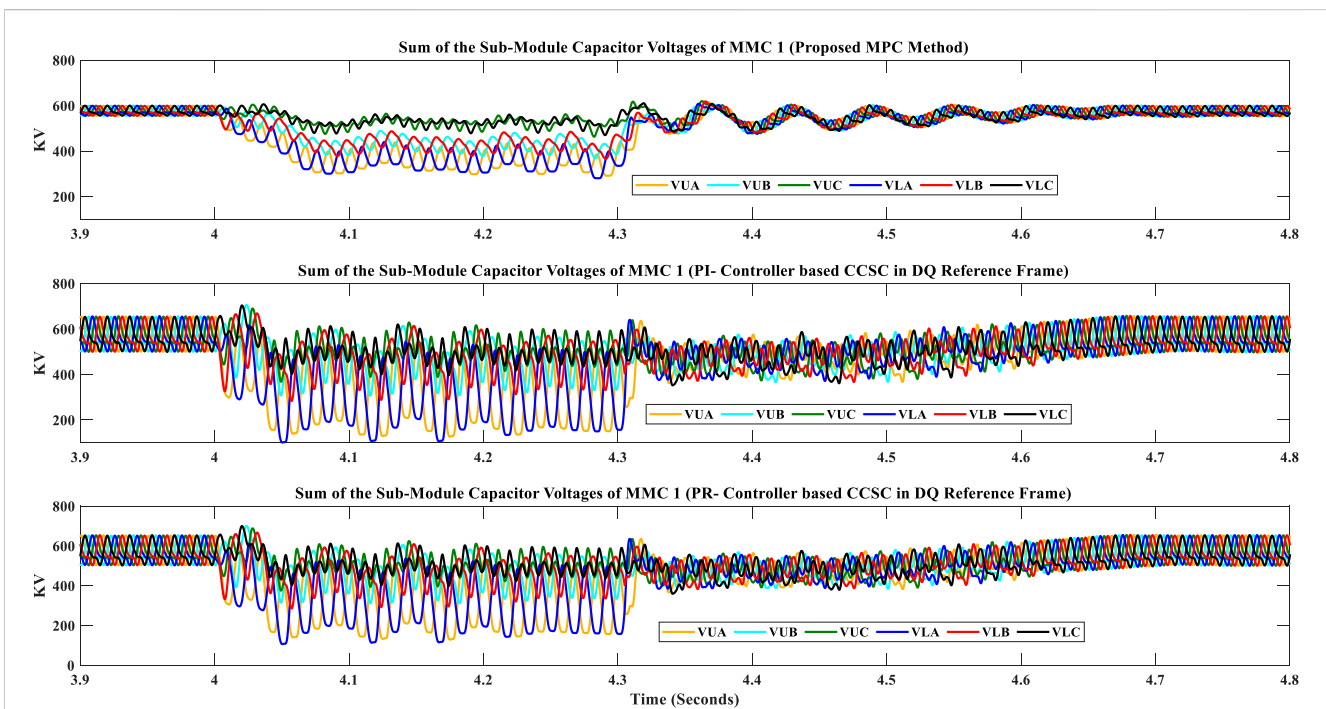


FIGURE 11 (A) Capacitor voltage ripple using proposed MPC method (B) Capacitor voltage ripple using the PI-controller-based CCC technique (C) Capacitor voltage ripple using the PR-controller-based CCC technique.

TABLE 2 Comparative analysis of the MPC controller versus traditional PI and PR controllers.

Performance Metrics	Advanced MPC controller	Traditional PI controller	Traditional PR controller
Effectiveness in CC Reduction	Superior	Moderate	Moderate
Steady-State Error for CC	Minimal	Greater	Greater
Efficacy in Second Harmonic Control	Complete	Partial	Partial
Impact on Converter Efficiency	Enhanced	Diminished	Diminished
Influence on Switch Current Stress	Lowered	Heightened	Heightened
Proficiency in capacitor voltage ripple Reduction	Superior	Moderate	Moderate
Stability of Capacitor Voltages	Stable	Variable	Variable

In comparison to Scenario 1, the complexity of mitigating capacitor voltage ripple and CC is heightened in situations involving an unbalanced grid, such as an SLG fault. It is pertinent to mention that arm capacitors are usually engineered to endure up to double the standard DC voltage. In Scenario 2, echoing the results from Scenario 1, the MPC controller outshines the traditional PI and PR-based methods in CC suppression, as evident by its swifter dynamic response and diminished steady-state discrepancies, which are highlighted in Figure 10. This controller proficiently minimizes the second harmonic current, leading to lower converter losses and alleviated stress on switching components. It addresses the capacitor voltage ripple problem effectively, sustaining even capacitor voltages and keeping operations within secure limits during the fault, as shown in Figure 11A. On the other hand, the PI and PR methodologies focus primarily on CC reduction, which leads to increased ripple magnitudes and uneven capacitor voltages, as Figure 11B, C illustrate. Therefore, the proposed MPC method demonstrates enhanced performance in managing CC and regulating capacitor voltages when juxtaposed with the PI and PR controllers, with this comparative performance encapsulated in Table 2.

The discussions presented previously establish that the suggested communication-independent AC FRT strategy delivers thorough FRT capabilities, circumventing the necessity for costly additional DC choppers. Furthermore, the refined CCC technique adequately controls the CC and capacitor voltage ripple, maintaining them within permissible thresholds. The system facilitates rapid recovery following faults and demonstrates a decrease in oscillations, specifically in THD.

5 Conclusion

This research work has successfully demonstrated the efficacy of communication free proposed MPC based method for MMC-HVDC systems addressing the challenges of FRT, CC suppression, and capacitor voltage ripple reduction under both normal and fault conditions. The proposed MPC based FRT method ensures the MMC-HVDC system's stability and reliability during disturbances without relying on additional external components like DC choppers. Simultaneously, the MPC algorithm adeptly handles various AC faults, maintains AC current tracking, and ensures effective CC suppression. It stands out in its ability to regulate capacitor voltages within grid-compliant levels while managing DC bus

voltage to facilitate desired power, even amidst AC faults. A thorough comparative evaluation has placed the proposed MPC control strategy in high regard, particularly when contrasted with traditional PI and PR-based controllers. With a faster dynamic response post-fault and proficient suppression of second harmonic currents, the proposed controller demonstrates an edge in performance, meeting stringent grid codes with lower steady-state errors and reduced losses. The promising results from this study not only highlight the efficiency of the proposed methodologies in current MMC-HVDC systems but also open up prospects for future integration with renewable energy sources. Plans to expand and validate the system in a Hardware-in-the-Loop (HIL) setup underscore the commitment to refining these strategies further, aiming to establish more robust, efficient, and versatile power transmission networks.

Data availability statement

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

Author contributions

MB: Methodology, Resources, Writing—original draft. JS: Conceptualization, Writing—original draft. KA: Investigation, Writing—review and editing. AM: Formal Analysis, Resources, Writing—review and editing. JA: Visualization, Supervision, Writing—review and editing. BA: Writing—review and editing. Project administration. MA: Writing—review and editing, Funding acquisition.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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