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EDITED BY

Yuqing Dong,
The University of Tennessee, Knoxville,
United States

REVIEWED BY

Haoasn Yang,
Hong Kong Polytechnic University, Hong
Kong SAR, China
Liang Zhang,
Southwest Petroleum University, China

*CORRESPONDENCE

Sihao Tang,
✉ tangsihao@hnu.edu.cn

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Phasor measurement method based on soft synchronized sampling with temporal pulse signal reference

Jie Zhang^{1,2}, Chao Tang¹, Chun Liu³, Hai Wang¹, Duan Junfeng⁴
and Sihao Tang^{4*}

¹State Grid Sichuan Electric Power Company Electric Power Science Research Institute, Chengdu, China, ²Sichuan Key Laboratory of Power Internet of Things, Chengdu, China, ³Leshan Power Supply Company of State Grid Sichuan Electric Power Company, Leshan, China, ⁴College of Electrical and Information Engineering, Hunan University, Changsha, China

Introduction: Phasor measurement is crucial for the monitoring and management of power grids. Traditional hardware-based phasor measurement units (PMUs) are effective but often complex and expensive. This paper introduces a software-based phasor measurement method that utilizes soft synchronization with temporal pulse signals from GPS and mobile communication stations, offering a simpler and cost-effective alternative.

Methods: The proposed method synchronizes the local oscillator with Pulse Per Second (PPS) signals from GPS and primary synchronization signals from mobile communication bases. Raw data affected by the local oscillator's instability are transformed into calibrated data using B-Spline interpolation to emulate an ideal sampling rate. The calibrated data are then subjected to a Recursive Discrete Fourier Transform (RDFT) algorithm for synchronized phasor measurement.

Results: The method's performance was assessed in compliance with the C37.118.1 standard. Key performance indicators, such as frequency, phase, and Total Vector Error (TVE), were evaluated. The proposed software-based approach demonstrated high accuracy in synchronized phasor measurements.

Discussion: The results confirm that the proposed method can serve as a highly accurate and simpler alternative to conventional hardware-based solutions. Its application promises to advance synchronized phasor measurement practices in power grid monitoring, enhancing reliability and reducing complexity and costs.

KEYWORDS

B-spline interpolation, synchronized sampling, synchrophasor estimation, temporal pulse, sampling time error

Abbreviations: ADC, Analog-to-digital converters; C37.118.1, IEEE standard for Synchrophasor measurements; CSACs, Chip-scale atomic clocks; DFT, Discrete Fourier transform; DOXO, Double-Oven controlled oscillators; FE, Frequency error; GNSS, Global navigation satellite system; GPS, Global positioning systems; NTP, Network time protocol; PLL, Phase locked loop; PPS, Pulse per second; PTP, Precision time protocol; RDFT, Recursive discrete Fourier transform; RFE, Rate of frequency error; STE, Sampling time error; TVE, Total vector error; VSI-OFM, Variable sampling interval control with operating frequency monitoring.

1 Introduction

Synchronized sampling is fundamental in power grid monitoring and is crucial for applications such as situational awareness (Appasani et al., 2021), fault location (Dashtdar et al., 2023), and oscillation monitoring (Almunif and Fan, 2019). This technique works by aligning the clocks in analog-to-digital converters (ADCs) with a universal time reference. Most often, this reference comes from Pulse Per Second (PPS) signals provided by Global Positioning Systems (GPS) (Pardo-Zamora et al., 2020), the IEEE 1588 Precision Time Protocol (PTP) (Ahmad Khan and Hayes, 2020), or the Network Time Protocol (NTP) (Park H. et al., 2021). Recently, synchronization signals from 5G networks have also been used (Xiao et al., 2021).

However, a persistent and yet unresolved challenge is observed in achieving consistent synchronization accuracy for all sampled data points within each standard 1-s timing interval (Qiu et al., 2021). While synchronization of the first sample in each interval across different monitoring devices is generally successful, subsequent samples exhibit diminished accuracy (Yao et al., 2016a). This degradation in synchronization is attributed to the inherent asynchrony between the local oscillators that govern the ADCs and the universal time references such as PPS signals (Jiang et al., 2000). The resultant Sampling Time Errors (STEs) not only accumulate but also significantly impair the performance and reliability of applications that are contingent upon high-fidelity synchronized data (Yao et al., 2016b). Thus, the motivation for this study is to explore an economical and effective solution to this pressing issue.

Various methods have been tried to improve the accuracy of synchronized sampling in power grids. One notable approach uses an external Phase Locked Loop (PLL) (Mellino et al., 2017). While this method improves time resolution, it has downsides such as high costs and long setup times, limiting its practical use (Gentile, 2009; Bondarev et al., 2022).

Another technique, called Variable Sampling Interval Control with Operating Frequency Monitoring (VSI-OFM), directly adjusts the ADC's sampling times (Yao et al., 2016b). This approach does reduce errors but makes the system more complicated, limiting its applications.

Lastly, high-precision clocks like chip-scale atomic clocks (CSACs) (Zhan et al., 2016) and Double-Oven Controlled Oscillators (DOXO) (Yao et al., 2019) have been explored. These provide stable frequencies but come with challenges like high costs and complexity, and in the case of DOXO, higher power consumption, making them less practical for wide use.

In summary, traditional hardware-focused methods like PLL, VSI-OFM, CSAC, and DOXO have their merits but also come with challenges such as cost, complexity, and limited applicability. These issues make it important to explore other, more flexible and cost-effective solutions.

One such promising alternative is soft synchronized sampling. This approach corrects timing errors between two consecutive PPS signals using interpolation techniques, eliminating the need for frequent adjustments of the ADC. While earlier methods like two-point interpolation (Ge and Zhang, 2021) and polynomial interpolation (Park S. H. et al., 2021) have been tried, they often fall short in terms of flexibility and accuracy. That's where this study comes in. We use B-Spline interpolation (Taghipour and Aminikhah, 2022) for its benefits like better curve fitting, smoothness, and low

computational needs (Greco and Cuomo, 2013). This makes it ideal for real-time applications that demand both accuracy and efficiency. Therefore, our paper introduces a new soft synchronized sampling method based on B-Spline interpolation. The contributions of this paper are summarized as follows:

- (1) A streamlined yet effective sampling methodology based on B-Spline interpolation is introduced. The need for frequent adjustments to the ADC is thus eliminated, resulting in a simplified sampling process.
- (2) A comprehensive analysis is provided that illustrates the advantages of B-Spline interpolation over traditional interpolation methods. Its suitability for high-fidelity synchronized sampling in power grid monitoring is thereby demonstrated.
- (3) The proposed methodology is rigorously validated against the C37.118.1 standard. Key performance indicators, such as frequency, phase, and Total Vector Error (TVE), are evaluated, confirming the method's practicality and advanced capabilities.

The remainder of this paper is organized as follows: Section 1 delves into the theoretical underpinnings of the proposed soft synchronized sampling scheme, elucidating the mechanics of B-Spline interpolation in the context of STE correction. Section 2 presents the experimental setup and methodology employed to validate the proposed approach, adhering to the C37.118.1 standard. Section 3 discusses the results obtained from both simulation and hardware experiments, evaluating key performance indicators such as frequency, phase, and Total Vector Error (TVE). Finally, Section 4 offers concluding remarks and outlines potential avenues for future research.

2 Methodology

2.1 Characteristics of PPS signals and local oscillator monitoring

Pulse Per Second (PPS) signals, commonly generated by systems such as Global Positioning Systems (GPS) and Precision Time Protocol (PTP), serve as a universal time reference for achieving synchronized sampling. These square-wave signals typically operate at a frequency of 1 Hz and have a pulse width ranging from 100 ms to 200 ms. The level type for these signals is generally TTL (Transistor-Transistor Logic). The mathematical representation of the PPS signal can be expressed as:

$$PPS(t) = A \cdot \text{sgn}(\sin(\pi ft)) \quad (1.1)$$

where A is the amplitude, $\text{sgn}(x)$ is the signum function, and f is the frequency, which is 1 Hz for PPS.

The PPS signal serves as a critical reference for monitoring the local oscillator, which drives the Analog-to-Digital Converter (ADC) during the sampling process. Accurate sampling is contingent upon the precise frequency of this local oscillator. To monitor the local oscillator's frequency, a microcontroller unit (MCU) typically controls a timer, which counts the number of oscillations between two consecutive PPS signals. The frequency of the local oscillator is then calculated as:

$$f_{\text{local}} = \frac{N_{\text{counts}}}{T_{\text{interval}}} \quad (1.2)$$

where f_{local} is the frequency of the local oscillator, N_{counts} is the number of timer counts, and T_{interval} is the time interval between two consecutive PPS signals, usually 1 s.

By using the PPS signal as a reference, the MCU can accurately determine the frequency of the local oscillator, setting the stage for subsequent calibration steps to mitigate Sampling Time Errors (STEs).

2.2 Sampling data correction based on B-spline interpolation

Upon obtaining the actual frequency f_{local} of the local oscillator through the method described in the section ‘‘Characteristics of PPS Signals and Local Oscillator Monitoring,’’ the next pivotal step is to utilize B-spline interpolation techniques to rectify the sampling time errors (STEs) that occur within each 1-s interval between two PPS signals.

B-spline interpolation was chosen for its capacity to produce smooth curves while allowing local control over curve shape, thus offering a balance between accuracy and flexibility. This method is also computationally less intensive compared to others such as kriging, making it well-suited for handling the large datasets that were critical for this study. Its computational efficiency is complemented by its robustness to noise, an essential feature given the noisy nature of the data used in our experiments. Furthermore, B-spline interpolation provides the versatility required for our study, as it can be adapted to handle both one-dimensional and two-dimensional data efficiently. Alternative methods like cubic interpolation and kriging were initially considered but were ruled out due to their computational intensity and lower robustness to noise.

The actual to ideal sampling interval ratio R serves as a crucial parameter for the B-spline interpolation technique. To elaborate, the B-spline interpolation function can be mathematically represented as:

$$f(x) = \sum_{i=0}^n P_i \cdot N_{i,k}(x) \tag{1.3}$$

Here, $f(x)$ stands for the interpolating function that provides an approximation of the original data. The variables P_i denote the control points, which are instrumental in shaping the curve, $N_{i,k}(x)$ are the B-spline basis functions of degree k and n indicates the total number of control points used for interpolation. The B-spline basis functions $N_{i,k}(x)$ are recursively defined as:

$$N_{i,0}(x) = \begin{cases} 1, & \text{if } x_i \leq x < x_{i+1} \\ 0, & \text{otherwise} \end{cases} \tag{1.4}$$

$$N_{i,k}(x) = \frac{x - x_i}{x_{i+k} - x_i} \cdot N_{i,k-1}(x) + \frac{x_{i+k+1} - x}{x_{i+k+1} - x_{i+1}} \cdot N_{i+1,k-1}(x)$$

$N_{i,k}(x)$ and $N_{i+1,k-1}$ are the previous degree B-spline basis functions. The terms $\frac{x-x_i}{x_{i+k}-x_i}$ and $\frac{x_{i+k+1}-x}{x_{i+k+1}-x_{i+1}}$ serve as weighting factors, determining how much influence the previous degree basis functions have on the current function. The breakpoints x_i and x_{i+1} decide the intervals over which the weighting factors and the basis functions are defined.

The control points P_i play a pivotal role in the curve-fitting process. Their determination is rooted in the actual to ideal sampling interval ratio, denoted as R . This ratio R is defined as:

$$R = \frac{T_a}{T_i} \tag{1.5}$$

where T_a represents the actual sampling interval and T_i stands for the ideal sampling interval. From the ratio R , the control points P_i can be directly calculated as a product of R and a coefficient α_i . Specifically, each control point is given by:

$$P_i = R \cdot \alpha_i \tag{1.6}$$

where α_i are pivotal parameters that are optimized to minimize the error between the interpolated and actual data points. In essence, these coefficients are responsible for ensuring that the B-spline interpolation aligns closely with the actual data. This error minimization is achieved through a least-squares optimization process. The objective function for this optimization is expressed as:

$$\min_{\alpha} \sum_{j=0}^m (f(x_j) - y_j)^2 \tag{1.7}$$

In this equation, y_j are the actual data points and m is the number of data points. By employing this detailed B-spline interpolation technique, the algorithm can effectively calibrate the STEs based on the monitored frequency of the local oscillator f_{local} , thereby achieving a higher degree of accuracy in synchronized sampling.

2.3 Phasor measurement based on corrected sampled data

To validate the effectiveness of the proposed algorithm, this study employs the calibrated samples to perform synchronized phasor computation in the power grid. The method chosen for this purpose is the Recursive Discrete Fourier Transform (DFT) algorithm. The principal theory behind this algorithm is as follows:

$$X[k] = (1 - \lambda) \cdot (X[k-1] + x[k] - X[k - N]) \tag{1.8}$$

Where $X[k]$ is the DFT output at the k^{th} sample, $x[k]$ is the k^{th} sample of the input signal, N is the window length, and λ is the forgetting factor. The magnitude $|X[k]|$ and phase $\angle X[k]$ of the DFT output can be calculated as:

$$|X[k]| = \sqrt{\text{Re}(X[k])^2 + \text{Im}(X[k])^2} \tag{1.9}$$

$$\angle X[k] = \text{atan2}(\text{Im}(X[k]), \text{Re}(X[k]))$$

Subsequently, the synchronized phasor \mathbf{P} can be derived from $X[k]$ as follows:

$$\mathbf{P} = A \cdot e^{j\phi} = |X[k]| \cdot e^{j\angle X[k]} \tag{1.10}$$

To quantify the accuracy of the phasor estimation, the concept of Total Vector Error (TVE) is introduced as a technical indicator for the subsequent experimental section. TVE is defined as:

$$\text{TVE} = \sqrt{\left(\frac{|\mathbf{P}_{\text{estimated}} - \mathbf{P}_{\text{actual}}|}{|\mathbf{P}_{\text{actual}}|} \right)^2} \tag{1.11}$$

Here, $\mathbf{P}_{\text{estimated}}$ is the estimated phasor and $\mathbf{P}_{\text{actual}}$ is the actual phasor. A lower TVE indicates a higher accuracy in phasor estimation.

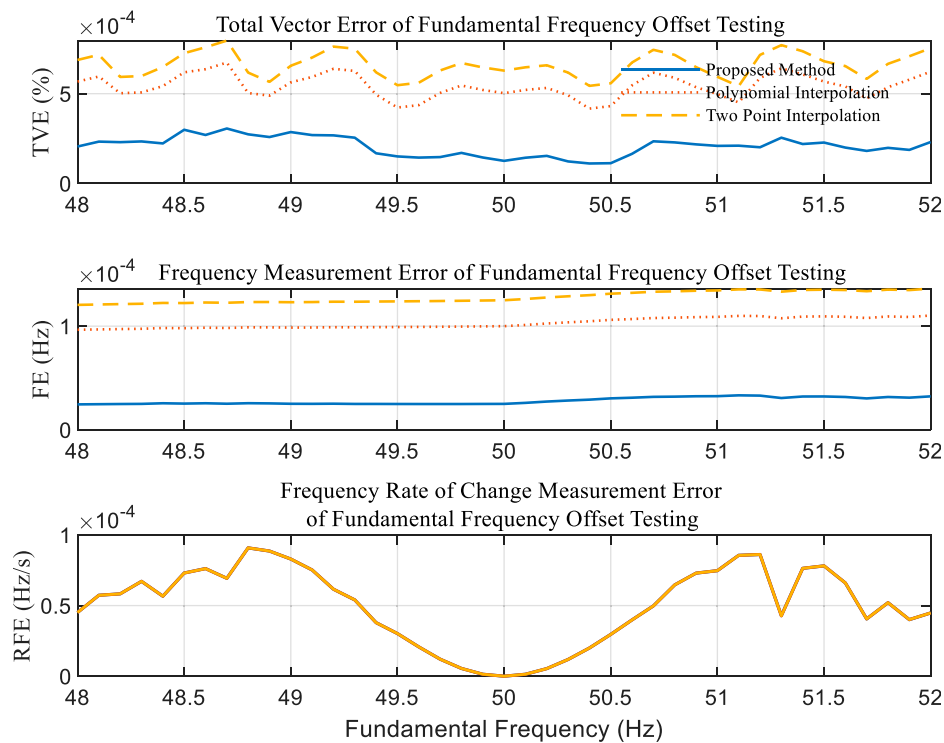


FIGURE 1
C37.118.1 fundamental frequency offset testing.

By employing the Recursive DFT algorithm on the calibrated samples obtained through B-spline interpolation, the system achieves high-accuracy phasor estimation, thereby enhancing the reliability and effectiveness of power grid monitoring systems.

3 Performance evaluation

To substantiate the efficacy of the proposed B-spline interpolation technique coupled with Recursive DFT for synchronized phasor estimation, a series of simulation experiments were conducted. The experiments were designed to emulate real-world scenarios encountered in power grid monitoring.

The simulation experiments are performed using a dedicated experimental setup to ensure the study's reproducibility and credibility. The hardware and software configurations are explicitly stated as follows:

- **Software Environment:** The simulations are conducted using MATLAB/Simulink, which incorporates the IEEE C37.118.1 standard for performance evaluation.
- **Hardware Configuration:** While the specific hardware setup is not critical for the MATLAB/Simulink-based simulations, it is noted that a computer with at least an Intel Core i7 processor and 16 GB RAM is used to ensure smooth execution of the simulations.
- **Signal Specifications:** A 50 Hz sinusoidal signal serves to simulate the voltage and current waveforms in the power grid.

- **Local Oscillator Frequency:** The local oscillator frequency is adjusted to vary within a range of ± 100 ppm to emulate the frequency drift commonly observed in real-world applications.

For comparative analysis, the proposed B-spline interpolation technique is rigorously benchmarked against traditional interpolation methods, including two-point interpolation and polynomial interpolation.

For comparative analysis, the proposed B-spline interpolation technique was benchmarked against traditional interpolation methods, specifically two-point interpolation and polynomial interpolation.

3.1 Steady-state conditions testing

Fundamental Frequency Offset Testing: In the conducted experiment, the frequency setting range for the power system is established between 45 Hz and 55 Hz, with an incremental step of 0.1 Hz. The thresholds for Total Vector Error (TVE), Frequency Error (FE), and Rate of Frequency Error (RFE) are set at 1%, 5 mHz, and 0.01 Hz/s, respectively.

As evidenced by Figure 1, all three algorithms under investigation satisfy the criteria delineated by the C37.118.1 standard. Notably, the proposed algorithm demonstrates superior performance in terms of both total phasor error and frequency measurement error, with average values recorded at $2 \times 10^{-4}\%$ and 2.5×10^{-5} Hz, respectively. In the

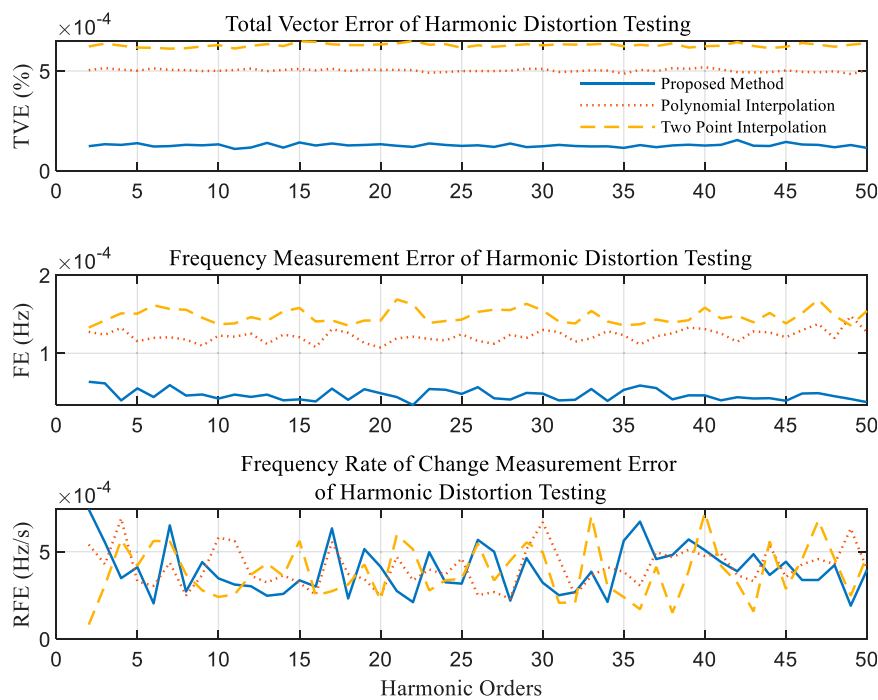


FIGURE 2
C37.118.1 harmonic distortion testing.

context of measuring the rate of frequency change, the performance across the three algorithms is observed to be comparable, with errors not exceeding 1E-4 Hz/s.

Harmonic Distortion Test: In the present experiment, the focus is on evaluating the algorithm’s measurement performance under the influence of harmonic interference. Harmonics ranging from the second to the 50th are added to the fundamental component for this purpose. According to the standard, the maximum allowable Total Vector Error (TVE) is set at 1%, while the thresholds for Frequency Error (FE) and Rate of Frequency Error (RFE) are established at 25 mHz and 0.1 Hz/s, respectively.

As corroborated by Figure 2, all three algorithms under scrutiny successfully meet the stipulated standard criteria. Importantly, the proposed algorithm exhibits superior performance in both TVE and FE metrics when compared to the other two algorithms under investigation.

Out-of-band interference test: In the experiment focused on out-of-band interference (OOBI), OOBI signals are superimposed onto the test signal within the frequency ranges of 10–45 Hz and 55–100 Hz. The frequency is incremented in steps of 0.1 Hz, and the amplitude of the interference is set at 10% of the fundamental component. According to the IEEE standard, the allowable limits for Total Vector Error (TVE), Frequency Error (FE), and Rate of Frequency Error (RFE) are defined as 1.3%, 10 mHz, and 0.1 Hz/s, respectively.

As substantiated by Figure 3, the performance metrics for all three algorithms under evaluation are nearly identical. This uniformity in performance is attributed to the significant degradation in measurement accuracy induced by OOBI. In this

specific scenario, the error resulting from sampling rate offset is markedly overshadowed by the error introduced by OOBI. Consequently, any efforts to enhance measurement accuracy should primarily focus on refining the synchronized phasor measurement algorithm.

3.2 Dynamic conditions testing

Amplitude Modulation Test: For the purpose of evaluating the efficacy of the proposed method in the context of small oscillations within power systems, tests are conducted under both amplitude-modulated and phase-modulated conditions. The modulated signal employed for these tests is represented in its general form as follows:

$$X_a = X_m [1 + k_x \cos(2\pi f_m t)] \times \cos(2\pi f_0 t + \phi) \tag{1.12}$$

where k_x represent the amplitude modulation depths. f_m and f_0 is the modulation frequency and nominal power system frequency respectively. X_m is the amplitude of the input signal. At reporting time tags $t = nT$ (where n is an integer and T is the phasor reporting interval) the PMU shall produce a synchrophasor measurement of:

$$X(nT) = \{X_m / \sqrt{2}\} [1 + k_x \cos(2\pi f_m nT)] \angle \phi \tag{1.13}$$

From the results in Figure 4, it is observed that the measurement error exhibits a proportional increase with the escalation of modulation frequency. Notably, the proposed algorithm maintains commendable measurement performance even under amplitude modulation testing conditions at a modulation frequency of 5 Hz.

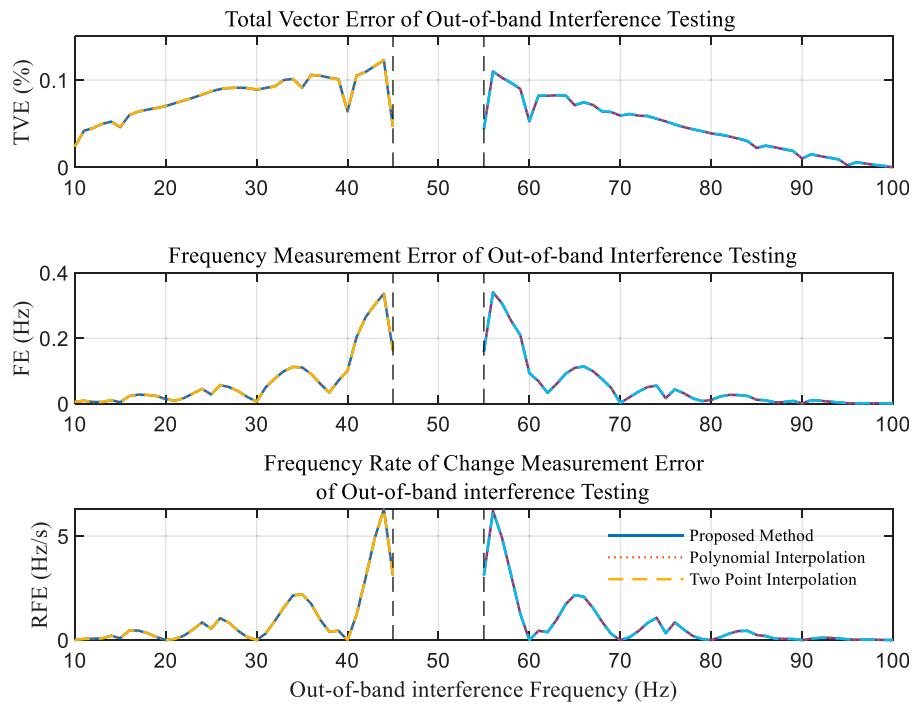


FIGURE 3
C37.118.1 out-of-band interference testing.

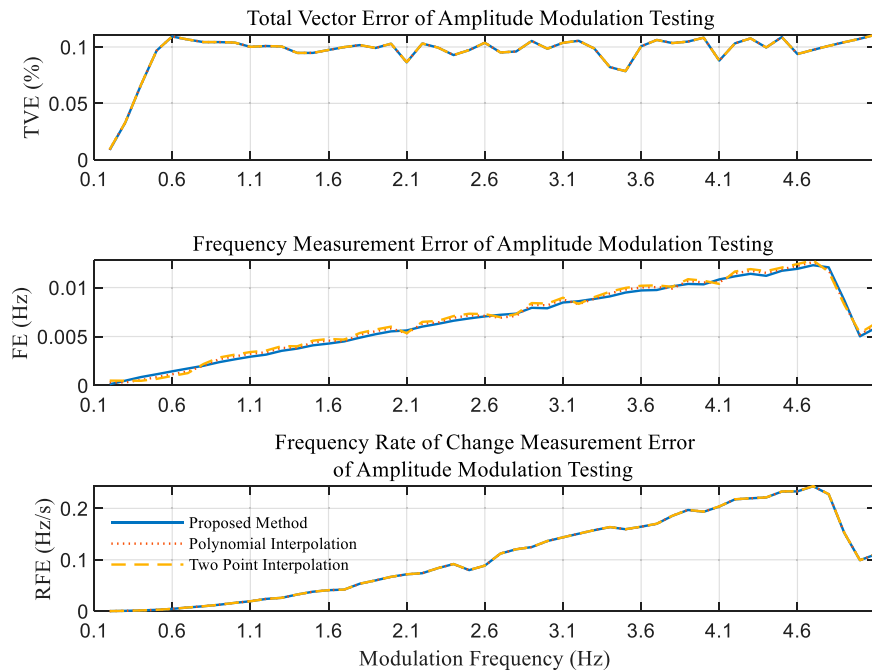


FIGURE 4
C37.118.1 amplitude modulation testing.

Furthermore, when evaluated against the Frequency Error (FE) index, the proposed algorithm demonstrates a marked superiority over the other two algorithms employed for comparative analysis.

Phase Modulation Test: To assess the performance of the proposed method under small oscillations in power systems, behaviors under either amplitude or phase-modulated conditions are:

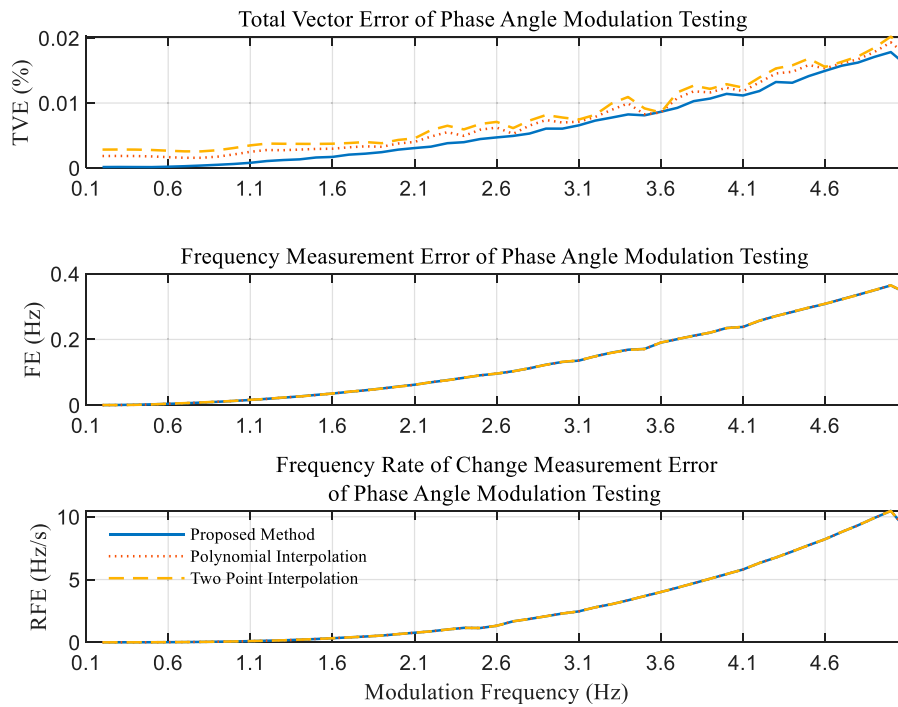


FIGURE 5 Phase angle modulation testing.

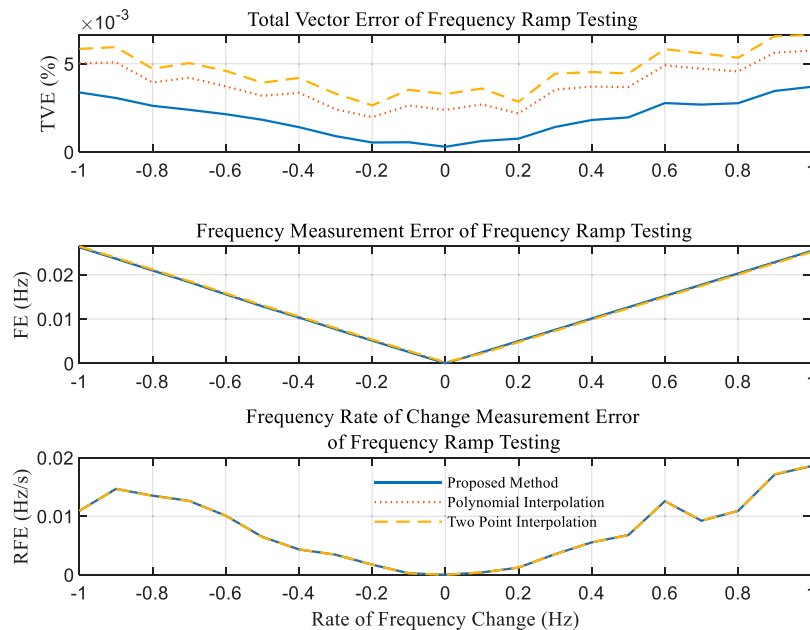


FIGURE 6 Frequency ramp testing.

$$X_a = X_m \times \cos[2\pi f_0 t + k_a \cos(2\pi f_m t - \pi)] \quad (1.14)$$

The parameters delineated in Eq. 1.14 bear identical significance to those in Eq. 1.12. Correspondingly, the phasor associated with the input signal is represented as follows:

$$X(nT) = \{X_m / \sqrt{2}\} \angle \{k_a \cos(2\pi f_m nT - \pi)\} \quad (1.15)$$

Based on the experimental data shown in the Figure 5, it is evident that the performance disparities among the three algorithms are minimal in the context of phase modulation testing. However,

the proposed algorithm exhibits a marginal superiority when assessed against the Total Vector Error (TVE) index.

Frequency Ramp Test: Given that the frequency of the power system is inherently variable, it becomes imperative to evaluate the measurement performance of the methods under conditions of frequency fluctuations. For this analysis, the system frequency is still assumed to be 50 Hz; however, any alteration in frequency is mathematically considered as a change in the phase angle. The input signals for this scenario can be mathematically represented as follows:

$$X_a = X_m \cos[2\pi f_0 t + \pi R_f t^2] \quad (1.16)$$

where X_m is the amplitude of the input signal, and R_f is the frequency ramp rate in Hz/s. Its corresponding phasor at time nT is:

$$X(nT) = \{X_m/\sqrt{2}\} \angle \{\pi R_f (nT)^2\} \quad (1.17)$$

The IEEE Standard limits for this test are 1%, 10 mHz, and 0.1 Hz/s, respectively. Clearly, the proposed method fully satisfies the IEEE Standard requirements. Furthermore, based on the Total Vector Error (TVE) outcomes, it is evident that the proposed algorithm is more effective in mitigating the sampling time error within the collected data. In contrast, the other two algorithms under evaluation exhibit inadequate efficacy in eliminating such errors, thereby leading to residual sampling time errors. This observation is substantiated by the results presented in Figure 6.

4 Conclusion

In the realm of power grid monitoring, this study introduces a pioneering soft synchronization-based phasor measurement method. Leveraging time pulse signals from GNSS or mobile stations, the local oscillator is meticulously observed. This is followed by the B-spline interpolation which refines the raw data, bringing it in line with an ideal sampling rate. Subsequently, the synchrophasor is extracted using a recursive DFT algorithm.

Beyond the technical advancements, the practical significance of this research lies in its potential to seamlessly integrate into existing power grid systems. By validating the method against the C37.118.1 standard and juxtaposing it with both two-point and polynomial interpolations, it has been demonstrated that the proposed approach not only simplifies the phasor measurement process but also augments accuracy. This suggests a shift towards a more cost-effective and efficient means of monitoring, reducing the reliance on more complex hardware-based solutions. As power grid infrastructures continue to evolve, this method holds promise in enhancing the reliability and efficiency of real-world applications.

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Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material, further inquiries can be directed to the corresponding author.

Author contributions

JZ: Conceptualization, Formal Analysis, Funding acquisition, Investigation, Methodology, Validation, Writing–original draft. CT: Data curation, Methodology, Visualization, Writing–review and editing. CL: Software, Writing–review and editing. HW: Validation, Writing–review and editing. DJ: Data curation, Writing–review and editing. ST: Writing–review and editing.

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Conflict of interest

Authors JZ, CT, and HW were employed by State Grid Sichuan Electric Power Company Electric Power Science Research Institute. Author CL was employed by Leshan Power Supply Company of State Grid Sichuan Electric Power Company.

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The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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