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## Low voltage protection method of DFIG based on rotor-side double current limiting circuit

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A doubly fed induction generator (DFIG) configured for crowbar protection faces the following problems during low voltage ride through (LVRT): delayed input of crowbar protection and the difficulty in coordinating current limiting targets and DC voltage overrun with constant resistance rectification. A low voltage protection method of a DFIG based on a rotor-side double current limiting circuit is proposed. The rotor current characteristics during a fault are analyzed from a time domain perspective and used as a basis for resistance setting. The transient response characteristics of a resistive superconducting fault current limiter (RSFCL) are used for fast initial suppression of rotor currents. The adaptive crowbar resistance adjustment method is used to realize the coordinated consideration of current limiting and DC voltage non-overrun. The simulation results show that the proposed protection method effectively shortens the actual input time of the current limiting circuit and has good suppression ability for the rotor current at the early stage of fault. The adaptive and flexible resistance setting of the controllable crowbar circuit ensures that the DC voltage does not exceed the limit during the fault current limiting period, which helps improve the LVRT capability of doubly fed wind turbines.

#### KEYWORDS

doubly fed induction generator, low voltage ride through, double current limiting circuit, resistive superconducting fault current limiter, resistance setting

### 1 Introduction

Doubly fed induction generators (DFIGs) are widely used under the goals of China's carbon peaking and carbon neutrality (De Souza et al., 2022). The rotor side of the DFIG induces a large electromotive force, which leads to rotor overcurrent when the grid voltage drops. The overcurrent in the rotor may cause damage to the inverter and generator and even lead to disconnection of the DFIG from the grid when more serious. Therefore, the short-circuit current and DC voltage on the rotor side are often used as important indicators to evaluate the LVRT capability of the DFIG (Okedu et al., 2012; Ren et al., 2022; Chen et al., 2021).

Oriented to the rotor current suppression during LVRT, the current research is centered on the control strategies and hardware circuits. As for control strategies, the LVRT performance of the DFIG is improved by using differential feedforward control of the stator current (Huilan et al., 2021). In Xiao et al. (2012) and Ding et al. (2021), a current limitation method has been proposed by controlling the magnetic chain. Although it does not rely on hardware circuits, it involves complex magnetic chain observation and separation techniques that are difficult to implement and not highly adaptable. Overall, it is difficult to effectively limit the rotor current by relying only on inverter control methods. Hardware circuits are still required to limit the current when the rotor current is at a higher level.

For more serious faults, the DFIG is usually equipped with an external circuit to suppress the rotor current, and one of the conventional methods used is crowbar protection (Camacho et al., 2017; Döşoğlu, 2020; Hamdan and Noureldeen, 2021). After a fault occurs, the short-circuit current is limited by blocking the rotor-side converter (RSC) and putting in a crowbar circuit. While limiting the current, the resistor also bears a part of the voltage. Although a large resistance can effectively suppress the rotor overcurrent, too large a crowbar resistance will cause the DC voltage to rise, and there will be the risk of voltage overrun (Pannell et al., 2010; Justo et al., 2015). The conventional method always has a fixed resistance setting, therefore the conventional crowbar protection is poorly coordinated and the objectives of the current limiting and avoiding DC overvoltage cannot be achieved simultaneously (Reddy and Saha, 2022). On the basis of conventional crowbar protection, there are some research devoted to the improvement of crowbar protection, such as the setting up of a resistance value for the crowbar. A method for implementing fault ride-through by the hierarchical input of protection circuits was proposed by Zhao et al. (2016). An LVRT scheme for the DFIG based on crowbar parallel dynamic resistance was proposed by Zhang and Jiang (2014). However, methods used by Zhao et al. (2016) and Zhang and Jiang (2014) result in longer investment time for parallel resistors, which is not conducive for rapid protection after a fault. An adaptive switching strategy for crowbar protection has been proposed by Tan et al. (2021). The neural networks are used to efficiently fit DFIG rotor current transient processes after resection. The application of this method in engineering practice remains to be verified. A new crowbar circuit structure was proposed by Yongqing et al. (2014), but the resistance setting value of the crowbar resistance was not specified. A new type of resistance series capacitive crowbar structure had been proposed by Zheng et al. (2012), but it is not easy to apply in practice. The crowbar protection solutions studied in the existing literature basically focus on performance optimization after the crowbar is put in, such as the adaptive resistance setting of the crowbar. They are useful for improving the LVRT performance and avoiding DC voltage overruns and have brought new solution ideas for the crowbar resistance setting. However, the assumptions of the aforementioned studies are overly ideal, that is, they assume that the crowbar resistor is put in at the moment of fault but ignore the fact that the crowbar is not actually put in instantaneously after a fault, there is a big difference with the actual response process.

In fact, according to the operating regulations of LVRT, the detection of the voltage drop (fault detection) is the basis of LVRT implementation, and there is a significant delay in the input of the actual crowbar protection. The conventional method is used to calculate the RMS value of the voltage through fast Fourier transform (FFT), which has a long calculation window. Thus, there is an obvious time delay (basically around 10 ms) in identifying faults and crowbar actions (Chakraborty and Maity, 2023). Some rapid fault detection methods have been proposed to facilitate the rapid implementation of LVRT. Fan and Liu (2012) used park transform to detect faults, but the method relies on filters,

which may cause lag in the detection algorithm. Wavelet transform and Hilbert-Huang transform (HHT) methods were used to detect faults in Costa and Driesen (2012) and Hasan et al. (2020), respectively. Mathematical methods theoretically have faster detection speed, and the verification results show that the fault detection time is approximately 5 ms, but it is difficult to implement this in practice. The short-circuit current shows a decaying characteristic, and the current is maximum at the instant after the fault. However, due to the input delay of the crowbar resistor, the rotor current cannot be effectively suppressed at the early stage of the fault, which poses a serious threat to the inverter, which is also a problem at present. Although some of the aforementioned studies try to solve the delay of LVRT or crowbar protection input, they basically rely on complex mathematical methods, which have to be further tested for both practical engineering applications and implementation. Therefore, it is necessary to carry out further research on it and open up new ideas to solve the delay of the LVRT input.

Analogous to the current limiting objective of the DFIG and looking at system-level short-circuit current limiting measures, some valid studies can be found. At the system level, without changing the topology of the system, many scholars have investigated fault limiters. This is because short-circuit currents can be effectively suppressed by simply putting in a fault current limiter in the post-fault circuit, and this is especially true for resistive fault current limiters. This is the same basic logic as the DFIG input of crowbar resistors. Resistive superconducting fault current limiter (RSFCL) is usually used to limit short-circuit current in power systems. The current limiter can be considered a purely resistive element after a fault, which ultimately achieves the goal of current limitation. Bock et al. (2014) stated that RSFCL is an excellent means of limiting short-circuit currents, which has been verified. Although it is not directly applied to the current limitation of the DFIG, it opens up ideas for research in this work. Xi et al. (2019) analyzed the application of RSFCL in DC systems and showed a good current limiting effect. Jiang et al. (2021) also analyzed the application of RSFCL for reclosing of DC systems, and pointed out to its good current limiting characteristics. SE et al. (2019) connected RSFCL in series to the current limiting between the RSC and step-up transformer, which enhanced the LVRT capability of the DFIG by connecting the resistor in series, but the types of faults that can actually be coped with are not comprehensive. In summary, regarding the application of RSFCL in power systems, it is generally proved that the response is good, but its practical application to a DFIG is still relatively small. It is undeniable that the application of RSFCL in the power system has the possibility of migrating the application to the DFIG system. In particular, RSFCL has nearly transient response characteristics and the potential to shorten the delay of the traditional crowbar protection input.

It is not difficult to find that the existing studies on the adjustment of crowbar resistance ignore the fact of input delay, and the DFIG is still exposed to the risk of overcurrent at the instant of fault. While addressing the fault detection delay work, it is mostly difficult to implement, and the effectiveness is difficult to measure. The two parts (crowbar input delay and avoiding DC voltage overrun) are relatively independent and not well combined to form a perfect LVRT strategy. In order to effectively enhance the



LVRT capability of the DFIG, it is expected that the current is limited quickly after a fault and guaranteed that the DC voltage will not overrun during the current limiting period. In this paper, a low voltage protection method of the DFIG based on a rotor side double current limiting circuit is proposed, which will address both of these problems from the point of view of the easiest engineering implementation. The research idea is shown in Figure 1. By putting in RSFCL at the instant of the fault, the huge increase in current at the beginning of the fault is suppressed effectively. Different crowbar resistance values are adaptively put in depending on the rotor current and the DC voltage restraint, and DC voltage overrun is prevented. A simulation verification was carried out in PSCAD. The effectiveness of the DFIG low voltage protection scheme proposed in this article is verified.

## 2 Analysis of DFIG fault characteristics

The setting of the crowbar resistance value depends on the rotor current, and to more accurately characterize the faults of the DFIG, the dynamic mathematical model of the rotor is first analyzed. In general, traditional crowbar resistors are calibrated to the maximum shortcircuit current or to when a three-phase symmetrical fault occurs. There are two problems with this method of setting: first, three-phase short circuits occur infrequently and more asymmetrical faults occur. Second, the rectification is too harsh and the resistance value is not flexible, which may lead to problems such as DC voltage overrun.

Therefore, in conjunction with the practical situation and the methodology proposed in this work, the focus will be on analyzing the DFIG fault characteristics during asymmetric faults.

Assuming that the grid voltage falls asymmetrically due to a fault at time  $t_0$ , the stator voltage in the rotor coordinate system can be described as

$$\boldsymbol{u}_{s}^{r} = \boldsymbol{U}_{s}^{+} \mathbf{e}^{\mathbf{j} s \omega_{s} t} + \boldsymbol{U}_{s}^{-} \mathbf{e}^{-\mathbf{j} s \omega_{s} t}, \qquad (1)$$

where  $u_s^r$  is the stator voltage in the rotor coordinate system;  $U_s^+$  and  $U_s^-$  indicate the terminal positive and negative voltages, respectively; *s* represents the slip ratio; and  $\omega_s$  denotes the synchronous speed.

Due to the inability to mutate the stator chain after failure and considering that the stator inductance ( $L_s$ ) is much larger than the stator resistance ( $R_s$ ), after neglecting the relevant terms, the rotor open circuit voltage  $u_{r_0}^r$  induced by the stator magnetic chain can be obtained as

$$\begin{cases}
\boldsymbol{u}_{ro}^{r} = \boldsymbol{u}_{ro1}^{r} + \boldsymbol{u}_{ro2}^{r} + \boldsymbol{u}_{ron}^{r} \\
\boldsymbol{u}_{ro1}^{r} = U_{s}^{+} \frac{L_{m}}{L_{s}} s e^{js\omega_{s}t} \\
\boldsymbol{u}_{ro2}^{r} = U_{s}^{-} \frac{L_{m}}{L_{s}} (2-s) e^{-j(2-s)\omega_{s}t} \\
\boldsymbol{u}_{ron}^{r} = -\frac{(U_{s} - U_{s}^{+} + U_{s}^{-})}{j\omega_{s}} e^{j\omega_{s}t_{0}} \frac{L_{m}}{L_{s}} (1-s) e^{-\frac{(t-t_{0})}{T_{s}}} e^{-j\omega_{r}t},
\end{cases}$$
(2)

where  $u_{ro1}^r$ ,  $u_{ro2}^r$ , and  $u_{ro2}^r$  are the three types of rotor voltage components,  $L_m$  represents the magnetizing inductance,  $L_s$  denotes the stator inductance,  $U_s$  is the terminal voltage, and  $T_s$  indicates the decay time constant.

It can be seen that there are three voltage components in the DFIG under asymmetrical faults, corresponding to which there are three current components. Therefore, the superposition theorem can be used to find the rotor current during fault.

The rotor current component during an asymmetrical fault under the action of the three voltage-forcing components is expressed by Eqs. 3–5:

$$\boldsymbol{i}_{ro1}^{r} = -\frac{L_m}{L_s} \frac{sU_s^+}{js\omega_s\sigma L_r + R_r + R_c} e^{js\omega_s t},$$
(3)

$$\mathbf{i}_{ro2}^{r} = \frac{L_m}{L_s} \frac{(2-s)U_s^-}{j(2-s)\omega_s \sigma L_r - R_r - R_c} e^{-(2-s)\omega_s t},$$
(4)

$$\mathbf{i}_{ron}^{r} = -\frac{L_{m}}{L_{s}} \frac{(1-s)\left(U_{s} - U_{s}^{+} + U_{s}^{-}\right)}{j\omega_{r}\sigma L_{r} - R_{r} - R_{c}} \mathrm{e}^{j\omega_{s}t_{0}} \mathrm{e}^{-(t-t_{0})/T_{s}} \mathrm{e}^{-j\omega_{r}t}.$$
 (5)

Since the fault current at moment  $t_0$  cannot change abruptly, the rotor current also contains a DC component  $i_{rn}^r$  that decays exponentially with the time constant  $T_r$ , which can be determined as

$${}^{r}_{rn} = \left( {\boldsymbol{i}}^{r}_{r(t_0)} - {\boldsymbol{i}}^{r}_{ro1(t_0)} - {\boldsymbol{i}}^{r}_{ro2(t_0)} - {\boldsymbol{i}}^{r}_{ron(t_0)} \right) e^{-t/T_r}.$$
 (6)

In summary, the rotor current during an asymmetrical fault is expressed as



$$\mathbf{i}_{r}^{r} = \mathbf{i}_{ro1}^{r} + \mathbf{i}_{ro2}^{r} + \mathbf{i}_{ron}^{r} + \mathbf{i}_{rn.}^{r}$$
(7)

It can be seen that the asymmetrical fault current components are complex, and the influencing factors of the current are many and strongly coupled. Due to the negative sequence component in the rotor voltage, which leads to the DFIG rotor current component also containing a negative sequence component, the magnitude of the fault current amplitude is related to the actual fault voltage drop degree and turndown rate.

# 3 Low voltage protection method with double current limiting circuits

#### 3.1 Resistance characteristics of RSFCL

The resistive superconducting fault current limiter (RSFCL), as a kind of fault current limiting device, has zero resistance value when normal and a high resistance state after being triggering. Because of its good current limiting performance and resistance characteristics (Jiang et al., 2021), it has been applied in the field of power systems in recent years (Khatibi et al., 2022). Assuming the triggering current of RSFCL is  $I_c$ , its resistance characteristics can be represented as

$$R_{\rm SFCL}(t) = \begin{cases} 0 & (t < t_0) \\ R_{\rm m} \left( 1 - e^{-(t - t_0)/\tau_1} \right) & (t_0 < t < t_r) \\ R_{\rm m} e^{-(t - t_r)/\tau_1} & (t > t_r) \end{cases}$$
(8)

where  $R_{\rm m}$  is the maximum resistance in RSFCL triggered state;  $t_0$  and  $t_{\rm r}$  indicate the moment when the current first exceeds and falls below  $I_c$ , respectively;  $\tau_1$  represents the time constant when RSFCL is triggered, which is 0.8–1 ms generally; and  $\tau_2$  denotes the time constants in the RSFCL recovery process, which is approximately 50 ms.

The resistance characteristic corresponding to Eq. 8 is shown in Figure 2. Because of the very short trigger time, RSFCL can generally be considered to conduct transiently during a fault, and this characteristic has the potential to compensate for the delay in the input of the crowbar resistor.

With reference to the application scenario of RSFCL in the power grid, the aforementioned analysis shows that it is feasible to apply RSFCL to the DFIG current limiting circuit, and its advantages can be summarized as follows:

- 1) The transient response characteristics of RSFCL compensate for the delay problem of the traditional crowbar input and limit the rotor overcurrent at the initial stage of faults.
- 2) No interference with the normal operation of the system. Under triggering current  $I_{c}$  RSFCL exhibits zero impedance characteristics, and its impact on the original system is basically negligible.

# 3.2 Construction of DFIG double current limiting circuit and desired goals

The rotor current characteristics during faults vary depending on the degree of voltage drop, and it is hoped that the current limiting circuit will be adaptive to the actual fault current. Combining RSFCL transient response characteristics and multiscenario current limiting objectives, a double current limiting circuit scheme with RSFCL and a controllable crowbar resistor is proposed. The topology is shown in Figure 3.

The double current limiting circuit is constructed around the general control objective: limiting the rotor overcurrent to within 1.6 times the rated current. RSFCL is connected in series to the rotor circuit to compensate for the put-in time delay of crowbar resistance. Specifically, the double current limiting circuit operates as follows:

- Non-serious overcurrent scenarios. It is expected that RSFCL can limit the rotor overcurrent to 1.6 times the rated current target. More importantly, RSFCL can be put into current limiting at the near-instant of fault.
- 2) Serious overcurrent scenarios. In this case, the current limiting ability of RSFCL may be insufficient, and the controllable crowbar resistor input for further current limit. At this stage, the controllable crowbar resistor is mainly further harmonized with the goal of current limiting and DC voltage non-overrun.

# 3.3 Trigger current and resistance setting of RSFCL

The RSFCL trigger current  $I_c$  should be set to meet rapid basic suppression of the rotor overcurrent.  $I_c$  can be set to be greater than the maximum fault current on the rotor side of the DFIG in the event of a single-phase fault on the transmission line.  $I_c$  is given by



$$I_{\rm c} > K_{\rm rel} \cdot \left| \mathbf{i}_{\rm AG}^r \right|_{\rm max},\tag{9}$$

where  $\mathbf{i}_{AG}^{r}$  represents the rotor current when phase A is grounded, and its calculation is carried out according to Eq. 7.  $K_{rel}$  is the setting coefficient, which can be taken as 0.8 to reduce action delay. In fact,  $I_c < 1.6I_N$  should be ensured at the same time, otherwise  $I_c =$ min  $(1.6I_N, K_{rel} \cdot |\mathbf{i}_{AG}^{r}|_{max})$ .

For the resistance setting of RSFCL, consideration should be given to minimizing the dependence on crowbar resistance in scenarios where the rotor overcurrent is not severe. The resistance of RSFCL can be set according to the extreme condition of a single-phase grounding fault accompanied by a system voltage drop of 50%. Extreme refers to the degree of voltage drop, not to the type of fault.

In the event of a single-phase short-circuit ground fault in the grid, the stator three-phase voltage is expressed as

$$U_{s} - U_{s}^{+} + U_{s}^{-} = \frac{1}{3} \left( 3 - \sqrt{3} c_{b} e^{-j30^{\circ}} - \sqrt{3} c_{c} e^{j30^{\circ}} \right),$$
(10)

where  $U_s$  is the terminal voltage;  $U_s^+$  and  $U_s^-$  indicate the terminal positive and negative voltages, respectively; and  $c_b$  and  $c_c$  denote the voltage amplitude drop rates for phases B and C, respectively.

When RSFCL carries out a preliminary current limit, the current limiting circuit exists as  $R_{SFCL} = R' (R' \text{ denotes the total resistance of the current limiting circuit})$ . According to the analyses of Eqs. 3–7, it can be seen that Eq. 11 is satisfied when the current limiting target is set to less than 1.6 times the rated current:

$$\begin{cases} \left| \mathbf{i}_{AG}^{r} \right|_{\max} = \mathbf{i}_{ro1}^{r} + \mathbf{i}_{ro2}^{r} + \mathbf{i}_{ron}^{r} + \mathbf{i}_{rn}^{r} \leq 1.6I_{N} \\ \mathbf{i}_{ro1}^{r} = -\frac{L_{m}}{L_{s}} \frac{sU_{s}^{+}}{js\omega_{s}\sigma L_{r} + R_{r} + R'} e^{js\omega_{s}t} \\ \mathbf{i}_{ro2}^{r} = \frac{L_{m}}{L_{s}} \frac{(2-s)U_{s}^{-}}{j(2-s)\omega_{s}\sigma L_{r} - R_{r} - R'} e^{-(2-s)\omega_{s}t} \\ \mathbf{i}_{ron}^{r} = -\frac{L_{m}}{L_{s}} \frac{(1-s)\left(6 - \sqrt{3}c_{b}e^{-j30^{*}} - \sqrt{3}c_{c}e^{j30^{*}}\right)}{6\left(j\omega_{r}\sigma L_{r} - R_{r} - R'\right)} e^{j\omega_{s}t_{0} - (t-t_{0})/T_{s} - j\omega_{r}t} \\ \mathbf{i}_{rn}^{r} = \left[\mathbf{i}_{AG}^{r}\left(t_{0}\right) - \mathbf{i}_{ro1}^{r}\left(t_{0}\right) - \mathbf{i}_{ro2}^{r}\left(t_{0}\right) - \mathbf{i}_{ron}^{r}\left(t_{0}\right)\right] e^{-t/T_{r}} \end{cases}$$
(11)

To solve for the value of  $R_{SFCL} = R'$ , after assuming the degree of voltage drop in the power grid,  $U_s$ ,  $U_s^+$ , and  $U_s^-$  become known



TABLE 1 Parameters of the switches IGBTs.

Item	Value
Maximum collector–emitter voltage with gate–emitter shorted $(\mathrm{V}_{\mathrm{CES}})$	1,800 (V)
Gate-emitter peak voltage (V <sub>GES</sub> )	± 20 (V)
Collector-emitter saturation voltage (V <sub>CE sat</sub> )	2.2 (V)
Continuous DC collector current (I <sub>CDC</sub> )	6,000 (A)
Turn-on delay time, inductive load $(t_{d on})$	0.33 µs
Turn-off delay time, inductive load $(t_{\rm d\ on})$	0.8 µs

quantities. For the time variable t in Eq. (11), the offline setting is processed as  $t = t_0$ , where  $t_0$  is the assumed fault time. By solving Eq. 11 offline, the setting value of  $R_{SFCL}$  can be obtained.

## 3.4 Implementation and resistance setting of controllable crowbar circuit

The controllable crowbar circuit is shown in Figure 4. The switching of  $R_2$  and  $R_3$  is controlled by two IGBTs, and the resistance value of the input circuit can be equivalently changed by changing the duty ratio of the IGBT. The specific parameters of



the IGBT are shown in Table 1, which are also the parameters of the simulation model described in Section 4.

RSFCL and crowbar bar resistor inputs form a double current limiting circuit and exists as  $R' = R_{SFCL} + R_c$ , where  $R_c$  is the equivalent crowbar resistance.

According to the control objectives, it is generally believed that the peak current value on the rotor side is less than 1.6 times the rated value, and the maximum crowbar resistance  $R_{C \text{max}}$  applied satisfies Eq. 12:

$$\begin{cases} |\mathbf{i}_{r}'|_{\max} \leq 1.6I_{N}, \quad R' = R_{\text{SFCL}} + R_{1} + \frac{R_{2}R_{3}}{R_{2} + R_{3}} \\ R_{1} + R_{2} + R_{\text{SFCL}} \leq R_{\text{Cmax}}, \quad R_{1} + R_{3} + R_{\text{SFCL}} \leq R_{\text{Cmax}}, \qquad (12) \\ R_{\text{Cmax}} = \frac{\sqrt{2} U_{r \max} \omega_{s}}{\sqrt{3.2U_{s}^{2} - 2U_{r \max}^{2}}} \left( L_{s} + \frac{L_{r}L_{m}}{L_{r} + L_{m}} \right) \end{cases}$$

where  $U_{r \max}$  denotes the maximum value of the rotor voltage.

By solving Eq. 12 to get the value of  $R_1$ ,  $R_2$ ,  $R_3$  can realize the setting of crowbar resistance.

In addition to current limiting, controllable crowbar circuits should avoid DC voltage overruns during the current limiting process. For this consideration, during the fault period, the rotor current  $i_r^r$  is measured in real time, and the DC bus voltage constraint is set as shown in Eq.13:

$$\begin{cases} \left| \vec{i}_{r}^{r} \right|_{\max} \left( R_{1} + \frac{R_{2}R_{3}}{H_{1}R_{2} + H_{2}R_{3}} \right) \leq U_{\text{DCmax}} \\ R^{\prime} = R_{\text{SFCL}} + R_{1} + \frac{R_{2}R_{3}}{H_{1}R_{2} + H_{2}R_{3}}, \end{cases}$$
(13)

where  $U_{\text{DCmax}}$  represents the maximum value of the DC bus voltage.

According to Eq. 13, by changing the duty ratio of  $H_1$  and  $H_2$  of the two IGBTs, the corresponding crowbar resistance values are applied to suppress rotor overcurrent.

# 3.5 Implementation of the DFIG double current limiting circuit

Based on the aforementioned analysis, it can be seen that RSFCL can compensate for the put-in time delay of the crowbar circuit. The resistance setting of controllable crowbars is more coordinated with multiple goals. Combining the aforementioned two characteristics, the control strategy of the DFIG double current limiting circuit is constructed in Figure 5.

TABLE	2	Parameter	of	DFIG.
	_		•••	

ltem	Value
Rated rotor current $(I_N)$	1.2 (kA)
Stator resistance (R <sub>s</sub> )	0.0054 (p.u.)
Stator leakage inductance (L <sub>s</sub> )	0.0930 (p.u.)
Rotor resistance (R <sub>r</sub> )	0.0062 (p.u.)
Rotor leakage inductance (L <sub>r</sub> )	0.0998 (p.u.)
Magnetic inductance (L <sub>m</sub> )	3.986 (p.u.)
Slip ratio (s)	-0.2
Stator-rated voltage (U <sub>s</sub> )	690 (V)
Rated power	5 (MW)
Rated DC voltage	1,450 (V)
Maximum DC voltage allowed	1,720 (V)
Rated frequency	50 (Hz)
Rated wind speed	11 (m/s)
Grid connected transformer	0.69/35 (kV)
Rated power factor	1

## 4 Simulation verification

To verify the applicability of the proposed strategy, a 5 MW DFIG simulation model was built in PSCAD, as shown in Figure 3, and the DFIG was connected to the grid via step-up transformers. The other parameters of the DFIG are listed in Table 2. The DFIG operates in constant power factor mode, and the power factor is set to 1, only active power is output during steady-state operation. For steady-state operation, the DFIG uses a dual closed-loop control strategy: an outer power loop and an inner current loop. The control is realized by PI session, and RSC uses the grid voltage directional vector control method (Zhu et al., 2015; Bekiroglu and Yazar, 2022). We assume that a fault occurs at the point of common connection (PCC) at 2 s, with a fault duration of 0.1 s. After the fault, it is triggered according to the fault threshold and switched to LVRT control, which means the crowbar is put in. It should be noted that the relevant protection configurations, operation control methods, and control parameters in the model are set according to the actual project. Therefore, the model can accurately reflect the problems of



conventional crowbar protection and, at the same time, verify the effectiveness of the strategy proposed in this work.

The initial values  $R_{\rm SFCL} = 0.21 \ \Omega$ ,  $R_1 = 0.302 \ \Omega$ ,  $R_2 = 0.168 \ \Omega$ ,  $R_3 = 0.197$ , and  $I_c = 2.6 \ \text{kA}$  are selected.

## 4.1 Rotor current characteristics during faults

AG, AB, ABG, and ABC faults are carried out as examples. The faults are all set at PCC, and the rotor current is analyzed.

According to the theoretical analysis provided in Section 2, the size of the rotor fault current is determined by the type of fault and the depth of voltage drop, with a sudden increase and decaying trend after the fault, which is verified by Figure 6. The rotor current during AG faults is the smallest among all types of faults (Figure 6A) and is essentially equal for AB and ABG faults (Figures. 6B, C). While during three-phase fault, although there is no additional negative sequence component, due to the maximum degree of grid voltage drop, the rotor overcurrent is the most serious and the maximum current is approximately 1.1 times the two-phase fault (Figure 6D).

In order to ensure the current limiting effect, the crowbar resistor is usually set according to the maximum overcurrent, that is, the three-phase fault corresponding to Figure 6D. The traditional method of the crowbar resistance setting is poorly coordinated, which may have a better current limiting effect, but the DC voltage will probably exceed the limit. DC voltage that overruns under conventional protection will be presented in comparison in Section 4.3.

# 4.2 Traditional crowbar protection action characteristics

This section verifies the action characteristics of the crowbar protection when different types of faults occur at PCC. Figure 7 shows the phase-A rotor current waveform,  $t_0$  is the time of fault, and  $t_1$  is the actual input time of the crowbar (the same below). As

the severity of the fault increases (reflected in higher rotor overcurrent), the actual crowbar protection protective action time will be shorter, but not instantaneous.

In the case of AG fault, the crowbar protection delays the action by 8.1 ms; in the ABG fault, the crowbar protection delays the action by approximately 5 ms; and in the ABC fault, the crowbar protection delays the action by approximately 4.2 ms. Non-serious faults correspond to longer crowbar action times than do the serious one. This delay essentially limited by the control system's detection of the fault is actually related to the type of fault, and different fault types have different delay input characteristics. From the shortcircuit current characteristics, it can be seen that the current shows a decaying characteristic, and the short-circuit current is maximum at the instant after the fault. However, due to the input delay of the crowbar resistor, the rotor current cannot be effectively suppressed at the early stage of the fault, which poses a serious threat to the inverter, which is also a problem at present. In actual operations, single-phase faults occupy a larger proportion, and it is more important to face the problem as it is difficult to effectively suppress the overcurrent at the early stage of faults in weak fault scenarios.

## 4.3 Simulation verification of double current limiting circuit

#### 4.3.1 Non-serious fault

The AG fault is set in this section, the voltage at PCC, rotor current, and DC bus voltage are shown in Figure 8, where  $t_0$  is the fault time and  $t_2$  represents the time of completion of RSFCL inputs.

In Figure 8A, the bus voltage drops by approximately 40%, and the drop is relatively slow. In the 2.7 ms after the fault when the RSFCL is input, the first stage of transient current limiting is completed, which satisfies  $t_2 - t_0 = 2.7$  ms. Although this work emphasizes the transient conduction of RSFCL, Figure 8B shows that there is a delay of approximately 2.7 ms during AG fault for the following reasons: first, there is a time constant A (0.8–1 ms) for RSFCL conduction, which is ignored in the analysis in Section 3.1.



FIGURE 7

Traditional crowbar protection action characteristics. (A) Rotor current with the AG fault. (B) Rotor current with the ABG fault. (C) Rotor current with the ABC fault.



#### FIGURE 8

Double current limiting circuit operating characteristics for non-serious fault. (A) Voltage at PCC. (B) Rotor current with AG fault. (C) Voltage of DC capacitor



Double current limiting circuit operating characteristics for serious fault. (A) Voltage at PCC. (B) Rotor current with ABC fault. (C) Voltage of DC capacitor

Second, a short delay is required for the rotor current to develop to Ic. After RSFCL acts, it approximately reduces by 66.7% when compared to the traditional crowbar input time of 8.1 ms, which helps limit the short-circuit current quickly in the early stage of the fault.

As for the voltage of the DC capacitor, in the case of non-serious faults, only RSFCL limits the current, and its resistance is not rectified as harshly as the traditional crowbar rectification. The DC voltage response shown in Figure 8C exhibits two characteristics while meeting the current limiting objective: first, the rapid response, and second, the DC voltage with RSFCL smaller than that with traditional crowbar. The second characteristic becomes more obvious as the severity of the fault increases, which is analyzed in the next section. It should be noted that in considering that the DFIG is generally configured with crowbar protection and rarely without it, the main focus in Figure 8C is to compare the DC voltage of the proposed scheme and the conventional one. The same is true for the serious fault in Section 4.3.2.

#### 4.3.2 Serious fault

The ABC fault set in this section is shown in Figure 9A; the bus voltage drops by approximately 80%, and the voltage drop is fast, with rapid fault development. According to the double current limiting circuit proposed in this work for current limiting, the rotor current waveform is shown in Figure 9B, where ① and ② are the fault moment and time when RSFCL is put into completion, respectively. While RSFCL works, the action time is also shortened by approximately 30%, the rotor current is effectively suppressed at the beginning of the fault, and there is an obvious advantage in the speed of current limiting when compared with the traditional crowbar method. It means that RSFCL can shorten the action time by at least 30% more than the conventional crowbar protection in the early stages of fault, thereby effectively

suppressing the huge increase in rotor current in the early stages of the fault.

As the fault develops, only RSFCL cannot meet the current limiting objective. Therefore, at moment ③, the crowbar circuit in the double current limiting circuit is put into operation. At moment ④, the controlled crowbar circuit adjusts the resistance value for the first time to ensure that the DC capacitor voltage does not exceed the limit.

The DC capacitor is rated at 1.45 kV, and the maximum voltage allowed is 1.72 kV. Under severe ABC fault, DC voltage overruns occur with conventional crowbar protection, as shown in Figure 9C. By contrast, when using the double current limiting circuit proposed in this work, the crowbar resistance is adaptively adjusted under the DC voltage constraint of Eq. 13 to ensure that the DC voltage does not exceed the limit. After the double current limiting circuit is input, the rotor current is gradually reduced. The controllable crowbar resistor lowers the DC voltage by reducing the input resistance value, which further avoids the secondary voltage overrun. The double current limiting circuit has obvious advantages in suppressing the DC voltage overrun.

## 5 Conclusion

To ensure that DFIGs are not cut off from the grid during a fault, DFIGs are often configured with crowbar protection to enhance their LVRT capability. However, conventional crowbar protection configurations face the two following major problems: i) there is a delay in the action of crowbar protection triggered by the current threshold. It is difficult to effectively suppress the short-circuit current that increases in the initial period after a fault, which threatens the safe operation of the rotor and converter. ii) The current after a fault shows a tendency to decay, but the initial value of the fault current is closely related to the fault type. Therefore, the constant resistance of the crowbar is weakly adaptable to different fault types and may face the risk of DC voltage overrun. To address these problems, this work proposes a low voltage protection method of DFIG based on the rotor-side double current limiting circuit. After theoretical analysis and simulation verification, the following conclusions are arrived at:

- The proposed RSFCL current limiting scheme can shorten the input time of the current limiting resistor and effectively limit the rotor overcurrent at the early stage of the fault. This scheme effectively fills the gap of current limiting measures in the early stage of failure. The fast response of the current limiting strategy avoids the impact of large currents on the rotor and converter.
- 2) The controllable crowbar resistor effectively improves the current limiting circuits' resistance value setting problem. DC voltage constraints are constructed to dynamically adjust the resistance of the current limiting circuit to avoid the risk of DC voltage overrun and complete the second stage of current limiting.

The low voltage protection method of DFIG based on the rotor side double current limiting circuit proposed in this work is

good for different fault types. It is well adapted for severe or nonsevere faults. Along with the occurrence of faults, the proposed protection scheme responds quickly, which ultimately reduces the blocking time of RSC and improves the LVRT performance of the DFIG.

## Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material; further inquiries can be directed to the corresponding author.

## Author contributions

HY: methodology, visualization, manuscript writing-original, and manuscript writing-review and editing. CY: project administration, supervision, and manuscript writing-review and editing. YL: formal, investigation, analysis and manuscript writing-review and editing. RM: resources, software, validation, and manuscript writing-review and editing.

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## Conflict of interest

Authors HY, CY, YL, and RM were employed by Jiangsu Frontier Electric Technology Co. Ltd.

The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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