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RECEIVED 15 June 2023

ACCEPTED 24 July 2023

PUBLISHED 08 August 2023

CITATION

Guo C, Xin Z, Han J, Hu L and Lu B (2023),
Review of the calculation of DC-link
capacitor current.
Front. Energy Res. 11:1240755.
doi: 10.3389/fenrg.2023.1240755

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Review of the calculation of DC-link capacitor current

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In the voltage source power electronic converter, DC-link capacitors usually work as buffering elements between the DC and AC sides. The high failure rate and large space occupied by the DC-link capacitors directly affect the reliability and power density of the converters. The analysis and calculation of the DC-link capacitor current is crucial to achieve the refined design of converters. In this work, the analysis and calculation methods of DC-link capacitor current are divided into three categories, according to the calculation principle, namely, simulation method, RMS analysis method, and spectral analysis method, and their calculation methods are summarized. First, the types of capacitors and their characteristics are briefly introduced. Second, the three-phase two-level converter is taken as an example to introduce the basic principles, calculation steps, application scope, advantages, and disadvantages of the latter two methods in detail, as well as the influence of non-ideal factors, such as the output ripple on the calculation results. This work also discusses the calculation of the multi-level converter's DC-link capacitor current spectrum and the current characteristics of multi-phase converters, which are rarely reported. Third, the problem of resonance between the DC-link capacitors and the DC bus inductor is introduced. For the distributed arrangement of multiple DC-link capacitors on DC bus converters, this study proposes a method based on a constant current source equivalent circuit, which can accurately calculate the DC-link capacitor current spectrum that is affected by loop current and resonance. Finally, the current problems and future directions of the DC-link capacitor design are pointed out.

KEYWORDS

DC-link capacitors, current calculation, sizing design, resonance, multi-level converter, multi-phase converter

1 Introduction

With the continuous development of power electronics, the voltage source converter (VSC) is widely used in photovoltaic systems, wind power generation, motor drives, DC microgrids, and so on (Rixin et al., 2008; Yang et al., 2010; Colak et al., 2011; Kumar and Jain, 2014; Watanabe et al., 2016). Since pulse-width modulation (PWM) is usually used on the converter side of the VSC, high frequency harmonics are introduced on the DC side (Dahono et al., 1996; Cross et al., 1999; Kolar and Round, 2006). The DC side usually uses DC-link capacitors as a buffer and voltage regulator, and several typical configurations are shown in Figure 1 (Wang and Blaabjerg, 2014). The main roles of DC-link capacitors include 1) compensating the power pulsation on the AC side and buffering the energy exchange between the AC and DC sides; 2) stabilizing the DC-side voltage and suppressing the voltage harmonics on the DC side; 3) absorbing the current ripple on the DC bus; 4) providing transient power peaks to the load; and 5) absorbing the demagnetization energy of the drive motor in case of an emergency shutdown of the converter (Kolar and Round, 2006; Wang and Blaabjerg, 2014). It can be said that the DC-link capacitors are the most important component observed on the DC side but also one of the components with the highest failure

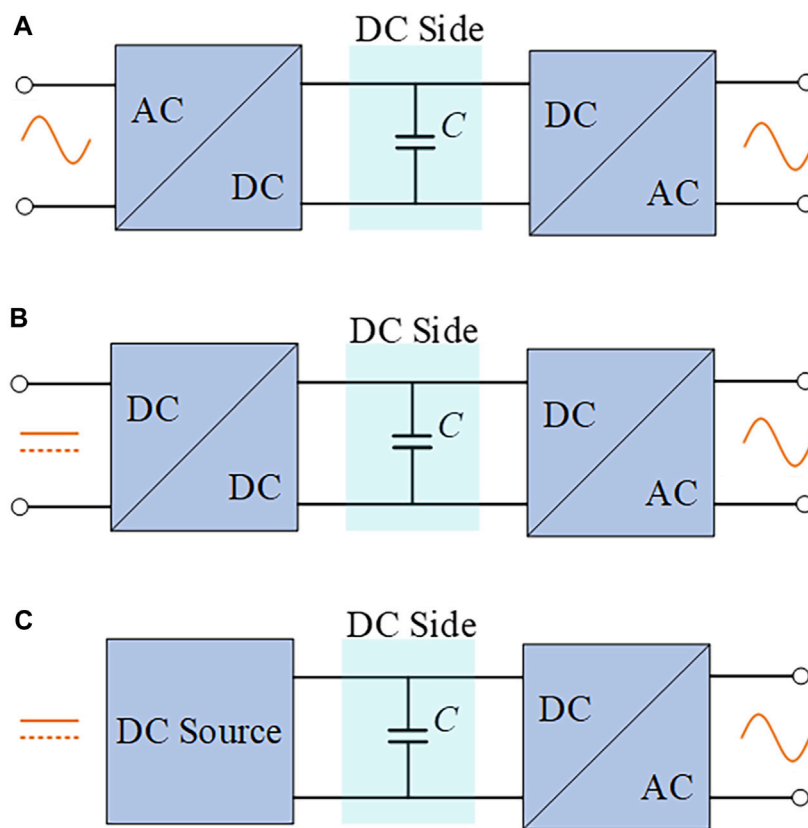


FIGURE 1 Typical configurations of power electronic conversion systems with DC-link capacitors; (A) AC-DC-AC converter, (B) DC-DC-AC converter, and (C) DC-AC converter for the DC power supply.

rate in the power electronic systems (Yang et al., 2011; Wang et al., 2013; Wang and Blaabjerg, 2014). The operating conditions of DC-link capacitors (temperature, humidity, ripple current, and voltage) significantly affect their reliability, and their lifetime estimation has been a hot topic of research (Gasperi, 1996; Gasperi, 2005; Yang et al., 2018; Torki et al., 2023). The literature (Kolar and Round, 2006) states that the operating voltage and especially the operating temperature have a significant effect on the operating life of electrolytic capacitors: the failure rate of an aluminum electrolytic capacitor is reduced to 60% if it operates at 0.9 times of its rated voltage compared to when it operates at the rated voltage; if the operating temperature is reduced, the expected life doubles for every 10°C reduction relative to the rated temperature. The literature (Wang et al., 2018) considers the non-linear process of equivalent series resistance (ESR) growth and capacitance reduction during degradation, and then a non-linear accumulated damage model is proposed to achieve the long-term evaluation of the capacitor life under variable loading conditions. The literature (Delmonte et al., 2020) proposes a procedure based on finite element simulations to compute a thermal model of capacitors, coupling with electrical SPICE simulations to evaluate the maximum operative temperature of capacitors. This method can reduce the damage caused by the overheating of capacitors and increase their service life in practical applications. Therefore, many methods have been proposed by domestic and foreign scholars to reduce the DC-

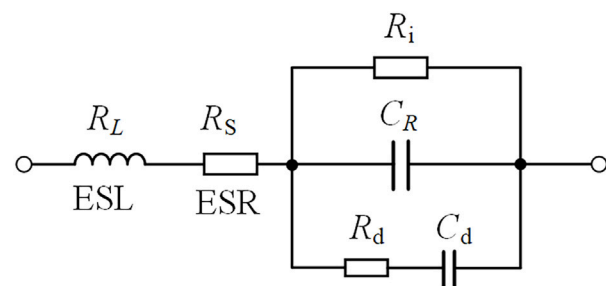


FIGURE 2 Simplified lumped model of capacitors.

side pulsation and heating of the capacitors, such as the optimization of the structure layout and application of new modulation methods to extend the life of DC-link capacitors (Kieferndorf et al., 2004; Su and Tang, 2012; Basler et al., 2015; Diana et al., 2015; Diana et al., 2018; Nie and Schofield, 2019; Yan et al., 2019). In addition, considering that the DC-link capacitors are components that occupy the largest space in a converter system (Huiqing et al., 2012; Ko et al., 2018), in order to improve the converter power density and prevent an increase in system cost, volume, and weight due to overdesigning, the design margin of the DC-link capacitors

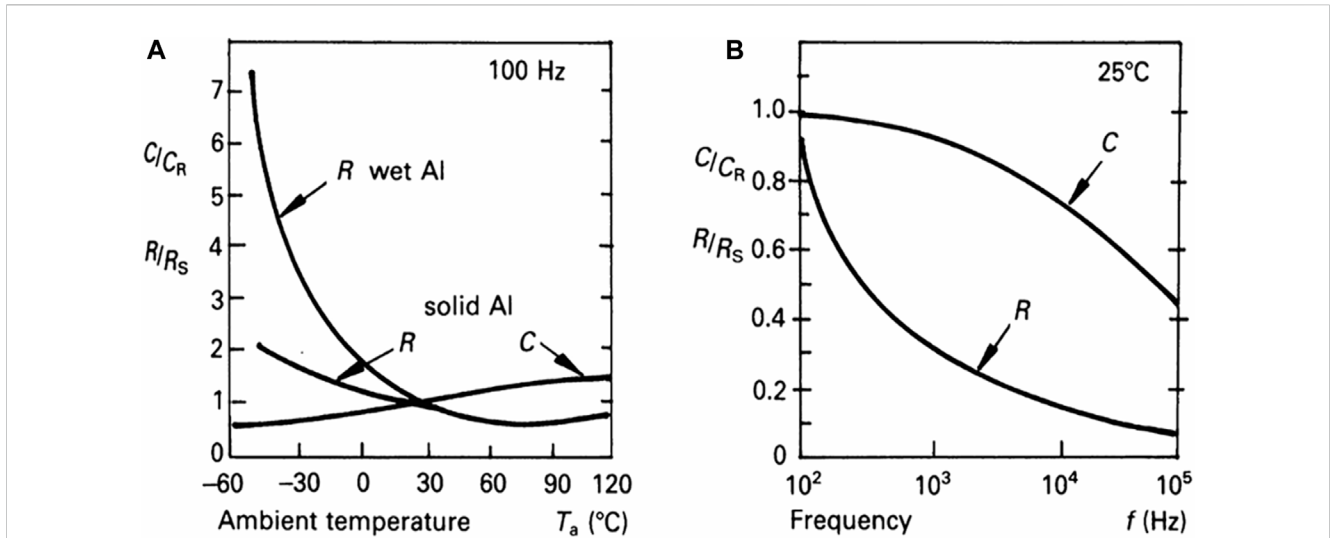


FIGURE 3 Variation of capacitor equivalent circuit parameters with frequency and temperature for 47 μ F and 350 V electrolytic capacitor, respectively (Williams, 1986). (A) Variation of capacitor equivalent circuit parameters with temperature, (B) Variation of capacitor equivalent circuit parameters with frequency.

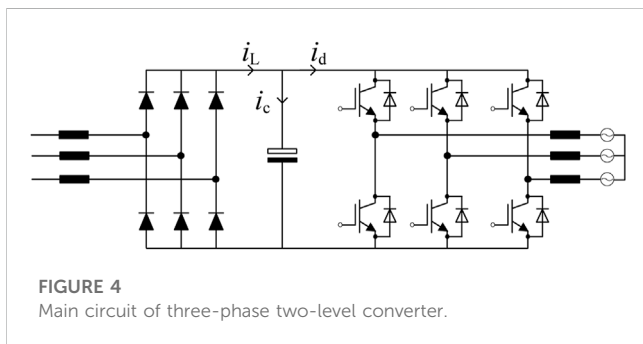


FIGURE 4 Main circuit of three-phase two-level converter.

should be as small as possible while ensuring reliability, which requires a more accurate estimation of the thermal stress of the DC-link capacitors.

The heating of DC-link capacitors is mainly caused by the current flowing through the capacitors and their own ESR (McGrath and Holmes, 2009; Wang and Blaabjerg, 2014). The ESR is an inherent property of the capacitor, so the analysis and calculation of the DC-link capacitor current is the basis of the capacitor design and life prediction, which is an important design to ensure the reliability of the converter. Therefore, the analysis and calculation of the DC-link capacitor current is worthy of an in-depth study in order to meet the minimum fault interval requirement of the converter and also realize the refined design of the system and improve the power density. The existing DC-link capacitor current analysis methods can be divided into three main types as shown in the following sections.

1.1 Simulation method

Simulation can accurately obtain the current waveform flowing through the DC-link capacitors, but in addition to the time required to build the simulation model, each simulation can

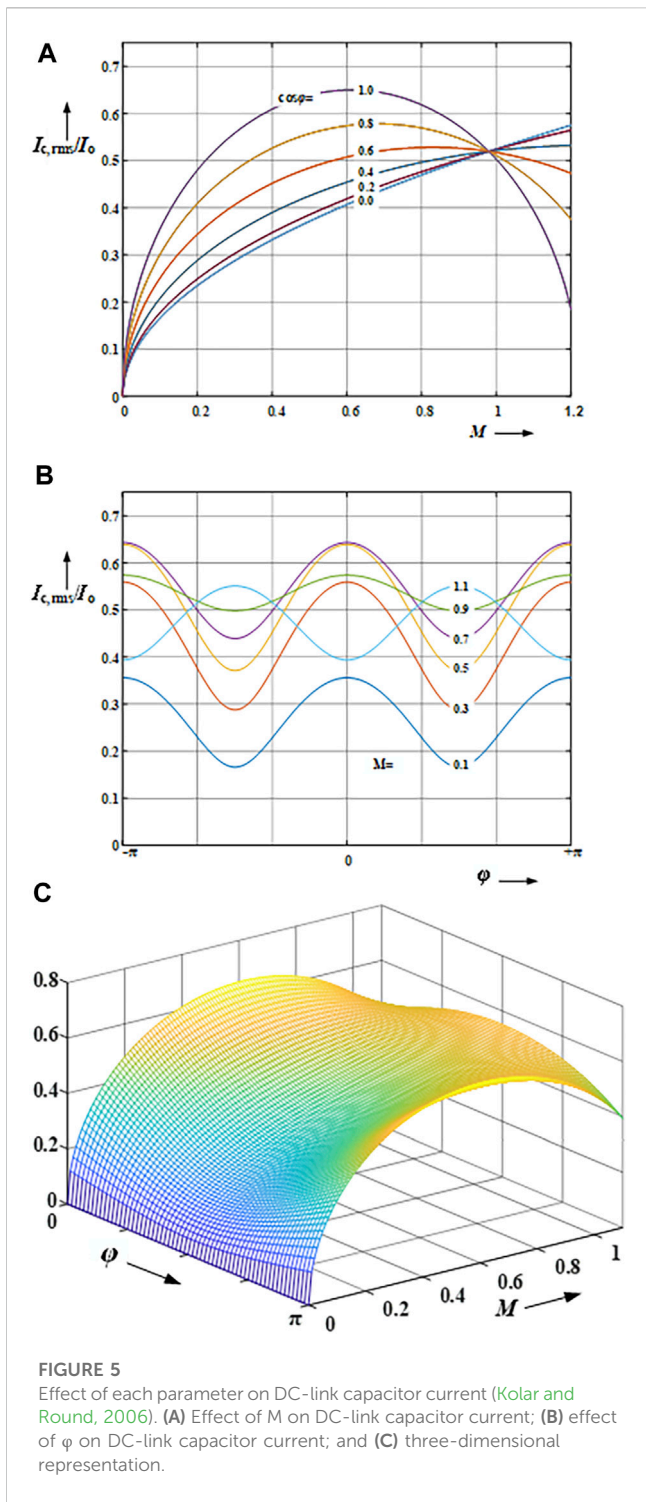
only solve a set of parameters. Besides, it is difficult to figure out the influence that each parameter has on the capacitor current, and it is impossible to establish the functional relationship between the operating point of the converter (determined by the modulation index, amplitude, and phase of the output voltage and current) and capacitor current. The guidance for a practical engineering design is limited.

1.2 Root mean square analysis method

The analytical method generally calculates the RMS of the DC-link capacitor current in the time domain. This method calculates the RMS value of the converter input current by analyzing the mean value and RMS value of the carrier wave period of the converter input current and using the integral in the time domain. When the output ripple on the rectifier side is not considered, the RMS value of the DC-link capacitor current becomes equal to the RMS value of the input current of the converter minus its average value. This method usually ignores the converter output current ripple but still maintains high accuracy and is the most used analysis method nowadays.

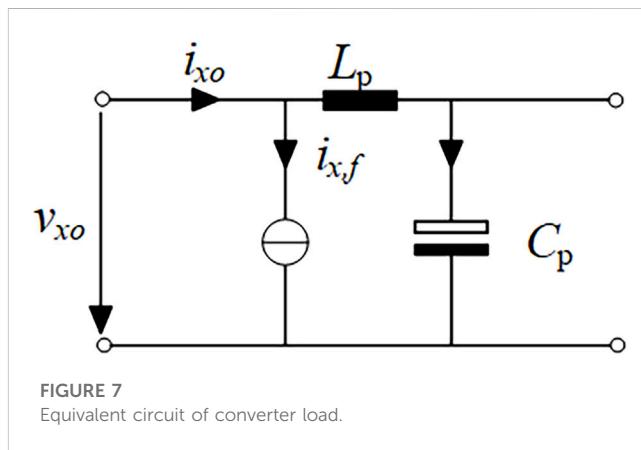
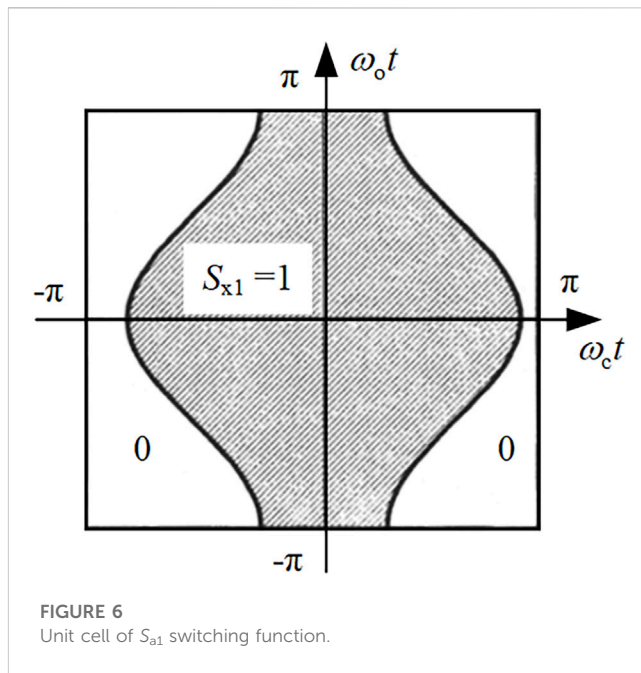
1.3 Spectral resolution method

The ESR of capacitors is sensitive to frequency and temperature, and failure to consider the effects of temperature, voltage, and frequency on the ESR will result in prediction errors (Wang and Blaabjerg, 2014); in order to calculate the heating of DC-link capacitors more accurately, it is sometimes necessary to calculate the spectrum of the capacitor current. The double Fourier analysis is the basis for calculating the DC-link capacitor current spectrum. This method is more complex than that of calculating current RMS values, but after obtaining the capacitor current

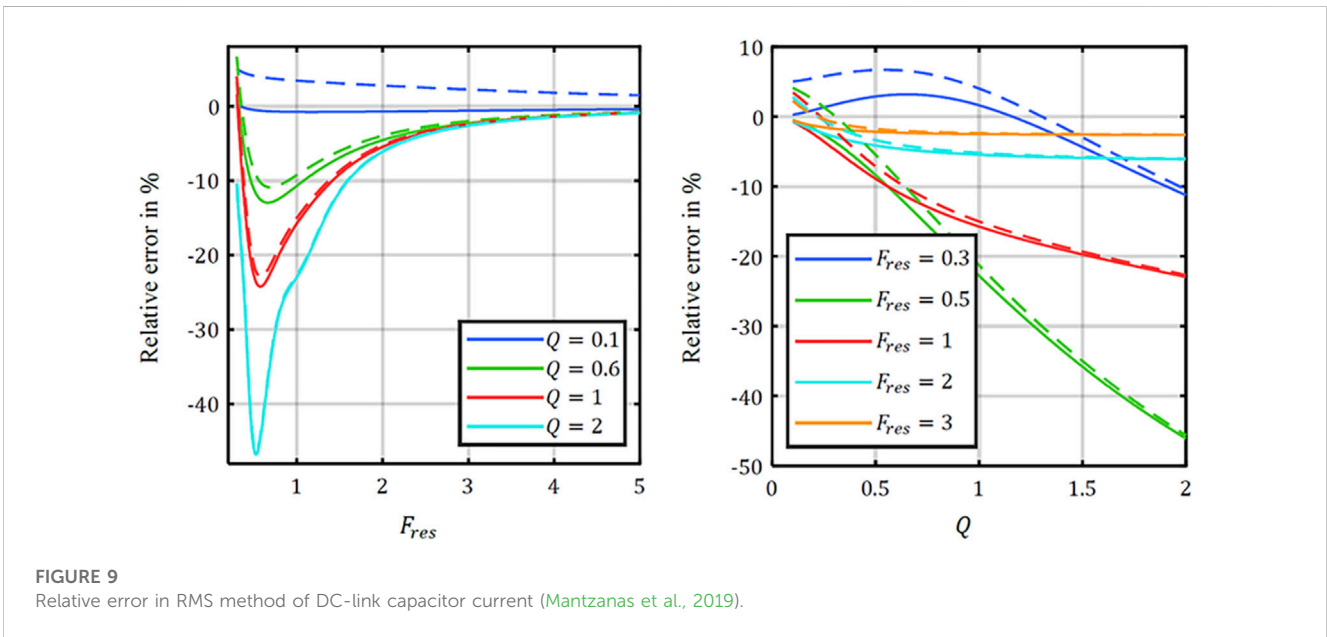
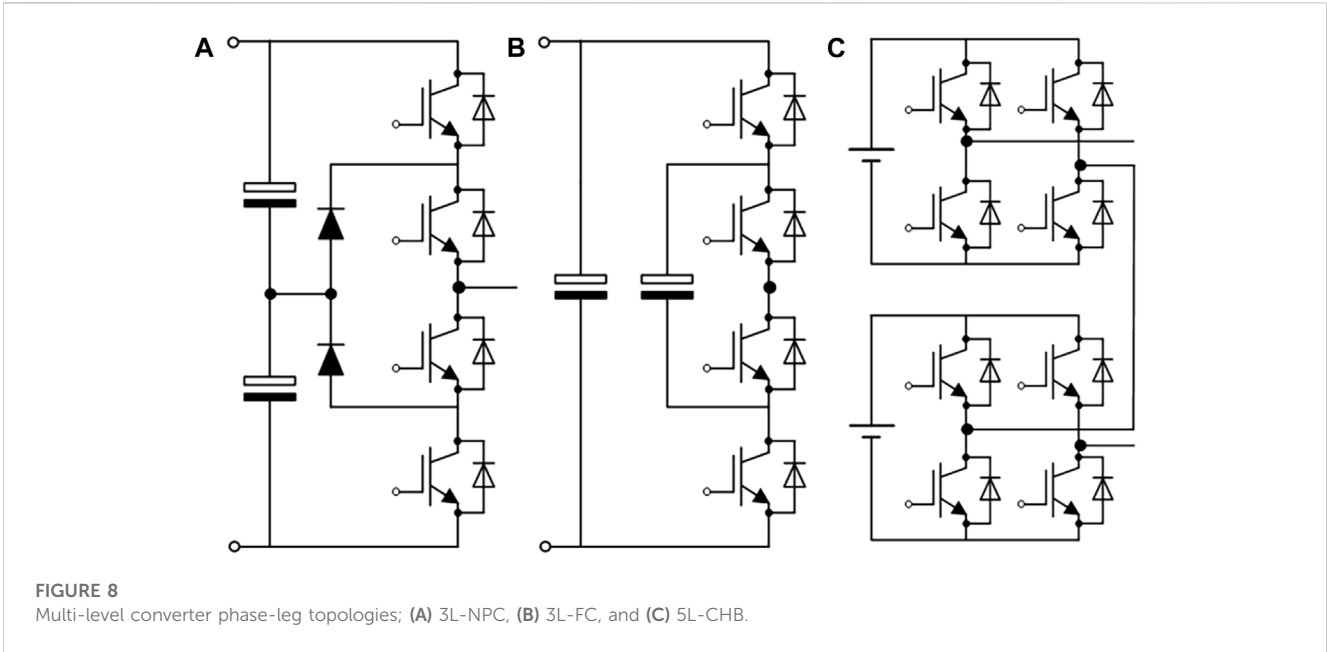


spectrum (harmonic resolution), the frequency and temperature can be taken into account in the temperature calculations of the capacitors according to the ESR model of the capacitors and thermal stress can be estimated more accurately.

This article will first introduce the types and characteristics of DC-link capacitors, and then introduce the RMS analysis method and the spectral analysis method in detail. The common characteristics of the DC-side DC-link capacitor current with each parameter will be analyzed by using the RMS analysis



method, and the effects of the output current ripple and diode reverse recovery on the DC-link capacitor current will be introduced. The harmonic analysis method is then introduced, and the rarely reported calculation method of the DC-link capacitor current for multi-level converters and the characteristics of capacitor current for multi-phase converters are further discussed. Meanwhile, considering the rapid development of new energy industries and wide application of advanced motor drive systems, converters with a distributed arrangement of multi-phase or multiple DC-link capacitors have been gradually adopted. In this arrangement, multiple DC-link capacitors may resonate with the DC bus spurious parameters, which greatly affect the accurate calculation results of the DC-link capacitor current. In this work, a method to analyze the resonance characteristics of distributed multi-capacitor systems is proposed, and a method to analyze and calculate the spectrum of distributed DC-link capacitor current, considering the effect of resonance, is proposed. Finally, an outlook on the method of DC-link capacitor current analysis and calculation is given.

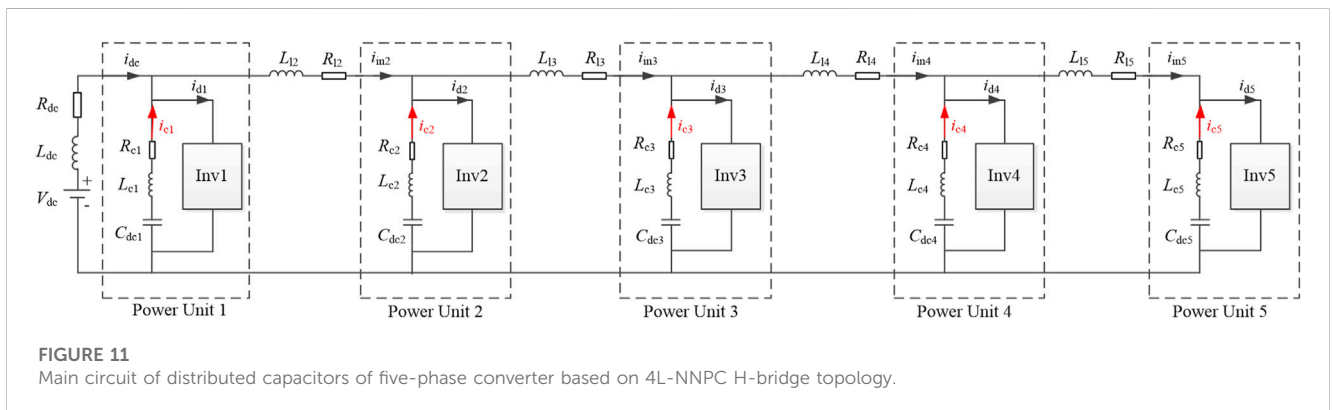
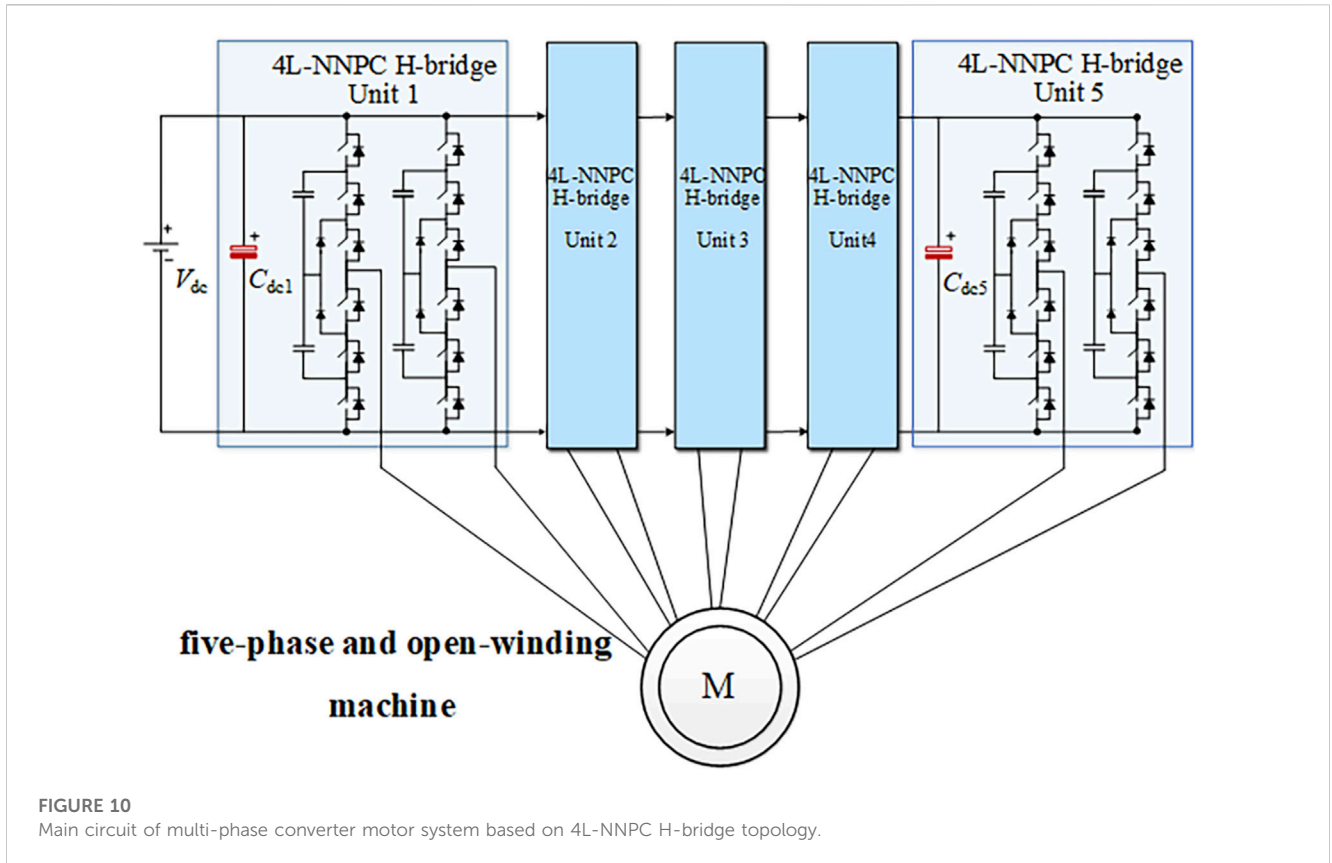


2 DC-link capacitors

Capacitors that are used as DC-link capacitors are usually of three types, namely, aluminum electrolytic capacitors, metallic polypropylene film capacitors, and ceramic capacitors (Williams, 1986; Wang and Blaabjerg, 2014). Each one of these three types of capacitors has its own characteristics and is suitable for different applications. Aluminum electrolytic capacitors have the highest energy density and lowest energy loss but have relatively large ESR and wear problems due to electrolyte evaporation (Gasperi, 2005). Metallic polypropylene film capacitors use plastic films as dielectric material and have good AC characteristics with small size,

wide frequency range, and operating temperatures up to 200°C but are relatively expensive and suitable for high current ripple applications (Huiqing et al., 2012). Ceramic capacitors are suitable in high-power and high-frequency switching power supplies with small size, low cost, and more balanced performance. In general engineering applications, converter systems for driving motors mostly use aluminum electrolytic capacitors (Huiqing et al., 2012).

The equivalent circuit model of the capacitor is shown in Figure 2, where C_R is the capacitance; R_S is the series equivalent resistance ESR determined by the lead and junction resistance; L_S is the series equivalent series inductance (ESL) caused by the structure



and supply line, which can be neglected at lower frequencies. R_i is the insulation resistance, which is usually large; R_d is the dielectric loss equivalent resistance caused by dielectric absorption and molecular polarization; and C_d is the inherent dielectric absorption capacitance, both of which usually need to be considered only in electrolytic capacitors operating at high frequencies.

The equivalent circuit parameters of the capacitor vary with the operating temperature, voltage stress, and frequency, as shown in Figure 3 (Williams, 1986). Failure to consider these variations will lead to incorrect calculations of electrical and thermal stresses in the capacitor and affect the accuracy of reliability estimation. Therefore, the accuracy of life estimation based on the harmonic spectrum of the current flowing through DC-link capacitors is higher during the refinement of the DC-link capacitor design.

2.1 Calculating RMS value of DC-link capacitor current

Calculating the capacitor current RMS value is a relatively quick and intuitive method, in which the calculation process is easy to understand, the physical meaning is clearer, and it is widely used in applications that do not require high accuracy in estimating capacitor heating (Kolar and Round, 2006; Kai et al., 2016). The following is an example of the most common three-phase two-level converter to introduce its calculation process.

The main circuit of the three-phase two-level converter is shown in Figure 4. The converter side uses space vector modulation (SVM) with two levels per phase bridge arm and

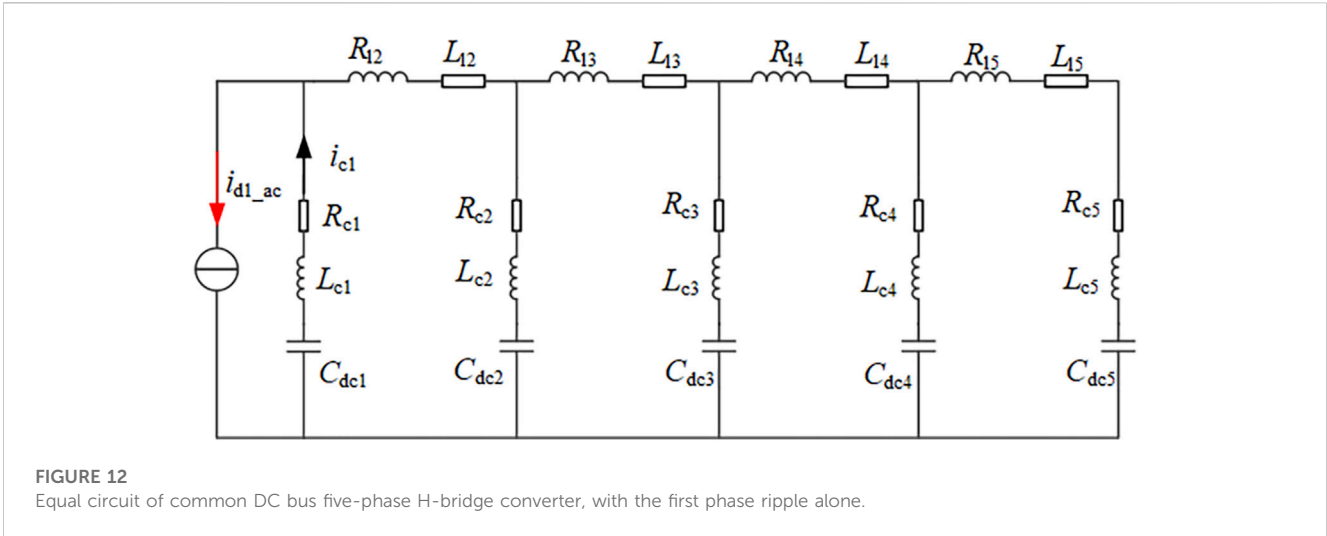


FIGURE 12 Equal circuit of common DC bus five-phase H-bridge converter, with the first phase ripple alone.

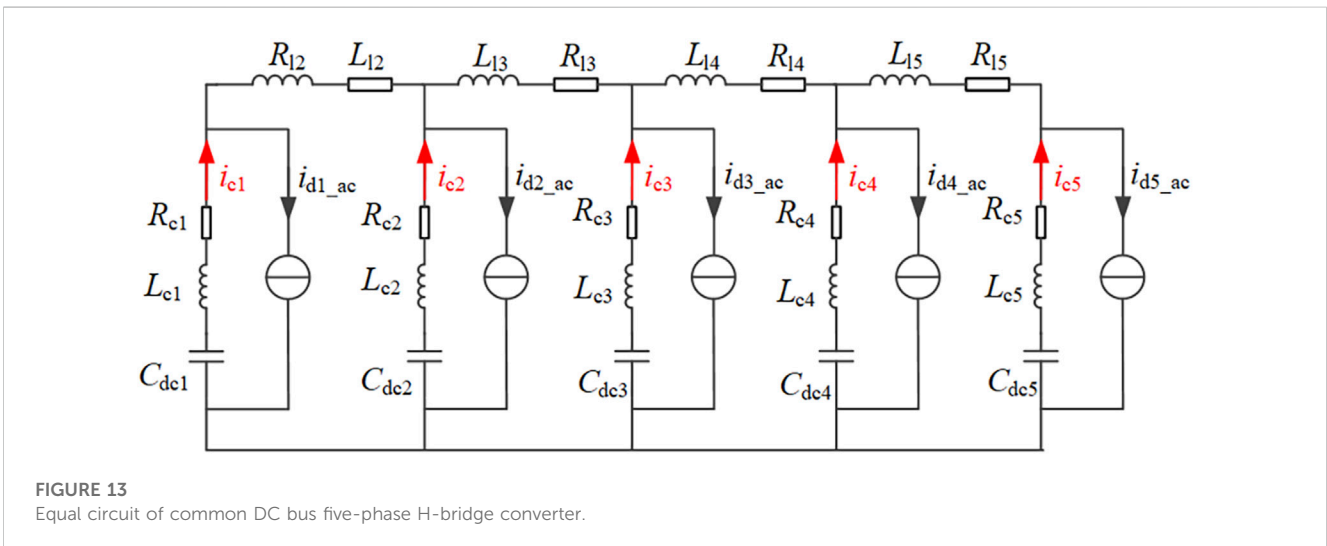


FIGURE 13 Equal circuit of common DC bus five-phase H-bridge converter.

$2^3 = 8$ states in total for the three phases. The reference voltage vector \vec{V}_{ref} can be expressed as

$$\vec{V}_{ref} = V_{ref} e^{j\omega t}, \tag{1}$$

where V_{ref} is the reference voltage amplitude, ω is the rotational angular velocity, and the modulated carrier wave period is T_s .

When the reference vector is in sector 1, in order to minimize the number of switch actions, the vector synthesis in one carrier wave period is

$$\begin{aligned} \vec{V}_0 [000] \rightarrow \vec{V}_1 [100] \rightarrow \vec{V}_2 [110] \rightarrow \vec{V}_0 [111] \rightarrow \vec{V}_0 [111] \\ \rightarrow \vec{V}_2 [110] \rightarrow \vec{V}_1 [100] \rightarrow \vec{V}_0 [000], \end{aligned} \tag{2}$$

where $\vec{V}_0 [000]$ means that the switching functions S_a , S_b , and S_c of the voltage vector \vec{V}_0 are all equal to zero, and the action times of the vectors \vec{V}_1 and \vec{V}_2 are

$$t_{v1} = \frac{\sqrt{3}T_s V_{ref}}{V_{dc}} \sin\left(\frac{\pi}{3} - \theta\right), \tag{3}$$

$$t_{v2} = \frac{\sqrt{3}T_s V_{ref}}{V_{dc}} \sin \theta. \tag{4}$$

The upper and lower switching signals of the bridge arm on the converter side are complementary. From the circuit in Figure 4, it can be seen that the input current i_d on the converter side is determined by the AC load current together with the switching state of the three-phase switching tubes. Using the switching function to express the state of the switching tube, the switching function is 1 or 0, where 1 means the switching tube is turned on and 0 means it is turned off, and at this time, the expression of the converter side DC bus input current i_d is

$$i_d = S_{a1} i_a + S_{b1} i_b + S_{c1} i_c, \tag{5}$$

where S_{x1} ($x = a, b, c$) are the switching functions of the tubes on the three-phase bridge arm; i_x is the AC output current of the three-phase converter bridge.

Since converters usually carry inductive loads such as motors, their output current ripple is relatively small, and the ripple can

TABLE 1 Parameters of the five-phase H-bridge.

Circuit parameter	Amplitude
DC voltage V_{dc}	10 kV
Output current amplitude I_o	100 A
Modulation ratio M	0.8
Base wave frequency f_o	50 Hz
Carrier ratio N	50
Power factor $\cos\Phi$	0.85
DC-link capacitors C	1200 μ F
Line resistance on the DC bus R_l	4 m Ω
Line inductance on the DC bus L_l	1 mH
Series equivalent resistance of DC-link capacitors R_c	1.4 m Ω
Series equivalent inductance of DC-link capacitors L_c	60 nH
DC power supply internal resistance R_{dc}	10 m Ω
DC power supply internal inductance L_{dc}	100 μ H

usually be neglected and treated as a standard sinusoidal waveform. The literature (Kolar and Round, 2006) explored the effects of ignoring/not ignoring the output current ripple on the solution results and pointed out that the difference between the calculated results of the DC-link capacitor current does not exceed 8%. For a three-phase balanced load, in neglecting the load current ripple, the load current satisfies Eq. 6:

$$\begin{cases} i_a = \sqrt{2} I_o \sin(\omega t + \varphi) \\ i_b = \sqrt{2} I_o \sin\left(\omega t - \frac{2}{3}\pi + \varphi\right), \\ i_c = \sqrt{2} I_o \sin\left(\omega t - \frac{4}{3}\pi + \varphi\right) \end{cases} \quad (6)$$

$$i_a + i_b + i_c \equiv 0, \quad (7)$$

where I_o is the RMS value of the load current. According to the aforementioned analysis, the average value of the input current on the converter side over half a carrier wave period is

$$i_{d,avg} = \int_0^{\frac{1}{2}T_s} i_d dt = (t_{V1}i_a - t_{V2}i_c)/T_s. \quad (8)$$

In Eqs 3, 4, θ represents the angle between the reference vector and the a -axis, and $\theta = \omega t - \frac{1}{2}\pi$ (Kolar and Round, 2006). Therefore, we substitute Eqs 3, 4, 6 into Eq. 8 to obtain

$$i_{d,avg} = \frac{\sqrt{6}I_o T_s V_{ref} \cos(\omega t) \cos\left(\frac{\pi}{6} + \varphi + \omega t\right) + \sqrt{6}I_o T_s V_{ref} \sin(\varphi + \omega t) \sin\left(\frac{\pi}{6} + \omega t\right)}{V_{dc} T_s}. \quad (9)$$

Further simplifying it to

$$\begin{aligned} i_{d,avg} = I_{d,avg} &= \frac{\sqrt{6}I_o T_s V_{ref} \cos\left(\varphi - \frac{\pi}{6}\right) + \sqrt{6}I_o T_s V_{ref} \cos\left(\frac{\pi}{6} + \omega t\right)}{2V_{dc}} \\ &= \frac{3\sqrt{2}}{4} I_o M \cos \varphi, \end{aligned} \quad (10)$$

where $M = 2V_{ref}/V_{dc}$. For a three-phase balanced load, the average value of the input current on the converter side of its converter is a constant over half a carrier wave period, which is only related to the modulation index and load and is independent of the carrier wave frequency. From the harmonics point of view, i_d contains no lower harmonic component except for the DC component and the carrier harmonic component.

The RMS value of i_d within half a carrier wave period satisfies

$$i_{d,rms}^2 = \int_0^{\frac{1}{2}T_s} i_d^2 dt = \frac{(t_{V1}i_a^2 - t_{V2}i_c^2)}{T_s}. \quad (11)$$

Due to the symmetry of the three-phase converter, the RMS value of the i_d over the fundamental period is obtained by integrating over a sector ($\pi/3$):

$$I_{d,rms}^2 = \frac{3}{\pi} \int_0^{\frac{\pi}{3}} i_{d,rms}^2 d\varphi, \quad (12)$$

and solving to get

$$I_{d,rms} = I_o \sqrt{\frac{2\sqrt{3}}{\pi} M \left(\frac{1}{4} + \cos^2 \varphi\right)}. \quad (13)$$

According to the circuit shown in Figure 4, the converter-side input current i_d , the DC-link capacitor current i_c , and the rectifier-side output current i_L are satisfied with the following:

$$i_c = i_d - i_L. \quad (14)$$

When the ripple of the rectifier output current is not considered, i_L contains only the DC component, whose magnitude is the same as the DC component $I_{d,avg}$ of the input current on the converter side. According to Parseval's theorem, the RMS value of the DC-link capacitor current at this time satisfies the following:

$$I_{c,rms}^2 = I_{d,rms}^2 - I_{d,avg}^2. \quad (15)$$

By substituting Eqs 10, 13 into Eq. 15 we obtain

$$I_{c,rms} = I_o \sqrt{2M \left[\frac{\sqrt{3}}{\pi} + \cos^2 \varphi \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} M \right) \right]}. \quad (16)$$

When considering the current ripple obtained by the rectifier side, the input current i_d on the converter side and output current i_L on the rectifier side can be expressed as follows:

$$i_d = I_{d,avg} + i_{d,ac}, \quad (17)$$

$$i_L = I_{L,avg} + i_{L,ac}, \quad (18)$$

where $i_{d,ac}$ is the AC component of the input current on the converter side, $I_{L,avg}$ is the DC component of the output current on the rectifier side, and $i_{L,ac}$ is its AC component. Equation 14 can be simplified as follows:

$$i_c = i_{d,ac} - i_{L,ac}. \quad (19)$$

The relationship between the frequency and phase of each harmonic of $i_{d,ac}$ and $i_{L,ac}$ will affect the RMS value of i_c . According to the Cauchy-Schwarz inequality, the RMS value of the aforementioned equation satisfies the relationship.

$$I_{c,rms} \leq I_{d,ac,rms} + I_{L,ac,rms}. \quad (20)$$

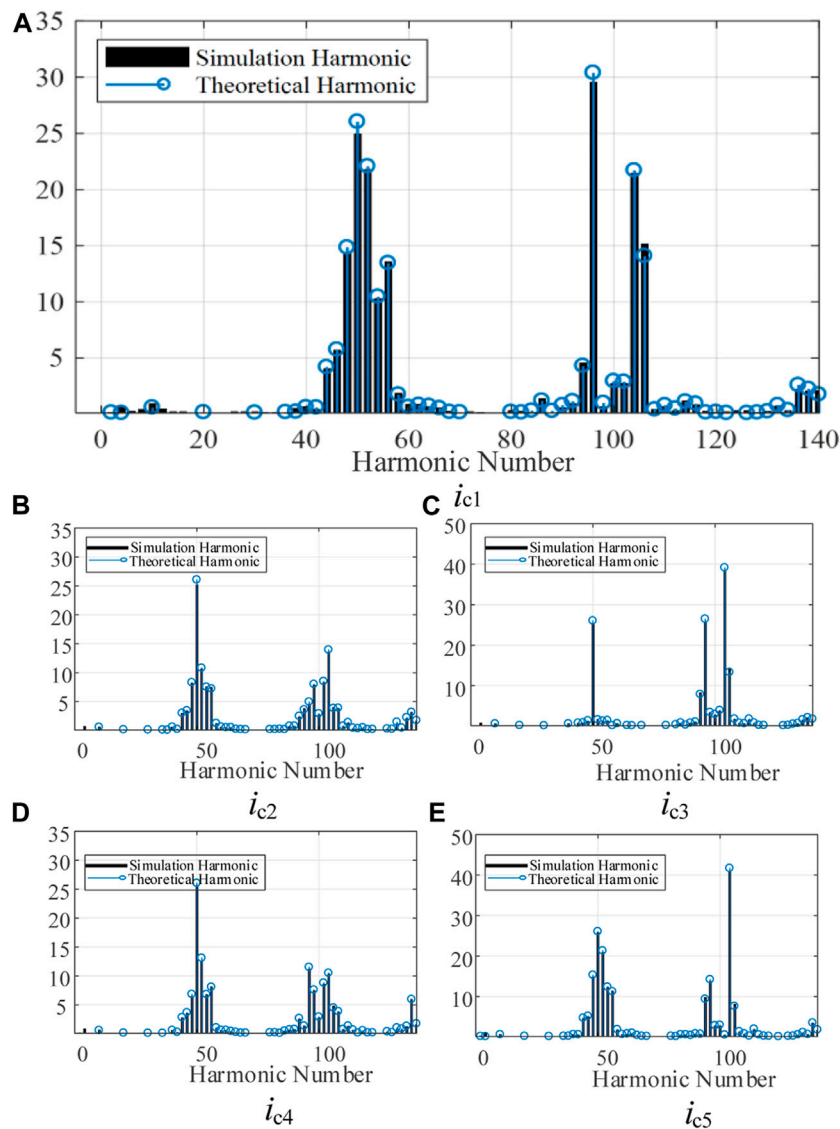


FIGURE 14 Comparison of simulation and theoretical result of harmonic spectra of DC-link capacitor current i_{c1} – i_{c5} . (A) Comparison of harmonic spectra of i_{c1} , (B) Comparison of harmonic spectra of i_{c2} , (C) Comparison of harmonic spectra of i_{c3} , (D) Comparison of harmonic spectra of i_{c4} , (E) Comparison of harmonic spectra of i_{c5} .

Equation 20 represents the worst-case maximum RMS value of the DC-link capacitor current.

2.1.1 Analysis of calculation results

According to Eq. 16, the RMS value of the DC-link capacitor current can be considered a function related to the load current and modulation index. When $\cos\varphi$ is close to 1, $I_{c,rms}$ is maximum when

$$M_{I_{c,max}} = \frac{8\sqrt{3}}{9\pi} \left(1 + \frac{1}{4\cos^2\varphi} \right) \approx 0.61. \quad (21)$$

According to Eq. 10, i_d has no DC component when $\cos\varphi$ is close to 0. The DC-link capacitor current $I_{c,rms}$ in Eq. 16 increases with the modulation index M . The ratio of its effective value to the load current ($I_{c,rms}/I_o$) is approximately proportional to \sqrt{M} .

When the modulation index M is close to

$$M = \frac{16\sqrt{3}}{9\pi} \approx 0.98, \quad (22)$$

$\cos\varphi$ in Eq. 16 is approximately dropped, and the value of $I_{c,rms}$ is largely independent of φ .

Figure 5 shows the relationship between the ratio of the RMS values of the DC-link capacitor current and load current ($I_{c,rms}/I_o$) with each parameter. As can be seen in Figure 5A, $I_{c,rms}/I_o$ approaches its peak (extreme value) when M is close to 0.6; and when $\cos\varphi = 0$, $I_{c,rms}/I_o$ no longer exhibits the extreme value characteristic but increases monotonically with M , and it is approximately proportional to \sqrt{M} . As can be seen in Figure 5B, when M is close to 0.98, the value of $I_{c,rms}/I_o$ has a weak relationship with φ , and its amplitude fluctuates very little with changes in φ .

The aforementioned analysis of the relationship between the DC-link capacitor current and variables is for the three-phase two-

TABLE 2 Comparison of the simulation and theoretical results of the RMS value of the DC-link capacitor current.

Capacitor current RMS	Phase 1 I_{c1_rms} (A)	Phase 2 I_{c2_rms} (A)	Phase 3 I_{c3_rms} (A)	Phase 4 I_{c4_rms} (A)	Phase 5 I_{c5_rms} (A)
Simulation result	43.53	34.39	44.29	34.84	46.35
Theoretical calculation	43.89	34.39	44.57	34.98	46.70

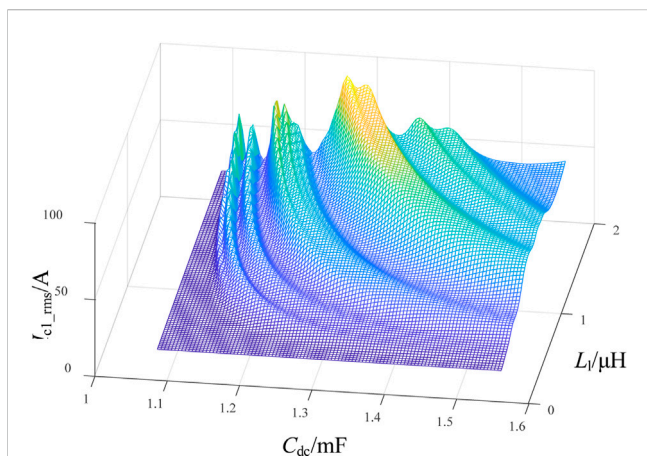


FIGURE 15 RMS value of first phase DC-link capacitor current with different capacitance C and DC bus inductance L_1 ($R_c = 1.4$ mΩ and $R_l = 4$ mΩ).

level converter topology, but the laws and trends of this relationship are also applicable to other conventional multi-phase and multi-level converter structures, where only the ratio and amplitude of the parameters between the corresponding variables are different. The correctness of the calculation results can initially be judged according to the corresponding trends in practical engineering.

2.1.2 Development of current RMS calculation

On the basis of the aforementioned calculation methods, domestic and foreign scholars have also optimized many of these and expanded new application areas. The literature (Pei et al., 2015; Li and Jiang, 2018) provides a more accurate analytical solution for the RMS value of the DC-link capacitor current, considering the ripple of the load current, and showing the calculation result that the load current ripple will increase the peak DC current, but its expression involves several AC side parameters and the result is more complicated. In the literature (Welchko, 2007), the RMS value of the DC-link capacitor current of a three-phase two-level converter after eliminating the common-mode voltage is calculated by analyzing the vector synthesis method, and the results show that the elimination of the common-mode voltage leads to an increase in the DC-link capacitor current to 1.3–2 times that of the original one. In the literature (Guo et al., 2018), the converter shunt diode reverse recovery problem was considered and the method for solving the RMS value of the DC-link capacitor current was optimized by considering more factors that affect the calculation results, such as the switching frequency of the converter, reverse recovery time, and current of the inverse shunt diode.

It should be noted that no matter how accurately the RMS value of the DC-link capacitor current is calculated, the method has its unavoidable limitation that the amplitude of each harmonic of the

capacitor current is not available. This will seriously affect the accuracy of the results when calculating the capacitor heating, and the error will exceed the impact of the output current ripple, diode reverse recovery time, and other factors on the heating calculation.

2.2 Calculation of DC-link capacitor current spectrum

Considering that the equivalent circuit parameters of capacitors are related to the operating temperature, voltage stress, and frequency, in order to estimate and calculate electrical and thermal stresses of capacitors more accurately, the current harmonic spectrum flowing through the DC-link capacitors has to be calculated for a more accurate estimation of heat generation in engineering. The current ripple on the DC side of the converter is observed as being caused by the PWM modulation strategy, and the current analysis of the PWM strategy mainly uses the double-Fourier analysis (Holmes, 1998; Moynihan et al., 1998; McGrath and Holmes, 2002).

2.2.1 Double-Fourier analysis

By continuing to use the three-phase two-level converter shown in Figure 4 as an example, the process of calculating the harmonic expression for the DC-link capacitor current using the double-Fourier analysis is described. Assuming a SPWM strategy at the converter side, we set the time variable as follows:

$$\begin{aligned} x(t) &= \omega_c t + \theta_c \\ y(t) &= \omega_o t + \theta_o \end{aligned} \tag{23}$$

where ω_c and ω_o are the carrier wave angular frequency and modulating wave angular frequency, respectively. θ_c and θ_o are the initial phase angles of the carrier and modulating waves, respectively. The switching function S_{x1} of the upper switching tube of a bridge arm on the converter side can be expanded into a double-Fourier series form as

$$\begin{aligned} S_{a1}(x, y) &= \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n} \cos(ny) + B_{0n} \sin(ny)] \\ &+ \sum_{m=1}^{\infty} [A_{m0} \cos(mx) + B_{m0} \sin(mx)] \\ &+ \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} [A_{mn} \cos(mx + ny) + B_{mn} \sin(mx + ny)], \end{aligned} \tag{24}$$

where

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} S_{a1}(x, y) e^{j(mx+ny)} dx dy. \tag{25}$$

TABLE 3 Comparison of DC-link capacitance current analysis methods.

DC-link capacitor current analysis method	Advantage	Disadvantage	Range of application
Simulation method	High accuracy	Difficulty in modeling	Less used
RMS analysis method	Small calculation volume; relatively high accuracy	Cannot show the effect of current spectrum	Most used
Spectral resolution method	High accuracy; shows the effect of current spectrum	More complex	Less used
Method based on a constant current source equivalent circuit	High accuracy; considers the resonance	High computational effort; difficulty in obtaining resonance parameters	Newly proposed; distributed DC-link capacitor current calculation

To simplify the expression, the modulated signal is expressed in the cosine form:

$$v_x = M \cos(\omega_o t + \theta_{ox}), \tag{26}$$

where θ_{ox} denotes the initial phase of the phase x ($x = a, b, c$) modulated wave. According to the relationship between the carrier and modulating wave, the unit element of the switching function S_{x1} can be obtained as shown in Figure 6.

The boundary of the unit cell shown in Figure 6 specifies the range of integration defined in Eq. 25, and it is only in this range that the switching function $S_{a1} = 1$ and Eq. 25 are rewritten as

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\frac{\pi}{2}(1+M\cos y)}^{\frac{\pi}{2}(1+M\cos y)} e^{j(mx+ny)} dx dy. \tag{27}$$

We solve the equation

$$S_{x1} = \frac{1}{2} + \frac{M}{2} \cos(\omega_o t + \theta_{ox}) + \frac{2}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} J_0\left(m \frac{\pi}{2} M\right) \sin m \frac{\pi}{2} \cos(m[\omega_c t + \theta_c]) + \frac{2}{\pi} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} \frac{1}{m} J_n\left(m \frac{\pi}{2} M\right) \sin\left([m+n] \frac{\pi}{2}\right) \times \cos(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_{ox}]). \tag{28}$$

and since the carrier phase angle is the same for all three half-bridge arms at any moment, for the convenience of calculation, the carrier phase angle θ_c is set to zero in the above equation, and the initial phase angles of the three modulated waves differ from each other by 120°:

$$\theta_{ax} = 0, \theta_{bx} = -2/3\pi, \theta_{cx} = -4/3\pi. \tag{29}$$

Assuming that the converter output current is a three-phase symmetric sine wave, for the convenience of calculation, Eq. 6 is expressed in the cosine form, and Eqs 6, 28 are taken into Eq. 5 to obtain the harmonic expression for the input current i_d on the converter side as follows:

$$i_d(t) = S_{a1}(t) \times I_o \cos(\omega_o t + \varphi) + S_{b1}(t) \times I_o \cos\left(\omega_o t - \frac{2}{3}\pi + \varphi\right) + S_{c1}(t) \times I_o \cos\left(\omega_o t - \frac{4}{3}\pi + \varphi\right). \tag{30}$$

The aforementioned equation can be reduced to a convolution integral in the frequency domain (McGrath and Holmes, 2009) or solved directly by using the prosthaphaeresis, and the result is

$$i_d(t) = \hat{A}_{00} + \sum_{n=1}^{\infty} [\hat{A}_{0n} \cos(2n\omega_o t) + \hat{B}_{0n} \sin(2n\omega_o t)] + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} [\hat{A}_{mn} \cos(m\omega_c t + 2n\omega_o t) + \hat{B}_{mn} \sin(m\omega_c t + 2n\omega_o t)], \tag{31}$$

where

$$\begin{aligned} \hat{A}_{00} &= \frac{1}{2} I_o A_{01} \cos \varphi = \frac{M}{4} I_o \cos \varphi, \\ \hat{A}_{mn} &= \frac{1}{2} I_o (A_{m,n-1} + A_{m,n+1}) \cos \varphi, \\ \hat{B}_{mn} &= -\frac{1}{2} I_o (A_{m,n-1} - A_{m,n+1}) \sin \varphi. \end{aligned} \tag{32}$$

The purpose of using the cosine form to express the modulating signal and output current on the converter side of the converter is to simplify the double-Fourier integral equation; except for the initial phase difference of $\pi/2$ of the modulating waveform, the connotations of using the sine and cosine forms are exactly equivalent. When using the sine form expression in Eq. 6, the solution results will not be any different, except that Eqs 24, 31 will be slightly more complicated.

According to Eq. 1, the DC-link capacitor current i_c is equal to the DC-side input current i_d minus the rectifier-side output current i_L . When the rectifier-side current ripple is not considered, i_c is equal to i_d , excluding its DC component.

$$i_c = i_d - I_{d,dc}. \tag{33}$$

The spectrum of the DC-link capacitor current is obtained by Eq. 33.

With $I_{d,h,rms}(k)$ denoting the RMS value of the k -th harmonic of the input current on the converter side, the RMS value of the current flowing through the DC-link capacitors according to Parseval's theorem is

$$I_{c,rms} = \sqrt{\sum_{k=1}^{+\infty} I_{d,h,rms}^2(k)}. \tag{34}$$

2.2.2 Considering AC output ripple

When considering the converter output current ripple, a correction to Eq. 30 is required. Usually, the corresponding harmonic component is superimposed on the fundamental component of the output current. According to the literature (Renken, 2005), the current ripple can be considered to be a result of the action of the converter output voltage on the filter

circuit, and the output port load is equated to the circuit shown in Figure 7, where $i_{x,f}$ is the fundamental component of the output current and the remaining components of each ripple are equal to the output voltage harmonics divided by the corresponding filter circuit impedance. Assuming that the converter output voltage harmonics resolution is $v_{x0}(\omega)$, the converter output current expression at this time is then

$$i_{x0} = i_{x,f} + \frac{v_{x0}(\omega)}{|Z(\omega)|} e^{j\varphi_z(\omega)}, \quad (35)$$

where $|Z(\omega)|$ is the filter circuit impedance, which is determined by the filter resistor, inductor, and filter capacitor parameters and $\varphi_z(\omega)$ is the corresponding phase shift angle; both parameters are functions of the harmonic frequency.

After the output current expression is corrected, it can then be substituted into Eqs 30–34 to calculate the DC-link capacitor current spectrum. In general, the output current ripple causes the DC-link capacitor current to become large when the output power is small. However, when the output power increases, the DC-link capacitor current caused by the fundamental component of the output current dominates, and the effect produced by the output ripple is very small and can basically be ignored.

3 Calculation of the multi-level, multi-phase converter structure DC-link capacitor current

3.1 Multi-level converter

In medium and high voltage and high-power applications, with the increase in DC-side voltage, the conventional two-level converters can no longer meet the requirements of the device withstand voltage levels. Multi-level converters are widely used in medium voltage and high-power applications because of the advantage of withstanding high voltage levels, no requirement for series connection of power devices, low harmonic distortion, and low switching losses. The conventional multi-level topologies mainly include neutral point clamped (NPC) (Nabae et al., 1981; Jayakumar et al., 2021; Xin et al., 2022), flying capacitor (FC) (Defay et al., 2010; Barth et al., 2019; Ye et al., 2021), and cascaded H-bridge (CHB) converters (Hammond, 1997; Lezana et al., 2008; Mhiesan et al., 2020; Maheswari et al., 2021), whose topologies are shown in Figure 8, where Figure 8A shows the topology of the three-level neutral point clamped (3L-NPC), Figure 8B shows the topology of three-level flying-capacitor (3L-FC), and Figure 8C shows the topology of the five-level cascaded H-bridge (5L-CHB).

The behavior of the switching device in the form of a switching function is continuously described, assuming that the dead time of the switch is not considered, and while treating the phase output current as a sinusoidal wave, the expression for the input current of the single bridge arm of the 3L-NPC converter is obtained according to Figure 8A.

$$i_{d1} = S_1 \times i_o, \quad (36)$$

$$i_{d2} = (1 - S_2) \times i_o, \quad (37)$$

$$i_n = (S_1 - S_2) \times i_o. \quad (38)$$

For the 3L-FC converter of Figure 8B, the relationship between the input current and flying capacitor is

$$i_{d1} = S_1 \times i_o, \quad (39)$$

$$i_{c2} = (S_2 - S_1) \times i_o. \quad (40)$$

For the 5L-CHB converter shown in Figure 8C, its input current expression is

$$i_{d1} = (S_1 - S_2) \times i_o, \quad (41)$$

$$i_{d2} = (S_3 - S_4) \times i_o. \quad (42)$$

These results show that for all these converter topologies, the DC input current or suspended capacitor current of a single bridge arm is defined by the product of two time-varying signals. When the multi-phase bridge arms are combined into a complete converter system, the DC-side current is the superposition of the input currents of each phase bridge arm.

For the calculation of the spectrum of the switching function, the same double-Fourier transform approach can be used for multi-level converters: first, the unit cell of the switching function is calculated according to the modulation strategy, then the integration range is determined according to the unit cell, and finally the spectral expression of the switching function is calculated (McGrath and Holmes, 2002; Bierhoff and Fuchs, 2008; Orfanoudakis et al., 2013; Sun et al., 2014).

3.2 Multi-phase converter

In recent years, multi-phase motors have been widely used in various fields because of their small size, light weight, and high torque density (Levi et al., 2007); the accompanying multi-phase converter technology is developing rapidly and is widely used. Generally speaking, the converter side of a multi-phase converter is one containing a multi-phase converter bridge arm; its DC side only has a set of DC-link capacitors, which are arranged between the rectifier side and multi-phase converter side.

The input current of the multi-phase converter side can simply be regarded as the superposition of the input currents of the bridge arms of each phase. Regardless of the number of phases on the converter side, the input current is obtained by a simple calculation of the superposition theorem. Taking the literature as an example, which first calculates the analytic expressions of the input current spectrum of a single-phase two-level H-bridge converter, and then gives the expressions of the input current spectrum of a 3-phase and 12-phase H-bridge converter by linear superposition of the output currents of each phase H-bridge converter unit.

It is shown that the RMS of the DC-side current will become significantly smaller as the number of converter phases increases (Parsa, 2005; Levi, 2008), and the multi-phase converter structure can reduce the DC-link capacitor requirements. This is because some of the harmonics of the input currents of each phase at the multi-phase converter side cancel each other on the DC bus, and as the number of phases increases, only the harmonics of the n^* phase times will remain, and the rest of the harmonics all cancel each other to zero.

Many modulation strategy optimization methods have also been proposed by domestic and foreign scholars to reduce the DC-side

current stress in multi-phase converter structures. The literature (Kim and Sul, 1993; Kieferndorf et al., 2004; Su and Tang, 2012; Rouhana et al., 2014; Umesh and Sivakumar, 2017) investigated the method of reducing DC-link capacitor current in-depth by carrier phase shifting; based on this, the literature (Diana et al., 2019) studied the RMS value of the input current of a five-phase two-level converter and explored the effect of the interleaved phase shifting strategy on the DC-link capacitor current. It was found that a correct phase-shifting strategy can reduce the DC capacitor current by approximately 40%. Multi-phase converter systems bring more freedom to the modulation strategy (Su and Tang, 2012; Diana et al., 2015), and converters with a large number of phases can significantly reduce the magnitude of the DC-link capacitor current by a reasonable modulation strategy (e.g., carrier phase-shift modulation).

4 DC-link capacitor resonance problem

4.1 Resonance between DC-link capacitors and bus inductor

Generally speaking, the resonance of DC-link capacitors and bus inductor is relatively weak, and this resonance problem is usually ignored. In actual engineering, when the DC-side cable is very long and the line inductance is large, the line inductance will resonate with the DC-link capacitors and affect the current flow through the DC-link capacitors due to the presence of the input current ripple on the converter side. Foreign scholars have studied the resonance of DC-link capacitors of the three-phase two-level converter, and the literature (Mantzanis et al., 2019) points out that the resonance degree of the DC-link capacitors is affected by the PWM carrier wave frequency and the magnitude of the inherent resonance frequency of the circuit. When the ratio of the PWM carrier wave frequency to resonant frequency is denoted by F_{res} , and the ratio of the PWM carrier wave frequency toward the modulating wave frequency is denoted by F_{ac} .

$$F_{res} = \frac{f_s}{f_{LC}} = 2\pi f_s \sqrt{LC}, \quad (43)$$

$$F_{ac} = \frac{f_s}{f_o}. \quad (44)$$

The quality factor Q of the DC-side circuit is equal to

$$Q = \sqrt{\frac{L}{C}} \frac{1}{R_{dc} + R_c}, \quad (45)$$

where C is the DC-link capacitor, L is the DC bus inductor, R_{dc} is the DC supply resistance, R_c is the series resistance of the DC-link capacitors, f_s is the carrier wave frequency, and f_o is the modulating wave frequency.

The literature (Mantzanis et al., 2019) shows that when $F_{res} > \max(10, 10/Q)$ and $F_{ac} \gg 10$, the inherent resonant frequency of the circuit is very low, the carrier wave ratio is very high, and the resonance has very little effect on the DC-link capacitor current at this time, and the method introduced in Sections 3, 4 can accurately solve the current flowing through the DC-link capacitors.

When $F_{res} < 1$, the inherent resonant frequency of the circuit is higher than the carrier wave frequency, if there is no large enough damping in the resonant circuit composed of the DC-link capacitors and DC-side inductor (the quality factor Q is very high), then the resonance will be very strong and will seriously affect the size of the DC-link capacitor current. At this time, the calculation method in Sections 3, 4 will have a huge error.

Figure 9 shows the relationship between the error of the RMS value calculation method of the DC-link capacitor current and each resonance parameter mentioned in Section 3. When F_{res} is very small ($F_{res} < 0.1$) or F_{res} is large ($F_{res} > 3$), the error of the conventional RMS calculation results is small. The larger the quality factor Q , the larger the error caused in the calculation of the RMS value. This is because as Q gets larger, the resistance of the resonant circuit will be smaller and its resonance will become stronger, resulting in a significantly larger DC-link capacitor current, making the traditional RMS calculation results small and providing a negative relative error.

This work argues that this is essentially because when F_{res} is large, the carrier wave frequency of the converter is greater than the inherent resonant frequency of the circuit, and the resonant frequency is close to the fundamentals of the converter input current spectrum, and the amplitude of the harmonic components in the vicinity is close to zero, and the resonance does not have a large impact on the input current spectrum. When F_{res} is very small, the inherent resonant frequency of the resonant loop is high and falls outside the high carrier side band of the converter input current, and since the amplitude of these high harmonics is very small, they do not have a large impact on the input current spectrum. When $0.1 < F_{res} < 1$, the resonant frequency falls within the low carrier side band of the converter input current, and the low carrier harmonic amplitude is large, which will significantly be amplified by the resonance, causing a significant increase in the DC-link capacitor current.

4.2 Resonance problem of multi-phase and multiple DC-link capacitors distributed arrangement structure

With the rapid development of new energy industry and the wide application of advanced transmission systems, some converter systems dealing in wind power generation, industrial transmission, vessel propulsion, and other fields gradually adopt the structure of the distributed arrangement of multi-phase DC-link capacitors based on the idea of a modular design. With this arrangement, multiple DC-link capacitors may generate more complex resonance with DC bus spurious parameters, forming a loop on the DC bus, which greatly affects the DC-link capacitor current.

In the field of vessel propulsion, new multi-phase open-winding propulsion motors are matched with multi-phase multi-level H-bridge converters. According to the DC 10 kV/tens of MW propulsion power demand, the converter side of the matched propulsion converter can adopt a five-phase H-bridge structure scheme based on four-level nested neutral point clamped (4L-NNPC) topology (Narimani et al., 2014; Tian et al., 2016; Tan et al., 2017), as shown in Figure 10.

This four-level five-phase H-bridge converter has a distributed arrangement of multiple DC-link capacitors, with independent DC-link capacitors on the DC side of each phase of the H-bridge power unit. Considering the effects of bus spurious parameters and DC-link capacitor series equivalent parameters, the topology of this type of multi-level five-phase H-bridge converter is shown in Figure 11.

Here, Inv_i denotes the phase i converter H-bridge power unit, i_{ci} denotes the current of the phase i DC-link capacitors; R_{ci} and L_{ci} are the phase i DC-link capacitor series equivalent resistance ESR and inductance ESL. R_{li} and L_{li} are the line resistance and inductance on the DC bus of section i , respectively. For the phase 1 power unit, its DC bus spurious parameters are combined into the DC power supply series impedance and are not listed separately. The five-phase power units in the actual converter have the same structure, the same length as the DC bus for each segment, and the same value for each phase parameter: $C_{dci} = C$, $R_{ci} = R_c$, $L_{ci} = L_c$, $R_{li} = R_l$, and $L_{li} = L_l$.

In order to simplify the resonant characteristics of the system, only the ripple introduced by the first phase H-bridge is considered first. The first phase H-bridge introduces the ripple current at both ends of the DC-link capacitor C_{dcl} branch and equates it to a “constant current source” i_{d1_ac} , with the corresponding ripple output. The resonant equivalent circuit of the frequency conversion system is shown in Figure 12.

According to Kirchhoff laws, the magnitude of the current i_{c1} in the branch of the capacitor C_{dcl} is

$$i_{c1} = i_{d1_ac} \frac{Z_{eq}}{Z_{eq} + Z_c} \tag{46}$$

where Z_{eq} is the equivalent line impedance after series-parallel connection of the rear four-phase DC-link capacitance and busbar spurious parameters.

$$Z_{eq} = \{[(Z_c + Z_l) \parallel Z_c + Z_l] \parallel Z_c + Z_l\} \parallel Z_c + Z_l \nu, \tag{47}$$

where $Z_c = \frac{1}{j\omega C} + j\omega L_c + R_c$ and $Z_l = j\omega L_l + R_l$ denote the DC-link capacitor branch and inter-cell DC bus impedance, respectively.

When the resistance R_c and R_l are very small, the denominator of $Z_{eq}/(Z_{eq} + Z_c)$ tends to be 0 at certain angular frequencies, the circuit resonates, and there is a sharp increase in the amplitude of the current i_{c1} phenomenon. Formula (46) is more complex to develop and directly provides the results of the resonance point; when R_c and R_l tend to be 0, the resonance point can be expressed as

$$\omega_1 = \sqrt{\frac{2L_c + (3 + \sqrt{5})L_l}{2C(L_c^2 + 3L_cL_l + L_l^2)}} \tag{48}$$

$$\omega_2 = \sqrt{\frac{2L_c + (3 - \sqrt{5})L_l}{2C(L_c^2 + 3L_cL_l + L_l^2)}} \tag{49}$$

$$\omega_3 = \sqrt{\frac{10L_c + (5 + \sqrt{5})L_l}{2C(5L_c^2 + 5L_cL_l + L_l^2)}} \tag{50}$$

$$\omega_4 = \sqrt{\frac{10L_c + (5 - \sqrt{5})L_l}{2C(5L_c^2 + 5L_cL_l + L_l^2)}} \tag{51}$$

The resonant characteristics of the system equivalent circuit when the five-phase equivalent constant current sources act separately are similar to those mentioned above. The analysis shows that the DC-link capacitors may resonate with the DC bus inductor when the DC-link capacitors are arranged in a distributed

arrangement and the DC bus resistance and the series resistance of the capacitor are very small. If the frequency of a certain ripple of the bus current is close to the system resonance point, it will cause a sharp increase of this ripple on the DC-link capacitors and significantly affect the current component of the DC-link capacitors. When the frequency of the system resonance point is close to the main spectrum of the H-bridge input current, it will cause a sharp increase in the harmonic amplitude of the DC-link capacitor current, which will lead to a sharp increase in the heating of the capacitor or even burn up in severe cases. Therefore, for the converter with the capacitor distributed arrangement, the possible resonance must be considered when the DC-link capacitors are selected and designed.

4.3 Distributed DC-link capacitor current calculation

Based on the topology of the converter side of the converter, the input current of the single-phase H-bridge can be calculated using the double-Fourier analysis method introduced in Section 4. Taking the 4L-NNPC topology shown in Figure 11 as an example, we assume that the harmonic expression of the input current of the H-bridge unit is calculated at this point as i_{di} , where $i = 1, 2, \dots, 5$.

According to the superposition theorem, the equivalent circuit response when each phase of the H-bridge input current acts separately is obtained and superimposed to obtain the current magnitude of each phase DC-link capacitor during normal operation.

The input source of each phase H-bridge converter unit as a harmonic is equated to the constant current source i_{di_ac} , and its output current is the input current of the H-bridge i_{di} minus the DC component.

$$i_{di_ac} = i_{di} - I_{d_dc}. \tag{52}$$

The resonant equivalent circuit of the five-phase converter system is obtained as shown in Figure 13.

When the phase 1 constant current source i_{d1_ac} acts alone, for the k -th harmonic $i_{d1h}(k)$ in i_{d1_ac} , its angular frequency is $\omega = 2\pi k f_0$, where f_0 is the fundamental frequency; similar to Eq. 16, when analyzing the resonance characteristics, the current component $i_{ci_d1h}(k)$ of the k -th harmonic $i_{d1h}(k)$ on the phase i DC-link capacitors can be found according to the series-parallel relationship of the circuit. Solving the current response of each phase DC-link capacitors under the action of each harmonic in i_{d1_ac} and linearly superimposing it, we can obtain the analytical formula of each phase DC-link capacitor current harmonic when the phase 1 constant current source acts alone as follows:

$$i_{ci_d1} = \sum_{k=1}^{+\infty} i_{ci_d1h}(k), \tag{53}$$

where $i = 1, 2, \dots, 5$.

The harmonic resolution of each DC-link capacitor current when the five constant current sources act individually is solved separately, and the results of each constant current source are linearly superimposed to obtain the harmonic resolution of each

phase DC-link capacitor current when the system works normally, where the phase i DC-link capacitor current is

$$\mathbf{i}_{ci} = \mathbf{i}_{ci_d1} + \mathbf{i}_{ci_d2} + \mathbf{i}_{ci_d3} + \mathbf{i}_{ci_d4} + \mathbf{i}_{ci_d5}, \quad (54)$$

where $i = 1, 2, \dots, 5$.

According to Parseval's theorem, the effective value of the current ripple of each phase DC-link capacitor can be calculated by Eq. 55:

$$I_{ci_rms} = \sqrt{\sum_{k=1}^{+\infty} I_{cih_rms}^2(k)}, \quad (55)$$

where $i = 1, 2, \dots, 5$ and $I_{cih_rms}(k)$ denotes the k -th harmonic RMS value of the DC-link capacitor current in phase i .

A five-phase 4L-NNPC topology H-bridge simulation circuit with multiple DC-link capacitor distributed arrangement structures is built using the MATLAB/Simulink simulation software, and the parameters are shown in Table 1.

The resonance points of the phase 1 DC-link capacitors at this parameter are located near the 54th, 103rd, and 140th harmonic frequencies, which fall near the three carrier side bands of the input current i_a . The phase 1 DC-link capacitor current i_{c1} harmonic spectrum is obtained by using the fast Fourier transform of the phase 1 DC-link capacitor current i_{c1} time domain simulation waveform on a fundamental period. The results are shown in Figure 14A when compared with the theoretical calculation results of Eq. 54. The results of equation calculation and simulation for the remaining four phases of the DC-link capacitor current are shown in Figures 14B–E.

The simulation results of the RMS value of the DC-link capacitor current for each phase are compared with the theoretical results calculated according to Eq. 55 as shown in Table 2.

It can be seen that the difference between the formula calculation and simulation results of the DC-link capacitor current spectrum is very small, which verifies the correctness of the equivalent circuit of multiple constant-current sources with the distributed arrangement of DC-link capacitors and the analytical formula of the DC-link capacitor current spectrum derived in the previous section.

The distributed arrangement of DC-link capacitors in common DC bus brings the problem of circulating current and resonance. The DC-link capacitors and DC bus parameters determine the resonance characteristics, such as the inherent frequency of the system, resulting in the DC-link capacitor current being directly influenced by several parameters, such as capacitor capacitance size and bus inductance resistance.

Here, we take the first phase DC-link capacitor current RMS value I_{c1_rms} as an example. According to Eq. 55, when the series equivalent resistance of the DC-link capacitors is $1.4 \text{ m}\Omega$ and line resistance on the DC bus is $4 \text{ m}\Omega$, the surface of the first-phase DC-link capacitor current RMS at different support capacitance C and line inductance on the DC bus L_1 is shown in Figure 15. As can be seen from the figure, there are several resonant peak points of the capacitor current RMS, and these resonant peak points should be avoided as much as possible to prevent the DC-link capacitor current from increasing when designing the actual multiphase inverter system.

This multi-constant current source equivalent circuit method can accurately calculate the resonance points of a multi-phase system, obtain the harmonic analytic formula of the DC-link

capacitor current considering the effects of resonance and circulating current, and quantitatively solve the magnitude of the DC-link capacitor current of each phase at resonance. According to this method, the main resonance points of the system can be avoided and the resonance of the DC-link capacitors and busbar inductor can be attenuated during the design, which can effectively guide the selection design of the DC-link capacitors and busbar parameters of the converter with the distributed arrangement of the DC-link capacitors.

5 Conclusion and outlook

According to the principle of DC-link capacitor current analysis methods in converter systems, this work divides the DC-link capacitor current analysis methods into three categories, namely, simulation method, RMS analysis method, and spectral analysis method. The research status, advantages, and disadvantages of the latter two analytical calculation methods are reviewed and summarized one by one, and their detailed calculation process is introduced with the example of a three-phase two-level converter. Then, the general solution of the input current spectrum of the multi-level converter and the characteristics of the multi-phase converter DC-link capacitor current are introduced. To address the problem of resonance with the DC bus when the converter has a distributed arrangement of multiple DC-link capacitors, this work investigates the effect of resonance on the DC-link capacitor current, equates each phase converter unit as a "constant current source" of the input current ripple, and establishes a resonant equivalent circuit of the common DC bus with multiple constant current sources. The resonant characteristics of the system are investigated, and the harmonic analytic formula of the DC-link capacitor current of each phase under resonance is derived, which can be used to guide the selection and design of the DC-link capacitors of converters of related structures. Details of the advantages and disadvantages of the aforementioned strategies and the applicable working conditions are shown in Table 3.

In the calculation of the DC-link capacitor current, the new energy field has complex working conditions. In photovoltaic power generation and wind power generation, the constant changes in sunlight and wind speed have a great impact on the current ripple stress of the DC-side DC-link capacitors, which must be considered in the actual calculation. Second, distributed multiple DC-link capacitor common DC bus structure converter devices are widely used, so the analysis and calculation of their capacitive resonance problems require the accurate acquisition of DC bus inductance. However, there is no good estimation method for measurement. In addition, the degradation of DC, DC-link capacitors, and other components (such as switching devices) in the converter system will in turn affect the DC-link capacitor current.

With the continuous development of power electronics technology, the selection and design of DC-link capacitors will face the following challenges in the future: 1) fierce competition in the global market. DC-link capacitors have to reduce the redundancy design to compress the cost under the premise of ensuring the system reliability. 2) The power density of converter devices is increasing, and the design of DC-link capacitors is subject to more and more severe volume and heat dissipation constraints. 3)

With the wide application of new energy fields and the development of advanced propulsion fields, the future working environment of DC-link capacitors may involve high temperature, sunlight (photovoltaic power generation), high salt and high humidity (vessel propulsion), and other harsh conditions, which puts forward further requirements on its reliability design.

Future research work can be targeted to explore these issues to achieve a more accurate analysis and calculation of the DC-link capacitor current and better guide its selection and design.

Author contributions

CG and BL were responsible for the main writing of the manuscript, while ZX was responsible for the revision of the manuscript. LH provided the ideas and revised the manuscript based on his extensive knowledge and experience in power electronics. All authors have contributed to the article and approved the submitted version.

Funding

This work was supported by the National Natural Science Foundation of China (grant no. 51907200) and the National

Defense Strengthening Foundation Plan of China (grant no. 2022-JCJQ-JJ-0537).

Acknowledgments

The authors would like to thank Xin and Associate Researcher Hu for their helpful discussions on topics related to this article.

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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