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The improved 2DoFs-PLL for MMC-HVDC transmission system

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The performance of a modular multilevel converter (MMC) is highly related to the three-phase phase-locked loop (PLL). The presence of the DC component, the harmonic component, and the negative sequence component results in the poor dynamic and steady-state performance of the PLL, such as fundamental frequency oscillations in the phase estimated by the PLL. In order to suppress the influence of parameters variation and disturbance of the three-phase grid voltage, an improved PLL with a moving average filter with two degrees of freedom PID (2DoFs-PID) is proposed. Moreover, to improve the phase margin and gain margin, an extra compensator with a pole and a zero is introduced into the 2DoFs-PLL. The improved 2DoFs-PLL can track the frequency and phase with superior accuracy, stability, and rapidity. Furthermore, the methodology for the parameters design of the 2DoFs PID controller is introduced, based on the index of integrated time and absolute error. A simulated model and experimental platform are established to verify the performance of the improved 2DoFs-PLL. The results show that the improved 2DoFs-PLL can meet the needs of both steady-state performance and dynamic performance by employing the 2DoFs-PID controllers.

KEYWORDS

modular multilevel converter (MMC), moving average filter, phase tracking, two degrees of freedom PID (2DoFs-PID), phase-locked loop (PLL)

1 Introduction

The renewable energy industry has risen an unprecedented height with the development of the carbon trading market (Chauhan and Saini, 2014; Chen and Chang, 2023). While renewable energy plants are almost all located in remote areas, leading to long transmission lines, a high-voltage direct current (HVDC) transmission system can decrease the transmission line losses and transmission cost, thus increasing the transmission power capacity and transmission distance (Liu et al., 2020; Nami et al., 2022).

A modular multilevel converter (MMC) is a modularization electrical equipment, which can output extra-high voltage and extra-high power (Ming et al., 2021; Errigo et al., 2022). The fundamental component of voltage output by an MMC increases as the output voltage level number increases. Thus, an MMC can improve power quality without passive filters (Shen et al., 2020; Reddy and Shukla, 2021). Moreover, the MMC is flexible in control and has low loss and extendibility, and it can control the active power and reactive power independently (Reddy and Shukla, 2021). Hence, the MMC has great potential in HVDC transmission systems.

The frequency and phase of the three-phase voltage are crucial in the control and synchronization of a grid-connected MMC (Florian et al., 2017; Xiong et al., 2021; Liu et al., 2022a). The synchronous reference frame phase-locked loop (SRF-PLL) can estimate the frequency and phase angle of the three-phase gird voltage (Xiong et al., 2021). Thus, the

control scheme of a grid-connected MMC usually employs the SRF-PLL to achieve the grid synchronization signal (Liu et al., 2022a). Under the condition of the balanced three-phase grid, the SRF-PLL can track the frequency and phase angle of the grid voltage (Florian et al., 2017; Liu et al., 2022b). Since the three-phase grid voltage always contains the direct current component, negative sequence component, and harmonic component, the dynamic response speed and steady-state output of the SRF-PLL deteriorate (Pedro et al., 2007). Furthermore, grid faults also result in the poor dynamic and steady-state performance of the SRF-PLL, such as voltage sags, phase jump, and frequency jump. For example, the direct current component results in frequency oscillations and phase oscillations, and the frequency of these oscillations is low, which is difficult to remove.

By introducing the second-order generalized integrator, trap filter, moving average filter, and so on into the SRF-PLL, its steady-stable performance is improved, while its bandwidth decreases (Xiong et al., 2015; Wu and Li, 2017). Furthermore, the dynamic response speed of the SRF-PLL deteriorates. In (Golestan et al., 2015a), to suppress the effects of an unbalanced component, a decoupled double synchronous reference frame PLL is introduced, which extracts the positive-sequence component and negative-sequence component in a three-phase grid voltage, while the effects of the DC component still remain. In (Golestan et al., 2016), five methods are introduced to eliminate the effects of the DC component, such as the dq-frame delayed signal cancelation operator, while it slows down the dynamic response speed of the SRF-PLL.

The two degrees of freedom (2DoFs) PID controllers are widely used in control fields. The parameters in 2DoFs-PID controllers can be set to meet the needs of both the tracking response performance and anti-disturbance performance. This paper introduces the 2DoFs-PID controller into the SRF-PLL to track different reference signals and suppress different disturbance signals. Moreover, to eliminate the effect of the DC component in the three-phase grid voltage, a moving average filter is introduced into the 2DoFs-PLL too, though the moving average filter introduces an extra pole into the 2DoFs-PLL system. In addition, in order to track the acceleration signal without steady-state error, the improved 2DoFs-PLL employs an extra integrator. In order to increase the gain margin and phase margin and eliminate the influence of the moving average filter and the extra integrator, a compensator with a pole and a zero is introduced into the improved 2DoFs-PLL too.

According to the index of integrated time and absolute error, the parameters design method of the 2DoF-PID controller is also proposed. Both a simulated model and experimental platform are built to verify the performance of the improved 2DoFs-PLL. The results show that the improved 2DoFs-PLL can track the constant acceleration signal and suppress the effects of disturbance signals.

2 The principle of phase-locked loop

2.1 The control scheme of modular multilevel converter

In a HVDC transmission system, the MMC can realize the AC-DC power conversation. Figure 1 shows the control scheme of the MMC with the outer DC voltage closed loop, inner current closed loop, and circulating current control loop.

As shown in Figure 1, u_a, u_b, and u_c are the AC system voltage; i_a, i_b, and i_c are the AC system current; θ is the phase angle of three-phase grid voltage; u_{dc} is the voltage of the DC bus; $u_{dc\text{-}ref}$ is the voltage reference of the DC bus; u_d and u_q are the d-axis voltage and q-axis voltage, respectively; i_d and i_q are the d-axis current and q-axis current, respectively; u_{a_ref}, u_{b_ref}, and u_{c_ref} are the output midpoint voltage reference of the bridge arm; i_{au}, i_{bu}, and i_{cu} are the current flowing through the upper bridge arm; i_{al}, i_{bl}, and i_{cl} are the current flowing through the lower bridge arm; u_{adiff_ref}, u_{bdiff_ref}, and u_{cdiff_ref} are the voltage drops of the bridge arm reactance, which are caused by a circulating current; u_{au_ref}, u_{bu_ref}, and u_{cu_ref} are the voltage reference of the upper bridge arm; and u_{al_ref}, u_{bl_ref}, and u_{cl_ref} are the voltage reference of the lower bridge arm.

L in Figure 1 is expressed as:

$$L = L_s + \frac{L_{arm}}{2} \tag{1}$$

where L_s is the interface inductance between the MMC and grid, and L_{arm} is the arm inductance.

The voltage references of the upper bridge arm and lower bridge arm are expressed as:

$$\begin{aligned}
u_{au_ref} &= \frac{u_{dc}}{2} - u_{a_ref} - u_{adiff_ref} \\
u_{bu_ref} &= \frac{u_{dc}}{2} - u_{b_ref} - u_{bdiff_ref} \\
u_{cu_ref} &= \frac{u_{dc}}{2} - u_{c_ref} - u_{cdiff_ref} \\
u_{al_ref} &= \frac{u_{dc}}{2} + u_{a_ref} - u_{adiff_ref} \\
u_{bl_ref} &= \frac{u_{dc}}{2} + u_{b_ref} - u_{bdiff_ref} \\
u_{cl_ref} &= \frac{u_{dc}}{2} + u_{c_ref} - u_{cdiff_ref}
\end{aligned} \tag{2}$$

2.2 The theory of phase-locked loop

As shown in Figure 1, θ has an important influence on the control system of the MMC. The three-phase grid voltage is assumed as:

$$\begin{cases}
u_a(t) = \sum\limits_{h=1,5,7\ldots\ldots} \left[U_h^{+}\cos\left(h\omega_1 t + \theta_h^{+}\right) + U_h^{-}\cos\left(-h\omega_1 t + \theta_h^{-}\right)\right] \\
u_b(t) = \sum\limits_{h=1,5,7\ldots\ldots} \left[U_h^{+}\cos\left(h\omega_1 t + \theta_h^{+} - \frac{2}{3}\pi\right) + U_h^{-}\cos\left(-h\omega_1 t + \theta_h^{-} + \frac{2}{3}\pi\right)\right] \\
u_c(t) = \sum\limits_{h=1,5,7\ldots\ldots} \left[U_h^{+}\cos\left(h\omega_1 t + \theta_h^{+} + \frac{2}{3}\pi\right) + U_h^{-}\cos\left(-h\omega_1 t + \theta_h^{-} - \frac{2}{3}\pi\right)\right]
\end{cases} \tag{3}$$

where U_h^{+} and U_h^{-} are the amplitude of the positive-sequence component and negative-sequence component, respectively, θ_h^{+} and θ_h^{-} are the phase angle of the positive-sequence component and negative-sequence component, respectively, h is the harmonic order, and ω_1 is the angular frequency of the fundamental harmonic.

With the regard to the DC component, the PLL applies the moving average filter to eliminate its influence, and with regard to the even-order harmonic component, the amplitudes are much

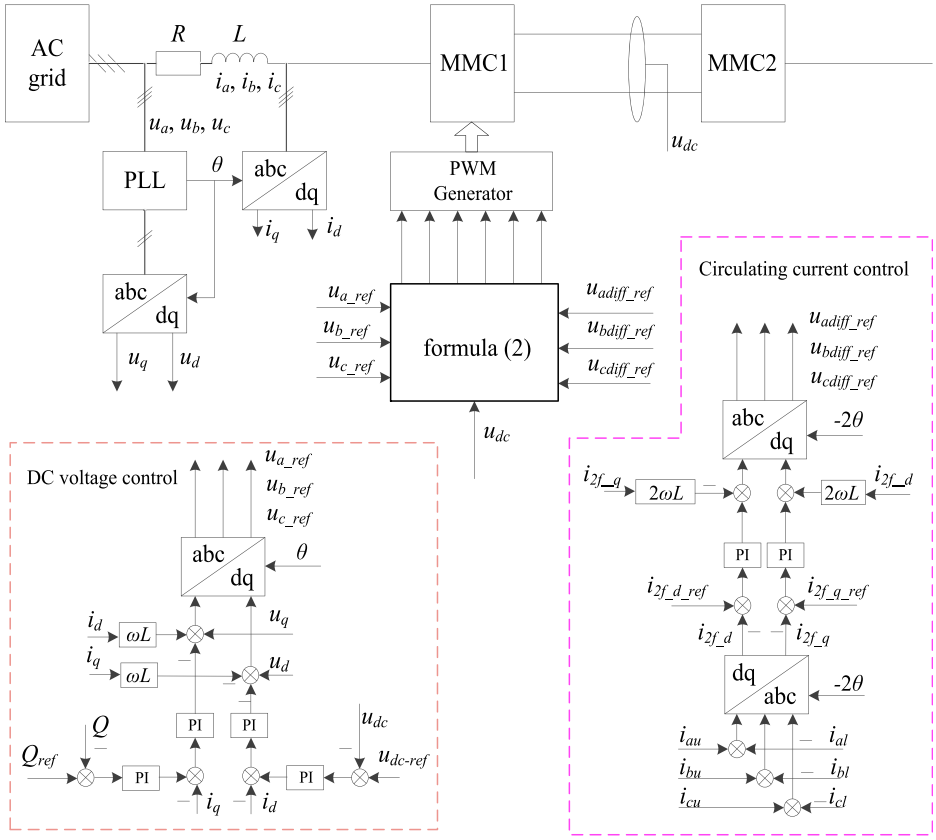

FIGURE 1
The control system of MMC.

lower. Thus, (3) neglects the DC component and even-order harmonic component.

By applying the Clarke transformation, (3) can be expressed as:

$$\begin{cases} u_\alpha(t) = \sum_{h=1,5,7.....} \left[U_h^+ \cos\left(h\omega_1 t + \theta_h^+\right) + U_h^- \cos\left(-h\omega_1 t + \theta_h^-\right)\right] \\ u_\beta(t) = \sum_{h=1,5,7.....} \left[U_h^+ \sin\left(h\omega_1 t + \theta_h^+\right) - U_h^- \sin\left(-h\omega_1 t + \theta_h^-\right)\right] \end{cases} \tag{4}$$

By applying the Park transformation, (4) can be expressed as:

$$\begin{cases} u_d(t) = \sum_{h=1,5,7.....} \left[U_h^+ \cos\left(h\omega_1 t + \theta_h^+ - \hat{\theta}_1^+\right) + U_h^- \cos\left(-h\omega_1 t + \theta_h^- + \hat{\theta}_1^+\right)\right] \\ u_q(t) = \sum_{h=1,5,7.....} \left[U_h^+ \cos\left(h\omega_1 t + \theta_h^+ - \hat{\theta}_1^+\right) - U_h^- \cos\left(-h\omega_1 t + \theta_h^- + \hat{\theta}_1^+\right)\right] \end{cases} \tag{5}$$

Once the output of PLL is θ_1^+, $u_q(t)$ is expressed as:

$$u_q(t) = U_1^+\left(\theta_1^+ - \hat{\theta}_1^+\right) + f' \tag{6}$$

where f' is the high-frequency disturbance.

Thus, the transfer function of the SRF-PLL with the first-order low-pass filter is expressed as:

$$G(s) = U_1^+ \frac{K_p s + K_i}{s^2\left(T_{lf} s + 1\right)} \tag{7}$$

where K_p and K_i are the proportional coefficient and integral coefficient, respectively, and T_{lf} is the time constant of the first-order low-pass filter.

According to (7), the bandwidth of the SRF-PLL is highly related with U_1^+. Thus, voltage sags will affect the stability of the SRF-PLL.

The SRF-PLL usually applies the PI controller instead of the filter. Thus, the dynamic speed of the SRF-PLL is relatively low. In (Golestan et al., 2014), the trap filter is applied to eliminate the specific-order harmonic, while its performance is insufficient to meet the time-varying three-phase grid. In (Golestan et al., 2015b; Hamed Hany et al., 2016), the second-order generalized integrator is applied in the PLL, which lacks the suppression of the DC component. Thus, the PLL will result in fundamental frequency oscillations and phase angle oscillations.

The transfer function of the moving average filter is expressed as:

$$G_{maf}(s) = \frac{1 - e^{-T_\omega s}}{T_\omega s} \approx \frac{1}{\frac{T_\omega s}{2} + 1} \tag{8}$$

(8) shows that the moving average filter is equivalent to an infinite number of cascaded trap filters. It can eliminate any integer-order harmonic component by setting the T_ω. Furthermore, compared with the PID controller, trap filter, and second-order generalized integrator, the moving average filter is much easier to implement in software.

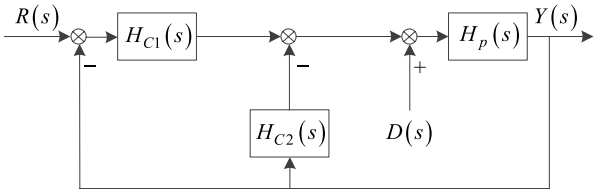

FIGURE 2
The PLL with the 2DoFs-PID.

2.3 2DoFs-PID

The single degree of the freedom PID controller cannot meet the needs of both the tracking performance and anti-disturbance performance. Figure 2 shows a PLL with the 2DoFs-PID controller.

As shown in Figure 2, $H_{C1}(s)$ is the transfer function of the PID controller in the feedback loop, and $H_{C2}(s)$ is the transfer function of the PID controller in the feed-forward loop. $H_{C1}(s)$ and $H_{C2}(s)$ are expressed as:

$$\begin{aligned} H_{C1}(s) &= \alpha K_P + \frac{K_I}{s} + \beta K_D s \\ H_{C2}(s) &= (1-\alpha)K_P + (1-\beta)K_D s \end{aligned} \tag{9}$$

where K_P, K_I, and K_D are the proportional coefficient, integral coefficient, and differential coefficient, respectively, and α and β are the coefficients of the two degrees of freedom.

As shown in Figure 2, the transfer function between the input signal and output signal is expressed as (10), and the transfer function between the disturbance signal and output signal is expressed as (11):

$$H_{YR}(s) = \frac{H_{C1}(s)H_p(s)}{1 + (H_{C1}(s) + H_{C2}(s))H_p(s)} \tag{10}$$

$$H_{YR}(s) = \frac{H_p(s)}{1 + (H_{C1}(s) + H_{C2}(s))H_p(s)} \tag{11}$$

3 The operation performance of 2DoFs-PLL

3.1 The closed-loop transfer function

Figure 3 shows the structural schematic diagram of the 2DoFs-PLL with the moving average filter. In order to improve the performance of the tracking acceleration signal, an extra integrator is applied in the forward path. Thus, there are a total of three integrators in the improved 2DoFs-PLL.

Based on the internal model principle, the 2DoFs-PLL can track an acceleration signal without a structurally steady error.

The extra integrator results in a smaller phase margin, and the moving average filter introduces an additional pole, which will impact the stability of the 2DoFs-PLL. Thus, to eliminate the influence of the extra integrator and moving average filter, a compensator with a pole and a zero is introduced. Its transfer function is expressed as:

$$H_{ex}(s) = \frac{1 + \frac{T_{\omega 1}}{2}s}{s} \tag{12}$$

The structural diagram of the improved 2DoFs-PLL is shown in Figure 4.

Thus, the closed-loop transfer function of the improved 2DoFs-PLL is expressed as:

$$H_{YR}(s) = \frac{\beta K_D s^2 + \alpha K_P s + K_I}{s^3 + K_D s^2 + K_P s + K_I} \tag{13}$$

$$H_{YR}(s) = \frac{s}{s^3 + K_D s^2 + K_P s + K_I} \tag{14}$$

3.2 Parameters design method

Based on (14), if K_P>0, K_I>0 and K_D>0 is satisfied, the improved 2DoFs-PLL is stable.

Moreover, according to (10) and (11), $H_{C1}(s)$ + $H_{C2}(s)$ is equivalent to the traditional PID controller. In terms of integrated time and absolute error, (13) should be expressed as:

$$H_{YR}(s) = \frac{2.97\beta\omega_0 s^2 + 4.94\alpha{\omega_0}^2 s + {\omega_0}^3}{s^3 + 2.97\omega_0 s^2 + 4.94{\omega_0}^2 s + {\omega_0}^3} \tag{15}$$

where $\omega 0$ is the bandwidth of the PLL.

Thus, according to (13) and (15), *KP*, *KI*, and *KD* are achieved.

Then, based on the integrated time and absolute error and *HYR*(*s*), the parameters α and β are achieved.

3.3 The performance of improved 2DoFs-PLL

To verify the performance of the improved 2DoFs-PLL, a simulated model is built, and the parameters are shown in Table 1.

According to (13) and (14) and Table 1, the settling time is 0.03s, the gain margin is 26.5dB, and the phase angle margin is 54°.

Figure 5 shows the response diagrams of the disturbance signals and reference signals.

As shown in Figure 5A, the improved 2DoFs-PLL can eliminate the influences of the disturbance signals on the output. The responses of the step disturbance signal, constant speed disturbance signal, and constant speed disturbance signal are relatively small. The unit step response is approximately equal to 5E-06. The responses of the constant speed disturbance signal and constant speed disturbance signal can even be ignored.

Furthermore, the improved 2DoFs-PLL shows a rapid responsibility of the step disturbance signal, constant speed disturbance signal, and constant speed disturbance signal. The decay time is about 0.06 s, which is equal to three power-frequency periods.

As shown in Figure 5B, the improved 2DoFs-PID can track the step reference, constant speed reference, and constant acceleration reference without the steady-state error, and for the step reference, the response is without overshoot.

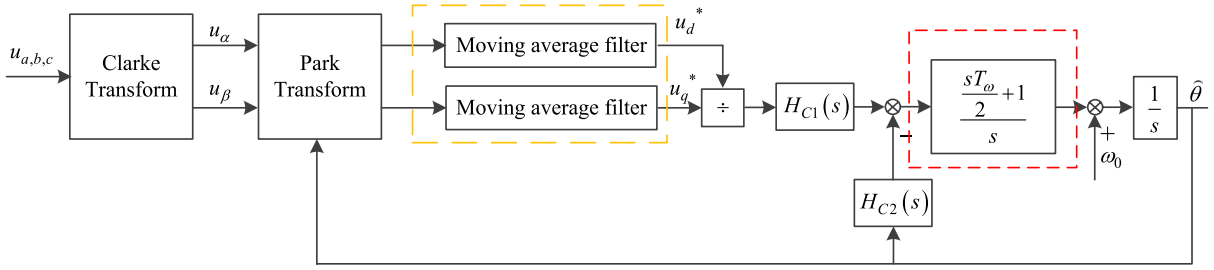

FIGURE 3
Structural diagram of the 2DoFs-PLL.

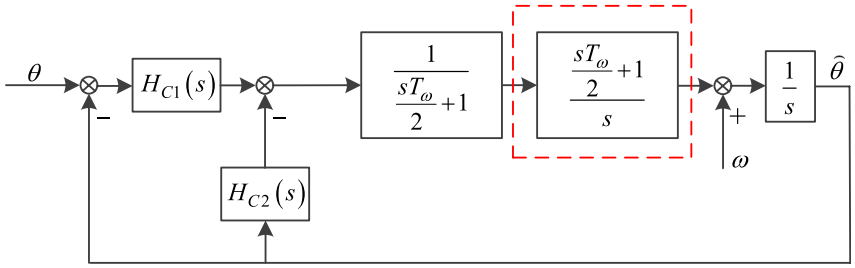

FIGURE 4
The transfer function of the improved 2DoFs-PLL.

TABLE 1 Parameters of 2DoFs-PLL.

Parameters	Value	Parameters	Value
ω0	70rad/s	*KP*	24,206
α	0.928	*KI*	343,000
β	0.738	*KD*	208

4 Results

To verify the proposed improved 2DoFs-PLL, a simulation model is built. To facilitate comparison, the SRF-PLL orientates the phase angle of the three-phase grid voltage at the zero-crossing point of the voltage, and the improved 2DoFs-PLL orientates the phase angle of the three-phase grid voltage at the peak point of the voltage. Thus, compared with the improved 2DoFs-PLL, the output of the SRF-PLL is 90° ahead.

Figure 6A shows the output diagram under the condition that there is DC component in the three-phase voltage. Figure 6B shows the output diagram under the condition that there is a harmonic component and negative sequence component in the three-phase voltage. Figure 6C shows the output diagram under the condition that there is a phase jump in the three-phase voltage. Figure 6D shows the output diagram under the condition that there is a voltage amplitude jump and frequency jump in the three-phase voltage.

As shown in Figure 6A, the DC component is introduced into the three-phase voltage at 0.2 s. Both the SRF-PLL and improved 2DoFs-PLL can track the phase angle rapidly. Compared with the SRF-PLL, the dynamic response speed of the improved 2DoFs-PLL is relatively higher since it contains a differentiation element, and there is a slight distortion in the output of the SRF-PLL. Thus, in respect to the DC component, both the dynamic performance and steady performance of the improved 2DoFs-PLL are superior to that of the SRF-PLL.

As shown in Figure 6B, the harmonic component and negative sequence component are introduced into the three-phase voltage at 0.2 s. The response of the SRF-PLL contains an apparent distortion. Thus, the SRF-PLL cannot adapt to the grid with a harmonic component. Meanwhile, the improved 2DoFs-PLL can track the phase angle without the steady-state error, and its response speed is still high. Thus, in respect to the harmonic component and negative sequence component, both the dynamic performance and steady performance of the improved 2DoFs-PLL are superior to that of the SRF-PLL.

As shown in Figure 6C, the phase jump is introduced into the three-phase voltage at 0.2 s. The response speed of the improved 2DoFs-PLL is slightly slower than that of the SRF-PLL, and both PLLs can track the phase angle without the steady-state error.

As shown in Figure 6D, the voltage amplitude jump and frequency jump are introduced into the three-phase voltage at 0.2 s, and the frequency is from 50to 45 Hz. Both PLLs can track the phase angle without the steady-state error.

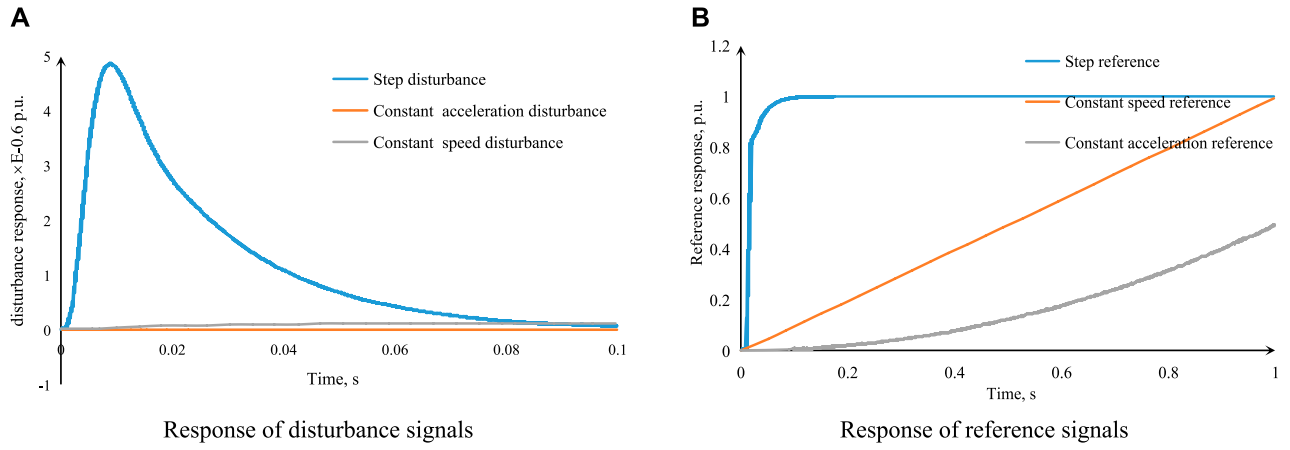

FIGURE 5
The responses performance of the improved 2DoFs-PLL. **(A)** The response of disturbance signals. **(B)** The response of reference signals.

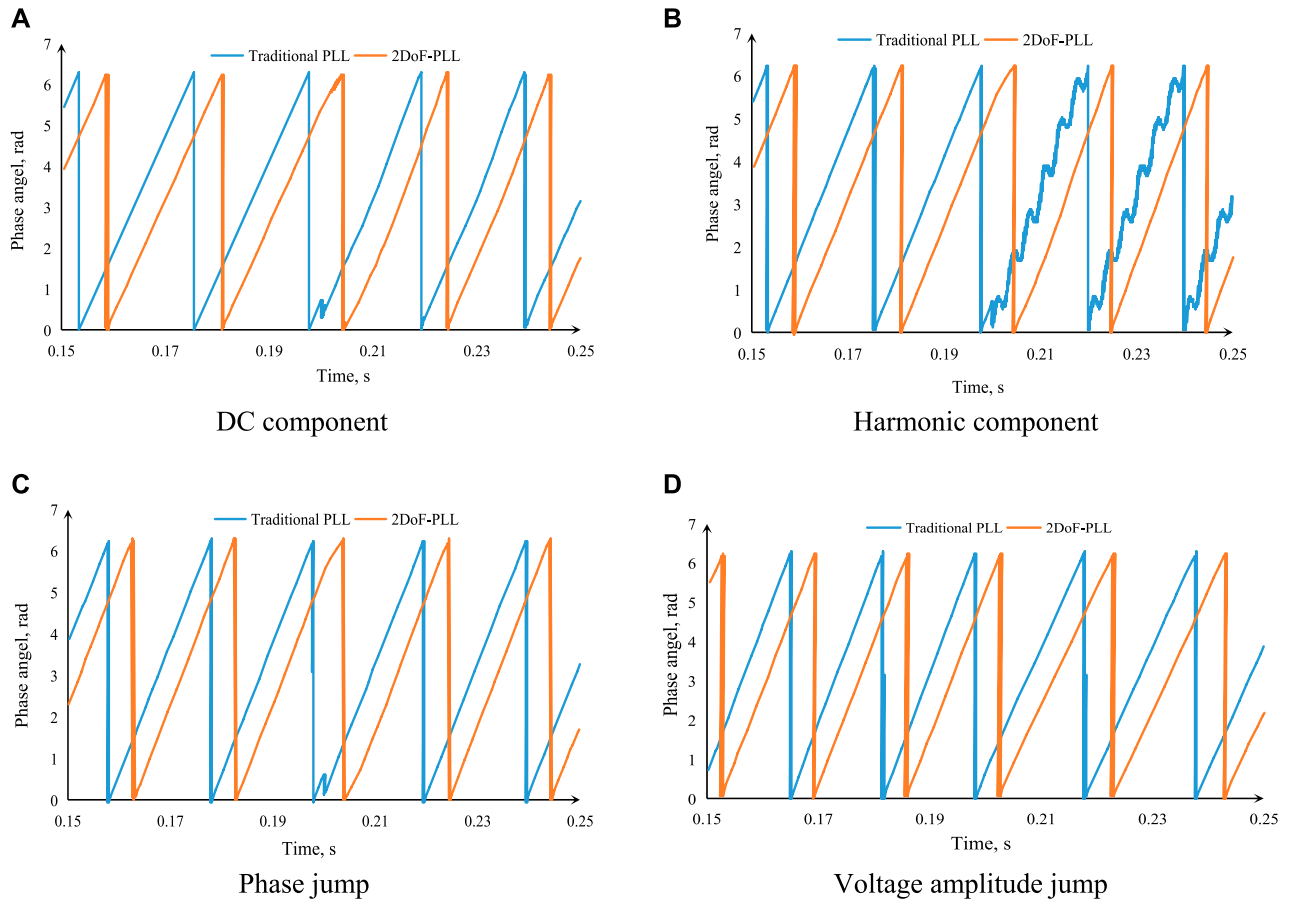

FIGURE 6
The response under different conditions. **(A)** The response under the condition of DC component. **(B)** The response under the condition of harmonic component. **(C)** The response under the condition of phase jump. **(D)** The response under the condition of voltage amplitude jump.

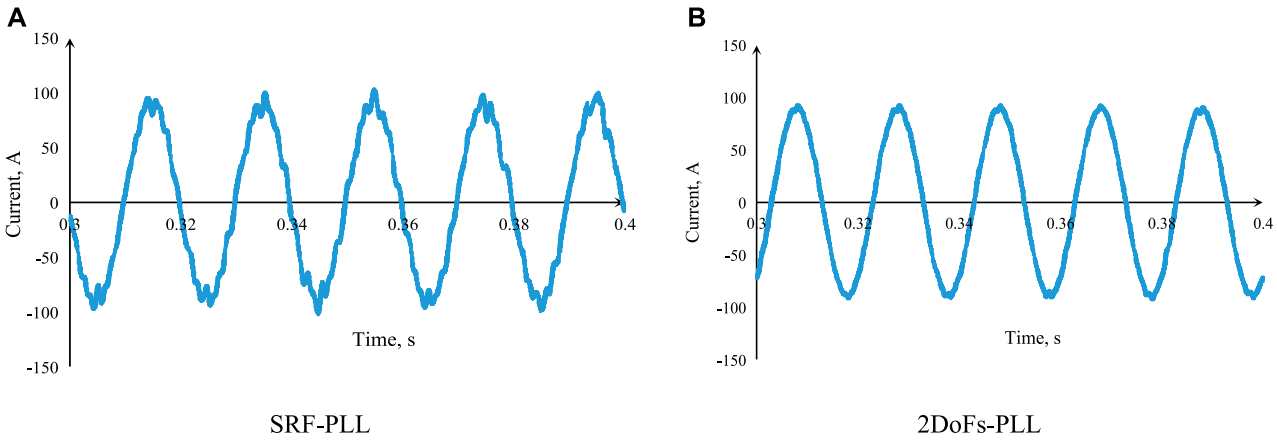

FIGURE 7
The output current of the MMC. **(A)** The output current with SRF-PLL. **(B)** The output current with 2DoFs-Pll.

Thus, compared with the SRF-PLL, the improved 2DoFs-PLL can track the phase angle under severe conditions.

Figure 7 shows the output current of the MMC under the conditions that the three-phase grid voltage contains the harmonic component. Moreover, the number of SMs in each arm is 12, the DC bus voltage is 12 kV, the amplitude of AC voltage is $12 \times \sqrt{3}/\sqrt{2}$ V, and the frequency is 50 Hz.

As shown in Figure 7, the control system with the improved 2DoFs-PLL shows a superior performance to the SRF-PLL.

5 Conclusion

The 2DoFs-PID controllers can eliminate the influences of different disturbance signals and track different reference signals without the steady-state error. In order to improve the phase margin and gain margin and counteract the effects of the moving average filter, an extra compensator with a pole and a zero is introduced into the improved 2DoFs-PLL. Based on the index of integrated time and absolute error, the parameters are designed too.

The simulated results show that the output of the improved 2DoFs-PLL is almost equal to zero with the step disturbance, constant speed disturbance, and constant acceleration disturbance. Moreover, the improved 2DoFs-PLL can track the step reference, constant speed reference, and constant acceleration reference accurately and rapidly.

The results also show that the dynamic response speed of the improved 2DoFs-PLL is relatively high. It can track the frequency and phase angle without the steady-state error under the conditions of the DC component, harmonic component, negative sequence component, phase jump, frequency jump, and amplitude jump.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material, further inquiries can be directed to the corresponding author.

Author contributions

Conceptualization, WW; methodology, WW, PW, and HC; software, PW and RB; validation, WW and HC; resources, WW and PW; data curation, HC, RB, and LG; writing—original draft preparation, WW and LG; writing—review and editing, WW, RB, and HC; supervision, WW and HC; funding acquisition, WW. All authors contributed to the article and approved the submitted version.

Conflict of interest

Authors WW, PW, and LG were employed by the Guangdong Power Grid Company; Author RB was employed by the company NR Electric Co., Ltd.

The remaining author declares that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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