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Topology and control strategy optimization of an auxiliary resonant commutated pole-based, soft-switching grid-connected inverter

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With the development of new energy industries such as photovoltaics, microgrids, or distributed energy sources require many DC-AC grid-connected interfaces. Reducing the switching loss of the inverter is important to improve the transmission efficiency of the inverter, reduce the heat generation of the inverter, promote the high frequency and miniaturization of the inverter, and efficiently use the distributed energy. Therefore, considering the wide application of DC-AC power electronic interfaces in microgrid and distributed energy, and to make up for existing deficiencies in traditional hard-switching inverters, an optimal control strategy and topology for an optimal-auxiliary resonant commutated pole (O-ARCP) inverter is proposed in this article. Firstly, this paper introduces the proposed inverter topology and analyzes the operation mode of the circuit with the control strategy. Then simulation experiments in islanding mode are carried out to verify the rationality of the content, and finally simplified experimental verification is carried out based on the simulation results. Simulation and experimental testing reveal that all switches of the proposed topology are in soft-switching mode, which proves the effectiveness of the proposed control strategy and analysis. The analysis and validation of this paper provide assistance in the development of control strategies and structures for soft-switching inverters.

KEYWORDS

inverter, auxiliary resonant commutated pole, soft switching, zero voltage switching, zero current switching

1 Introduction

The development of renewable energy can effectively reduce dependence on fossil fuels and environmental pollution. As a result, distributed energy sources such as photovoltaic power, wind power, and hydropower have been developing rapidly.

Many distributed energy sources can be efficiently arranged and managed when they are connected to a microgrid in a uniform manner. Therefore, the development of microgrids can help reduce carbon emissions, improve the utilization of clean energy, and solve the problem of local consumption of renewable energy. However, the large amount of distributed energy access requires more efficient power electronic interfaces, of which DC-AC power electronic converters are an important component. Further reducing the loss of the DC-AC converter and ensuring its efficient and stable operation is a key issue.

The conventional hard-switching inverter has a dramatic increase in switching losses as the pulse width modulation (PWM) frequency rises, and soft-switching techniques have been developed to reduce the losses caused by the increase in switching frequency (Zhang et al., 2010; Li and Xu, 2013; Mishima et al., 2013; Li, 2015; Pal A and Basu K. A., 2018; Samani et al., 2018).

The earliest soft-switching inverter is the resonant DC-link inverter proposed by Divan (1989), which was epoch-making for soft-switching inverter technology development. This topology is very simple, and only one set of LC devices is required to make the whole circuit work in soft-switching mode. However, it also has a very clear drawback: when resonance occurs, the DC bus voltage's resonant peak is too high, significantly increasing the stress on the bus voltage. Active clamped resonant DC-link inverters are proposed to solve this problem. Moreover, many new solutions have been proposed in recent years for resonant losses and control techniques (Divan and Skibinski, 1989; Deshpande et al., 1997; Jafar and Fernandes, 2002; Gurunathan and Bhat, 2007; Amirabadi et al., 2014).

Some scholars have proposed a parallel resonant DC link inverter to replace the resonant DC link resonant inductor connected in series among the bus power, where the resonant inductor is connected in parallel among the power channels. This structure bus voltage stress is not higher than the DC voltage, and the inverter can use PWM modulation. However, frequent bus voltage over zero can affect the efficiency of soft switching (Chibani and Nakaoka, 1992; Hui et al., 1996; Chen, 1998; De Andrade et al., 2001; Behera et al., 2004; Pan and Luo, 2004; Pan and Luo, 2005; Mandrek and Chrzan, 2007; Kedariseti and Mutschler, 2011; Wang et al., 2014).

The auxiliary resonant commutated pole (ARCP) inverter was proposed in 1989 with bus voltage not periodically resonating to zero. The auxiliary circuit only works at the moment of current change, with little loss to itself and low loss to the circuit. This approach is the best choice to achieve efficient soft switching under high power, but the voltage of the midpoint capacitor is not easy to stabilize due to the use of voltage-dividing capacitors. Subsequent scholars have proposed many improvement strategies.

Cai et al. (2019) proposed a novel ARCP inverter that achieved good results by replacing the position of the midpoint capacitor with a switching device.

Chu et al. (2014) and Chu et al. (2016) also utilized switching devices for current conversion, but too many auxiliary devices increase the losses.

Other studies (Yu et al., 2009; Chu et al., 2014; Chu et al., 2019; Wang and Wang, 2020; Chu et al., 2022) do not use a midpoint capacitor for current conversion, but their control strategy has an auxiliary circuit operating at both dead times within a single PWM cycle, which leads to an increase in losses.

The DC-AC power electronic converter interface assumes an important role in grid-connected or off-grid microgrids. The overall efficiency of the inverter cannot be improved due to the switching losses during the transmission of the DC-AC power electronic converter, and there are problems such as limited switching frequency, oversized filters, and heat generation. A new soft-switching topology of the auxiliary resonant commutation stage is proposed to address the switching losses in the transmission process of the grid-connected inverter. The control strategy and topology are simplified to address the complex control problem of the traditional soft-switching topology. The soft-switching process only occurs in the dead time of the inverter, and only half of the

auxiliary switches are required to work every half cycle to make the inverter work in the soft-switching mode. Based on this topology, the switching losses of the grid-connected inverter can be reduced, the conversion efficiency of the inverter can be improved, and the inverter can be operated at a higher frequency to reduce the harmonics.

2 Materials and methods

2.1 Introduction to auxiliary circuits

The soft-switching topology is shown in Figure 1. One of the phases is used as a reference to analyze its operating principle, and its equivalent circuit diagram is shown in Figure 1B.

The auxiliary circuit consists of switching S_1 and S_4 , resonant capacitors C_1 , C_2 , and C_3 , auxiliary diodes D_5 – D_{10} , and resonant inductors L_1 – L_4 .

L_1 , D_7 , and C_3 provide the ZCS turn-on condition for S_2 . C_3 provides the ZVS turn-off condition for S_2 . L_2 and C_1 provide the ZCS turn-on and ZVS turn-off conditions for S_1 .

C_3 and L_3 provide the ZCS turn-on condition for S_3 . C_3 provides the ZVS turn-off condition for S_3 . L_4 and C_2 provide the soft-switching condition for S_4 .

2.2 Basic working principle

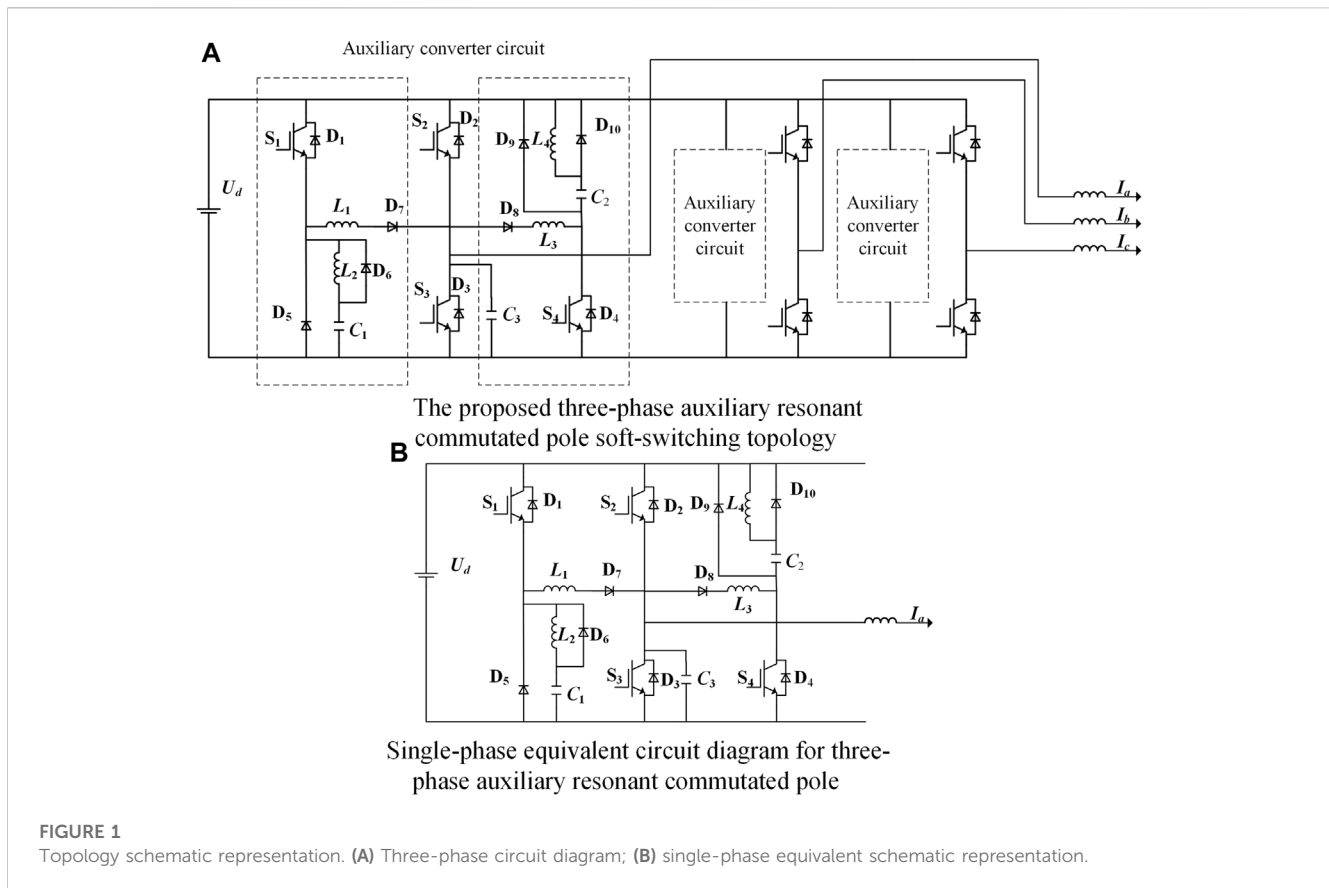
To facilitate the analysis of the entire circuit structure, the article takes one of the three equivalent phases for analysis. The topological circuit divides the circuit into two time periods with positive and negative load current directions, respectively. Its switching equivalent control schematic representation and partial voltage and current are shown in Figure 2.

Figure 2A includes the S_1 – S_4 switching operation mode when the load current direction is positive during the time period of t_0 – t_4 , the change in inductor current i_L flowing through the auxiliary inductor L_1 , and the change in voltage U_{c3} across the auxiliary capacitor C_3 .

Figure 2B includes the S_1 – S_4 switching operation mode when the load current direction is negative during the t_5 – t_9 time period, the change in inductor current i_L flowing through the auxiliary inductor L_3 , and the change in voltage U_{c3} across the auxiliary capacitor C_3 .

Where the signal is high level, S_1 – S_4 represents the switch turn-on state; when the signal is low level, S_1 – S_4 represents the turn-off state. For S_2 , S_3 , each drive interval has a certain dead time to turn on the auxiliary circuit to achieve the effect of soft switching.

As can be seen from Figure 2, under the control strategy proposed in this paper, only switch S_1 is required to work when the load current direction is positive to achieve the soft-switching effect. Similarly, only switch S_4 is required to work when the load current direction is negative. Compared with the control strategy proposed by Chu et al. (2016), the additional losses due to the need to turn on S_1 and S_4 alternately for each PWM cycle are greatly reduced. Compared to the control strategy in this paper, Chu et al. (2014) required multiple auxiliary switches to work alternately, which both complicates the control strategy and adds additional losses.



An analysis of the circuit yields the equivalent circuit diagram shown in Figure 3.

2.3 Operation mode with positive load current

When the load current direction is positive, the current mainly flows through switch S_2 only when a group of auxiliary components corresponding to S_1 is in working condition.

The operating mode is divided into five operating time periods, and, assuming it is in an ideal state, the principle of the circuit is analyzed as follows:

Mode t_0 : At this stage, switch S_2 is turned on, the auxiliary circuit does not work, and the load current flows from switch S_2 to the load.

Mode t_1 : Switch S_3 is in the off state at this stage. When switch S_2 needs to be turned off, the voltage across capacitor C_3 does not change suddenly, the magnitude of the voltage across capacitor C_3 is still the bus voltage, and the U_{C3} voltage drops to zero after a period of time. The voltage across switch S_2 is zero. Therefore, switch S_2 is the ZVS turn-off. When switch S_2 needs to be turned on, the auxiliary circuit needs to work to provide the ZVS turn-on condition for S_2 .

At this time, the voltage across U_{C3} decreases linearly, as shown in the following equation:

$$U_{C3} = U_d - U_d t,$$

where U_d is the busbar voltage.

Mode t_2 : S_3 is turned on at this stage. Because the capacitive voltage across U_{C3} has been reduced to zero in mode t_1 , S_3 is the ZVS turn-on.

Mode t_3 : S_1 turns on, and the resonant current i_{L1} begins to rise nonlinearly. Because L_1 and L_2 will obstruct the instantaneous current, the auxiliary switch S_1 is the ZCS turn-on. When the resonant current reaches the value of the load current, the resonant current i_{L1} is in the constant current stage. The voltage at both ends of capacitor U_{C3} starts to rise. When it reaches the bus voltage, diode D_2 conducts, so S_2 is the ZVS turn-on. At the same time, part of the current flows through L_2 and C_1 , and the voltage across C_1 begins to rise in preparation for the ZVS turn-off of S_1 .

The relevant changes are analyzed as shown in the following equations. The current i_{L1} flowing through L_1 is shown in the following equation:

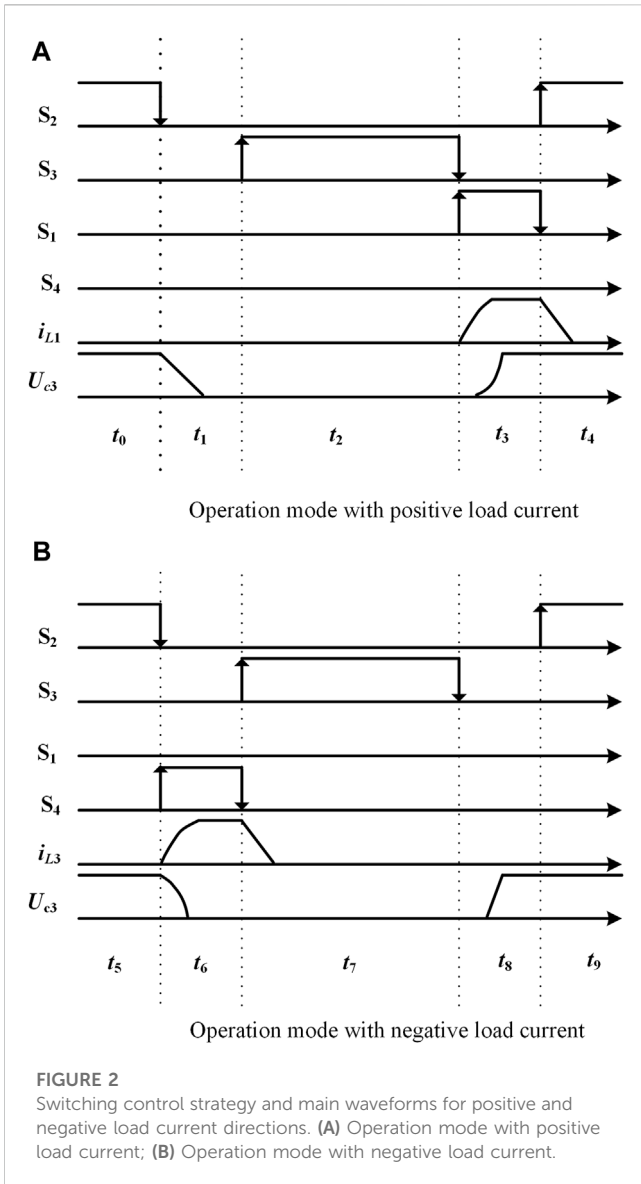
$$i_{L1}(t) = \frac{U_d}{Z_r} \sin \omega t + I_a.$$

The current i_{L2} flowing through L_2 is analyzed as shown in the following equation:

$$i_{L2}(t) = \frac{U_d}{Z_1} \sin \omega_1 t.$$

The maximum current I_{s1max} flowing through S_1 is shown in the following equation:

$$I_{s1max}(t) = i_{L1}(t) + i_{L2}(t).$$



The change in voltage across C_1 , C_3 is shown in the following equation:

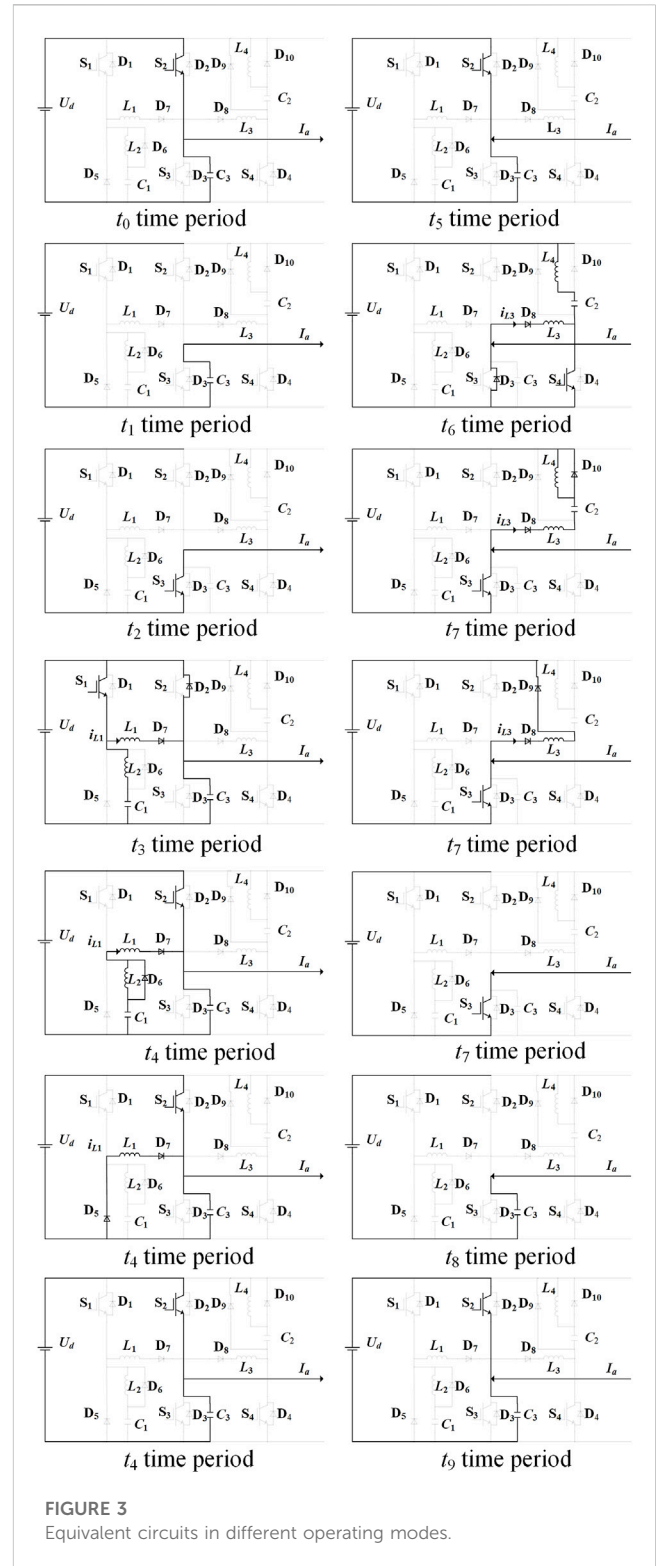
$$U_{e3} = U_d(1 - \cos\omega t),$$

where $\omega = 1/\sqrt{L_1C_3}$, $Z_r = \sqrt{L_1/C_3}$, $\omega_1 = 1/\sqrt{L_2C_1}$, $Z_1 = \sqrt{L_2/C_1}$, and I_d is the load current.

Mode t_4 : When the voltage across C_1 reaches the bus voltage, the voltage across C_1 does not rise due to the clamp effect of diode D_6 . When S_1 needs to be turned off, the voltage across S_1 is zero due to the presence of capacitor C_1 . Therefore, the S_1 turn-off belongs to the ZVS turn-off. When S_1 is turned off, the resonant current i_{L1} decreases at a linear rate.

2.4 Operation mode with negative load current

When the load current direction is negative, it is divided into five action time zones according to the action time sequence, and assuming that the circuit is in an ideal state, the corresponding



time range in Figures 2, 3 is the t_5 - t_9 time period, which is analyzed as follows.

Mode t_5 : At this time, switch S_2 remains on, but the load current direction is negative.

Mode t_6 : S_4 turns on, and the resonant current i_{L3} begins to rise nonlinearly. Because L_3 and L_4 will obstruct the instantaneous current, the auxiliary switch S_4 is the ZCS turn-on. The

TABLE 1 Simulation parameters of the three-phase ARCP inverter.

Component	Parameter
Output power	1 kW
DC voltage supply (U_d)	200 V
Switching frequency	10 kHz
Output frequency	50 Hz
Dead time	1 μ s
L_1, L_3	8 μ H
L_2, L_4	1 μ H
C_1, C_2	100 pF
C_3	10 nF

capacitance voltage U_{c3} begins to decrease until the D_3 begins to conduct. At this time, the capacitance voltage across C_2 begins to rise in preparation for the ZVS turn-off of S_4 .

At this time, the current i_{L3} flowing through the inductor L_3 changes, as shown in the following equation:

$$i_{L3}(t) = \frac{U_d}{L_3} \sin \omega_2 t.$$

The current i_{L4} flowing through inductor L_4 changes as shown in the following equation:

$$i_{L4}(t) = \frac{U_d}{\sqrt{L_4/C_2}} \sin \omega_3 t.$$

The current I_{S4} flowing through switch S_4 changes as shown in the following equation:

$$I_{S4} = i_{L3}(t) + I_a + i_{L4}(t).$$

The voltage across the capacitor C_3 changes as shown in the following equation:

$$U_{c3}(t) = U_d \cos \omega_2 t.$$

Here, $\omega_2 = 1/\sqrt{L_3 C_3}$, $\omega_3 = 1/\sqrt{L_4 C_2}$, I_a is the load output current, and U_d is the busbar voltage.

Mode t_7 : At this time, the S_3 anti-parallel diode has been on, and the switch S_3 should be turned on at this time. Therefore, the switch S_3 is the ZVS turn-on. Because the voltage at both ends of C_2 is the bus voltage, the voltage at both ends of switch S_4 is zero, and S_4 meets the condition of the ZVS turn-off. With the closing of S_4 , the energy stored in C_2 , L_3 , and L_4 is released back to the bus.

Mode t_8 : When the switch S_3 turns off, the voltage across the capacitor C_3 cannot change abruptly. Therefore, switch S_3 reaches the condition for the ZVS turn-off.

Mode t_9 : Because C_2 has stored enough energy before S_2 turns on, the voltage across S_2 is zero to meet the condition of the ZVS turn-on. Then, S_2 turns on and enters a new cycle.

3 Simulation data and analysis of an O-ARCP DC-AC power electronic converter in islanding mode

To verify the correctness of the analysis, the proposed three-phase ARCP inverter topology is simulated using MATLAB simulation software. Because some parameters of the three-phase circuit are the same, only one-phase parameters are listed.

The simulation parameters are shown in Table 1.

3.1 Parameter design when the load current direction is positive

3.1.1 Design of resonant inductor and resonant capacitor

The design of the L_1 and C_3 parameters depends on the resonant frequency f_r and the maximum load current I_{omax} , which must first be satisfied to achieve soft switching.

$$\frac{U_d}{Z_r} < I_{omax}.$$

Namely,

$$Z_r > \frac{U_d}{I_{omax}}.$$

The equation can be rewritten as follows:

$$Z_r = K \frac{U_d}{I_{omax}},$$

where $K > 1$, and the resonance duration period is defined by

$$T_r = \frac{1}{f_r} = 2\pi \sqrt{L_1 C_3}.$$

The auxiliary switch opening time cannot be less than t . t can be determined by the following equation:

$$t = \frac{1}{4} T_r = \frac{\pi}{2} \sqrt{L_1 C_3}.$$

Meanwhile, the duration of t should satisfy

$$t < t_{dead},$$

where t_{dead} is the dead time to prevent the upper and lower bridge arms from conducting at the same time.

Combining the aforementioned equations yields

$$t = K_1 t_{dead} = \frac{\pi}{2} \sqrt{L_1 C_3},$$

where $K_1 < 1$. It can be concluded that

$$C_3 = \frac{I_{omax}}{K U_d} \cdot 2K_1 \frac{t_{dead}}{\pi},$$

$$L_1 = \frac{K U_d}{I_{omax}} \cdot 2K_1 \frac{t_{dead}}{\pi},$$

where $K_1 < 1$ and $K > 1$.

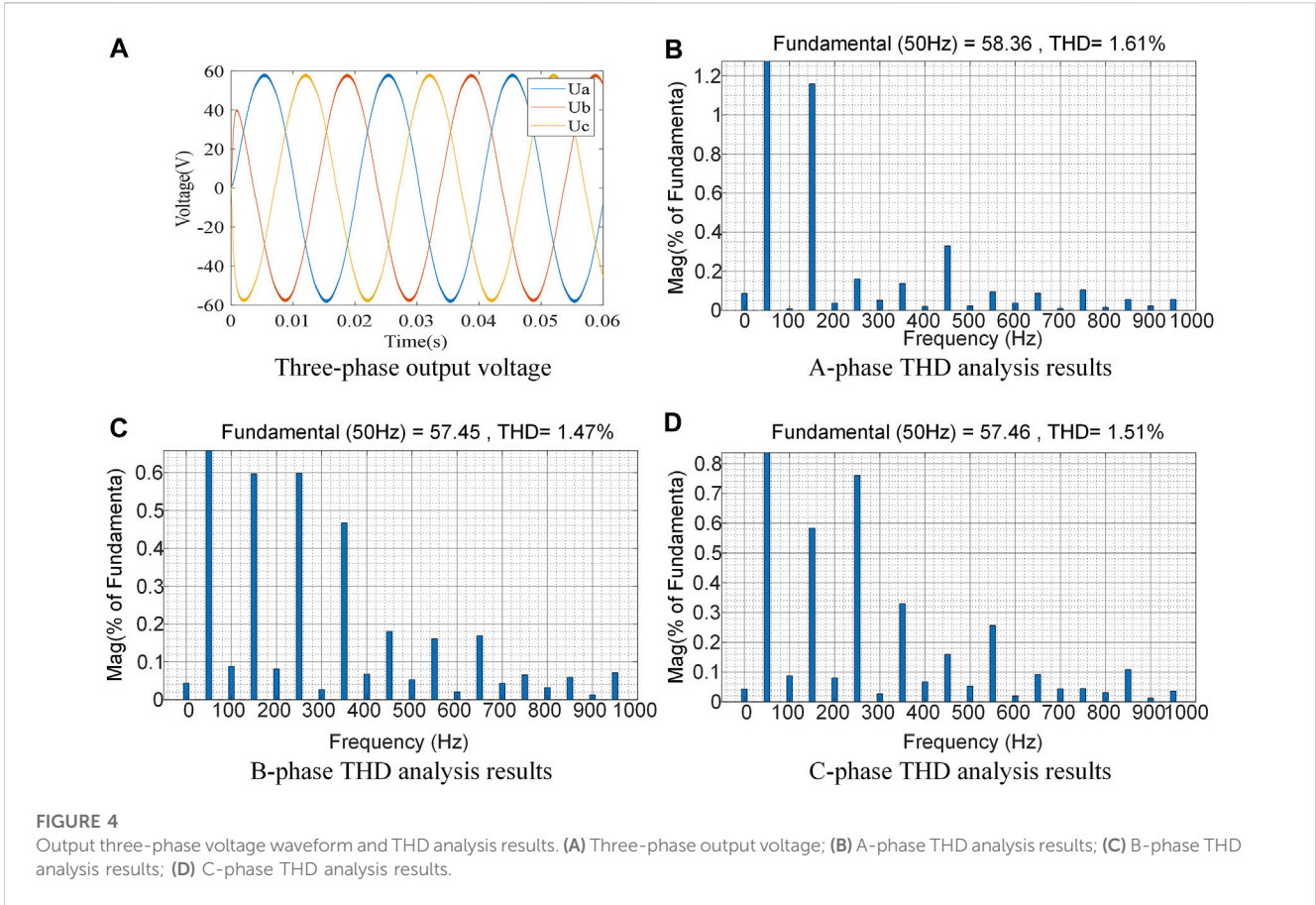


FIGURE 4 Output three-phase voltage waveform and THD analysis results. (A) Three-phase output voltage; (B) A-phase THD analysis results; (C) B-phase THD analysis results; (D) C-phase THD analysis results.

3.1.2 Parameter design of C1, L2

This phase has a small resonance duration, so only $t_1 < t$ needs to be satisfied.

$$t_1 = \frac{\pi}{2} \sqrt{L_2 C_2}.$$

Its peak resonant current can be given by

$$i_{L2} = \frac{U_d}{\sqrt{L_2/C_2}}.$$

The design should satisfy $i_{L2} < i_{L1}$ in order to reduce losses and current stress.

Therefore, it is obtained that

$$t_1 = K_2 t = K_2 \frac{\pi}{2} \sqrt{L_1 C_3},$$

$$i_{L2} = K_3 i_{L1} = K_3 \left(\frac{U_d}{Z_r} \sin \omega t + I_a \right),$$

where $K_2 < 1$ and $K_3 < 1$.

To simplify the design, i_{L1} can be simplified. This yields

$$L_2 = \frac{K_2}{K_3} L_1,$$

$$C_1 = K_2 K_3 C_3.$$

3.2 Parameter design when the load current direction is negative

The analysis process is the same as when the load current direction is positive.

$$L_3 = \frac{K U_d}{I_{omax}} \cdot 2 K_1 \frac{t_{dead}}{\pi},$$

$$L_4 = \frac{K_2}{K_3} L_3,$$

$$C_2 = K_2 K_3 C_3.$$

3.3 Simulation verification

The output three-phase voltage and its harmonic analysis are shown in Figure 4.

Figure 4A shows the output three-phase voltages, Figure 4B shows the results of the A-phase total harmonic distortion (THD) analysis with a value size of 1.61%, Figure 4C shows the results of the B-phase THD analysis with a value size of 1.47%, and Figure 4D shows the results of the C-phase THD analysis with a value size of 1.51%, which is not significantly different from the experimental tests in Section 4 and meets the design expectations.

Figure 5 shows the simulation diagram of the operation mode with positive load current direction, where the first picture shows

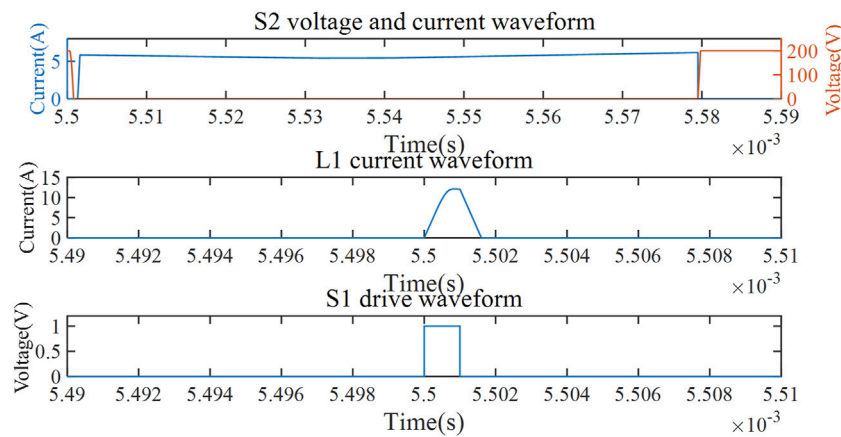


FIGURE 5
Key waveform with a positive load current direction.

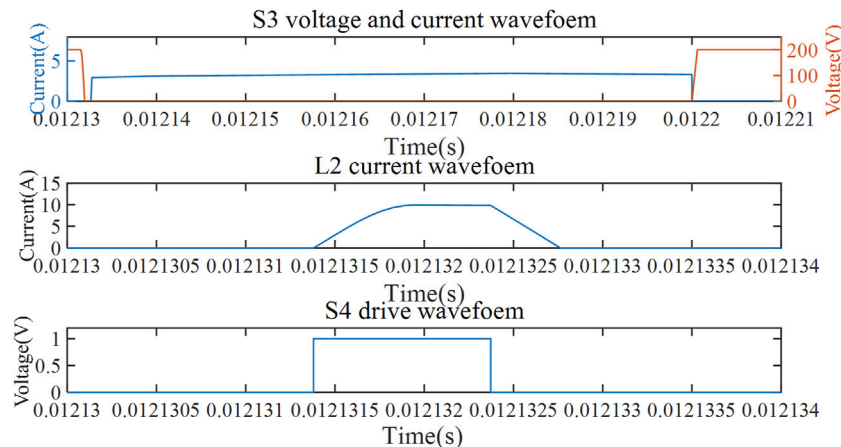


FIGURE 6
Key waveform with a negative load current direction.

the current and voltage waveforms on the switch side of S_2 , the second picture shows the current flowing through inductor L_1 , and the third picture shows the driving pulse of auxiliary switch S_1 .

A comparison with Figure 2 shows that the proposed topology achieves the desired soft-switching effect in the simulation verification.

Figure 6 shows the simulation diagram of the operation mode with negative load current direction, where the first picture shows the current and voltage waveforms on the switch side of S_3 , the second picture shows the current flowing through inductor L_2 , and the third picture shows the driving pulse of auxiliary switch S_4 . The comparison with Figure 2 is consistent with the analysis, and the desired soft-switching effect is achieved.

The first graph in Figure 7 shows the turn-off waveform of auxiliary switch S_1 in the operation mode with a positive load current direction. The second graph shows the turn-off waveform of auxiliary switch S_4 in

the operation mode with a negative load current direction. It can be seen that the proposed topology can satisfy the ZVS turn-off of the auxiliary switch and reduce the switching loss.

4 Experimental verification and analysis

Experimental verification was carried out to verify the correctness of the simulation strategy. In this verification, the parameters of the three-phase circuit were partially consistent, so only one-phase parameters are listed. The simulation parameters are shown in Table 2.

Figure 8 shows the hardware experimental platform of the proposed O-ARCP converter, including the basic circuits such as the main circuit, the auxiliary converter circuit, the filter, the main control circuit, and the driver circuit.

Figure 9 shows the output three-phase voltage waveform.

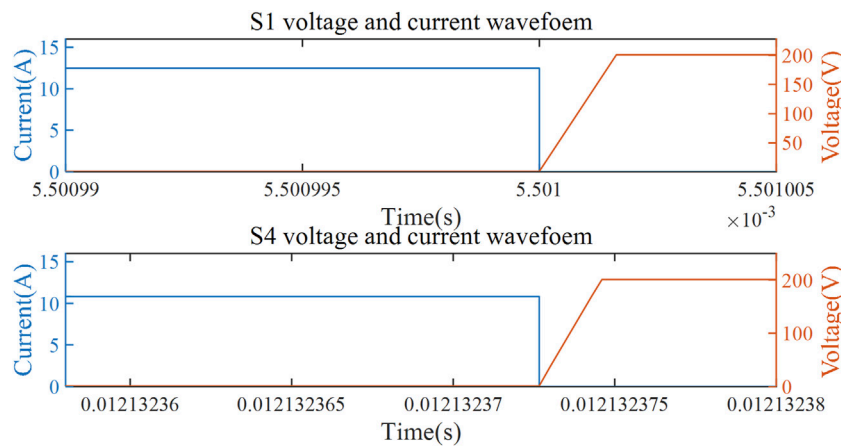


FIGURE 7 Auxiliary switch off waveform with positive and negative load current directions.

TABLE 2 Experimental parameters.

Component	Parameter
Control board	DSP TMS320F28335
S_1 – S_4	IRF640 (200 V, 18 A)
D_5 – D_{10}	SRA4E (400 V, 10 A)
Output power	500 W
DC voltage supply (U_d)	100 V
Switching frequency	10 kHz
Output frequency	50 Hz
Dead time	1.5 μ s
L_1, L_3	6.8 μ H
L_2, L_4	1 μ H
C_1, C_2	10 nF
C_3	100 nF

Figure 9A shows the inverter output three-phase voltage, and Figure 9B shows the inverter THD analysis results. From Figure 9A, we can see that the inverter output voltage waveform V_{pp} is 85.94 V, and the frequency is 50.01 HZ. As can be seen from Figure 9B, the THD analysis results for all three channels are 1% and meet the design criteria. The experimental results do not have large errors with the simulation results.

Figure 10 shows the experimental graph of the ZVS turn-on and the ZVS turn-off waveform.

Figure 10A shows the waveform diagram of the main switch ZVS turn-on moment, Figure 10B shows the waveform diagram of the main switch ZVS turn-off moment, and Figure 10C shows the waveform diagram of the auxiliary switch ZVS turn-off moment. The red lines represent the main switch drive signals, and the blue lines represent the voltage signals at both ends of the main switch.

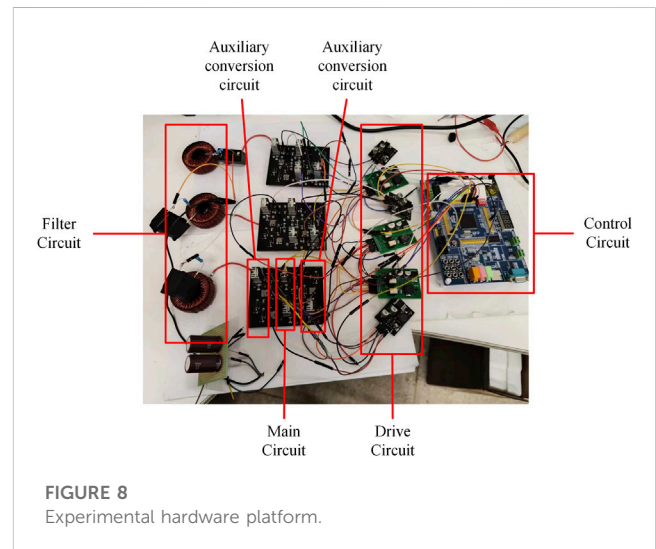


FIGURE 8 Experimental hardware platform.

It can be observed in Figure 10A that the voltage at both ends has changed to zero before the main switch is turned on. Therefore, the main switch meets the condition of the ZVS turn-on. In Figure 10B, after the main switch is turned off, the voltage at both ends is zero and rises slowly to the bus voltage after a period of time. Therefore, the main switch meets the condition of the ZVS turn-off. In Figure 10C, when the auxiliary switch is turned off, the voltage across the auxiliary switch is zero after taking approximately 2 μ s to reach the bus voltage. Therefore, the auxiliary switch meets the conditions for the ZVS turn-off.

5 Comparison and analysis of inverters

5.1 Comparison of the number of devices used

Table 3 compares the number of components used in the auxiliary circuit.

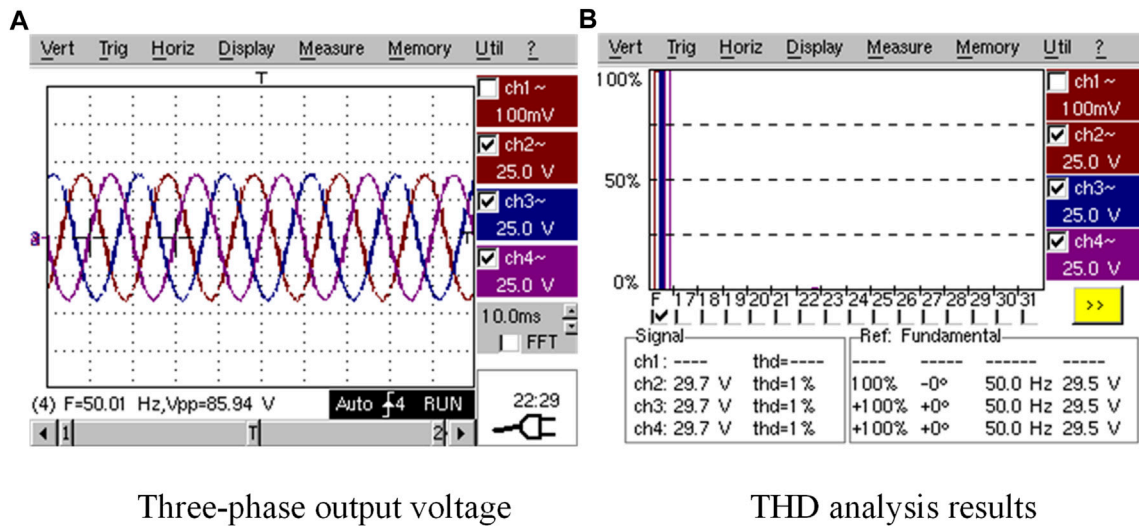


FIGURE 9 Three-phase voltage output and THD analysis results. (A) Three-phase output voltage; (B) THD analysis results.

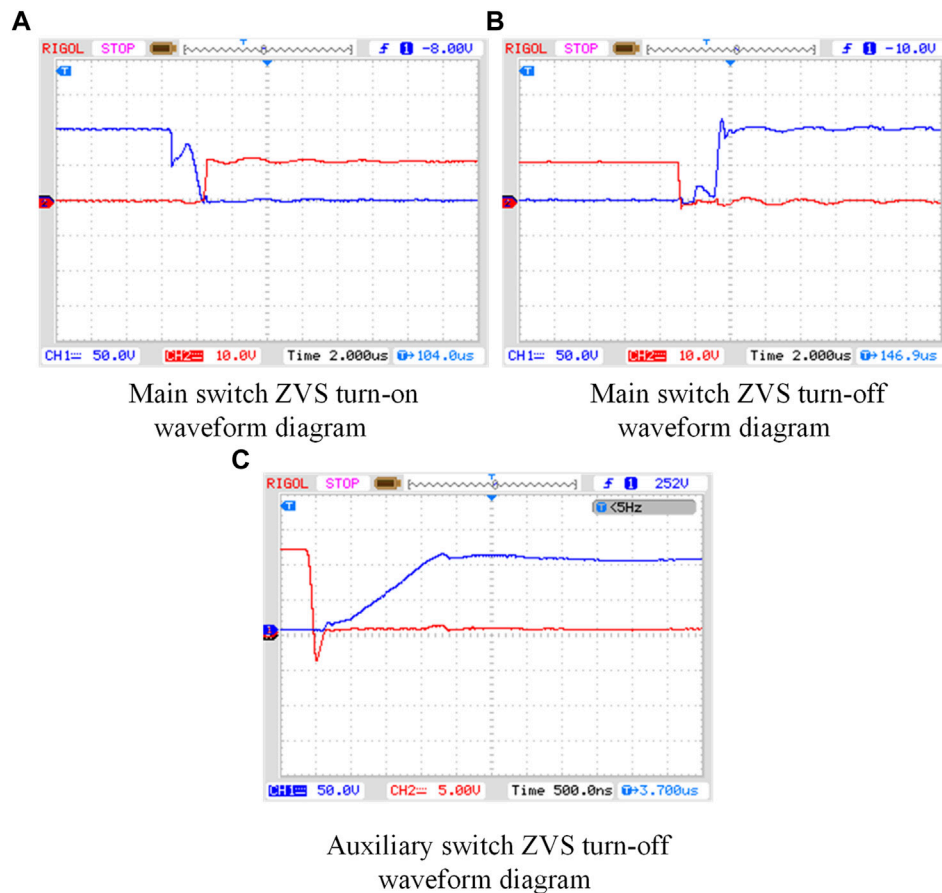


FIGURE 10 Experimental waveforms on both sides of the main and auxiliary switches. (A) Main switch ZVS turn-on waveform diagram; (B) Main switch ZVS turn-off waveform diagram; (C) Auxiliary switch ZVS turn-off waveform diagram.

TABLE 3 Comparison of the number of auxiliary components.

Number of components	Paper (Chu et al., 2014)	Paper (Cai et al., 2019)	Paper (Chu et al., 2016)	This paper
Auxiliary switch	12	12	6	6
Auxiliary diode	24	12	24	18
Resonant capacitor	18	12	18	9
Resonant inductor	12	6	12	12

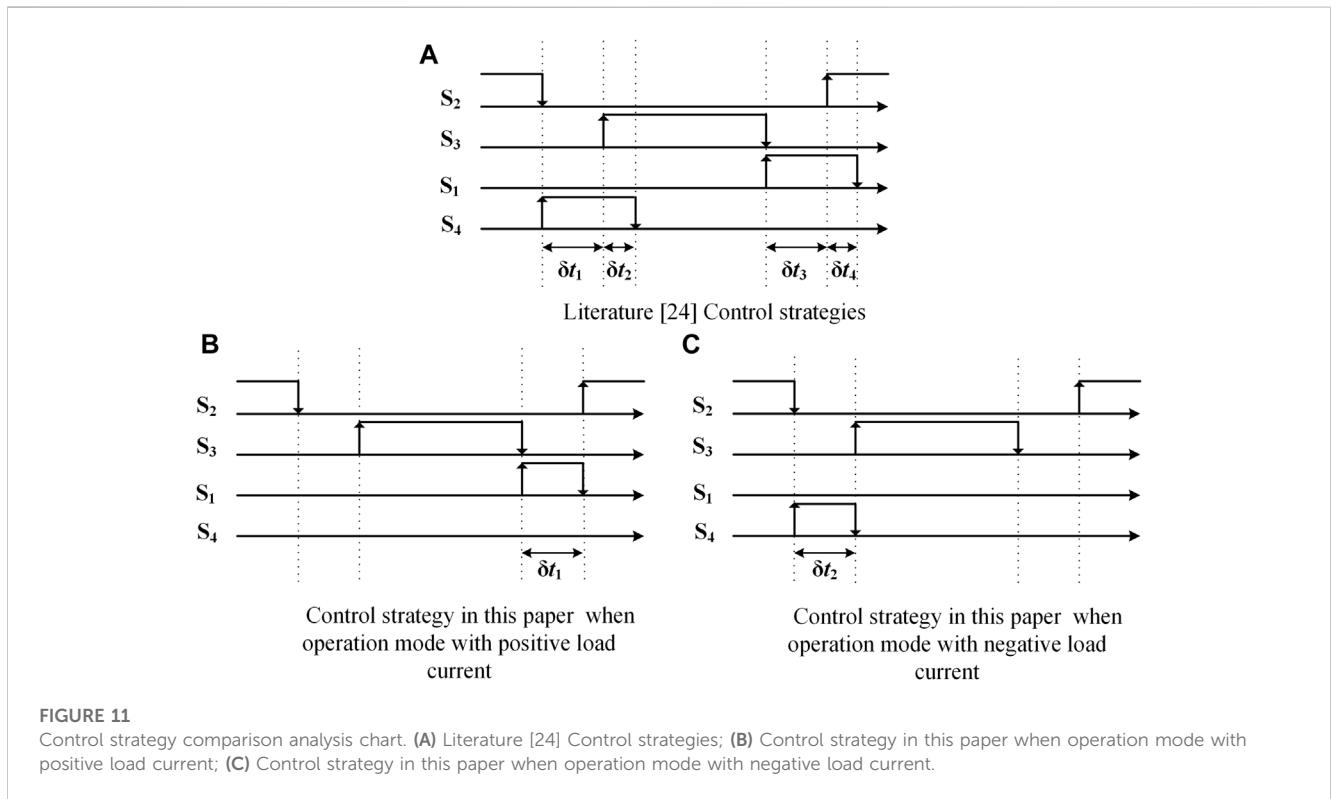


FIGURE 11 Control strategy comparison analysis chart. (A) Literature [24] Control strategies; (B) Control strategy in this paper when operation mode with positive load current; (C) Control strategy in this paper when operation mode with negative load current.

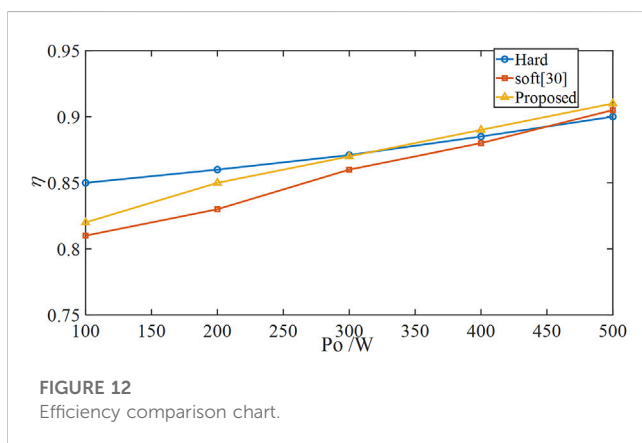


FIGURE 12 Efficiency comparison chart.

Under the control strategy proposed in this paper, only half of the components are working in each sine wave cycle on average, so in practice, three auxiliary switches are working in each cycle, in addition to nine auxiliary diodes, five resonant capacitors, and six resonant inductors. The two groups of devices work

alternately within the whole cycle, reducing the loss of the auxiliary circuit.

5.2 Comparative analysis of control strategies used

Figure 11 shows a comparison of the auxiliary switch control strategy described by Chu et al. (2016) and this paper. It can be seen from Fig. 11A that Chu et al. (2016) do not divide the action of the auxiliary switch into two moments according to the load current direction, and it is necessary to operate both switches S1 and S4 in one PWM cycle. In this paper, the control strategy is divided into two types according to the load current flow direction. Only the auxiliary switch S1 needs to be operated in each PWM cycle when the load current direction is positive, and only the auxiliary switch S4 needs to be operated in each PWM cycle when the load current direction is negative, thus avoiding the problem of operating both auxiliary switches S1 and S4 in each PWM

cycle. The control strategy described by Chu et al. (2016) is longer than the one proposed in this paper by one δt_2 and one δt_4 , and the losses generated by the auxiliary circuit in this control strategy are larger than those in this paper.

5.3 Efficiency comparison and analysis

Figure 12 shows the experimental efficiency curve of the proposed soft-switching inverter. When the output power is less than 300 W, both the soft-switching inverter proposed in this paper and the soft-switching inverter proposed by Chu et al. (2014) have less efficiency than the conventional hard-switched inverter. The reason is that the added auxiliary circuit generates more losses than the switching losses generated by the conventional hard-switched inverter.

When the output power is greater than 300 W, the efficiency of the soft-switching inverter proposed in this paper starts to be greater than that of the conventional hard-switched inverter. In contrast, the soft-switching inverter described by Chu et al. (2014) is still smaller than the conventional hard-switched inverter.

The main reason for this effect is that the number of auxiliary devices used in this article is less than that described by Chu et al. (2014). Therefore, the losses generated by the auxiliary circuits are smaller. The second reason is that the auxiliary switching control strategy used by Chu et al. (2014) is similar to that described by Chu et al. (2016). The control strategy in this paper has a relatively short operating time of the auxiliary circuit. As a result, fewer additional power losses are incurred.

6 Conclusion

An efficient soft-switching topology is proposed in this paper, and after theoretical analysis and simulation experiments, the following conclusions are drawn.

1. Compared with the control strategies proposed in the literature (Chu et al., 2014; Chu et al., 2016), under the control strategy proposed in this paper, only one set of auxiliary components is under operation in every half cycle, and the auxiliary components work only once in a cycle, which greatly reduces the losses due to the auxiliary circuit.
2. Compared with Chu et al. (2014), the proposed topology in this paper reduces the number of auxiliary components used and reduces the size and cost of the inverter.
3. It is verified by simulation and experiment that the transmission efficiency of the grid-connected inverter can be improved in grid-connected or islanded mode.

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Data availability statement

The original contributions presented in the study are included in the article/Supplementary material; further inquiries can be directed to the corresponding author.

Author contributions

CL and YW developed the idea. CL developed the theory, the calculations, and the simulations. YW supervised and reviewed this work. All authors contributed to the article and approved the submitted version.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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