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# Primary-side control for the flyback AC–DC converter

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This paper proposes a PSR flyback switching power supply AC/DC control chip with a maximum rated power based on the SMIC 0.18-μm CMOS process. The flyback power management system is based on pulse modulation technology working in the current discontinuous mode. The AC/DC control chip mainly includes a power supply module, clock signal generation module, constant voltage control module, constant current control module, driving module, and constant voltage and constant current mode switch module. The various module circuits of the system are analyzed and simulated. Compared with similar products, the system simulation results have advantages in some indicators.

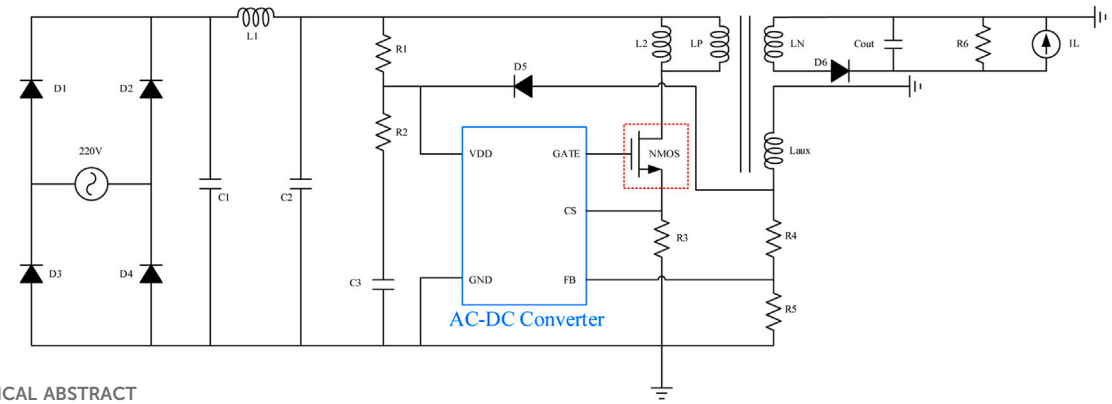
KEYWORDS

**flyback converter, primary-side feedback, AC/DC, CMOS, integrated circuits**

## 1 Introduction

In recent years, with the rapid development of electronic information technology, people's demand for alternating current/direct current (AC/DC) power chips is growing rapidly. AC/DC is increasingly required to have higher safety and reliability while ensuring performance. At present, the flyback converter and forward converter are common low-power energy conversion circuits. Because of their advantages of simple structure, low cost, and low standby power consumption, they are widely used in AC and DC power adapters and other power management systems (Kawauchi and Tanzawa, 2020; Ye and Tanzawa, 2020; Ishida and Tanzawa, 2021; Zhou et al., 2021). On one hand, their topological structure based on the unique application of transformers to the input and output of the system has excellent electrical isolation effect, avoiding the high-voltage input part and low-voltage output part of the system and the ground wire short circuit caused by the potential safety hazards, compared with the non-isolated power system and isolated power system, therefore having higher security and reliability. On the other hand, the design of the forward converter and flyback converter is flexible and changeable. The operating point of the system can be directly determined according to the ratio of turns of the inductor on both sides of the transformer. The system has a wide voltage input and output range, and a high voltage current change ratio (He et al., 2019). Combining these two advantages, the flyback converter and forward converter are widely regarded in power supply engineering design. Flyback topology in the same switching cycle, the original with vice and the inductance of the induced electromotive force polarity, will be adaptive to change and does not need extra inductance reset circuit (Chang et al., 2019). Therefore, the flyback converter has the advantage of simple structure compared with the forward converter (Tang et al., 2021a; Chen et al., 2021; Leng and Chiu, 2021; Wu et al., 2021).

Flyback converters are classified into primary-side regulated (PSR) flyback converters and secondary-side regulated (SSR) flyback converters, according to different output feedback methods. Traditional SSR converters need optical couplers and high-precision voltage sources to achieve accurate detection and transmit the sensing output information to




GRAPHICAL ABSTRACT
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the control integrated circuits (ICs). Although it is easier to obtain higher output accuracy in this way, it makes the circuit structure more complex (Jung and Cho, 2014). At the same time, under the condition of high temperature, the current transfer ratio of the optical coupler will be greatly reduced, which has a great influence on the output precision of the system. The PSR system has good reliability, security, and anti-interference, and has the advantages of simple structure and low cost, and there is no need for optical couplers and precision voltage sources (Li and Chen, 2013). Therefore, more and more researchers apply PSR flyback to the power management system.

Chao Chang Chu from National Chiao Tung University put forward self-calibrated knee voltage detector (SC-KVD) technology (Chiu et al., 2014). The sampling accuracy of the auxiliary winding is greatly improved by changing the resistance partial voltage of the feedback loop to dynamically adjust the delay time of the RC network. Ali Shagerdmootaab from Simon Fraser University in Canada proposed a serial primary-side control structure for driving high-brightness LED (HB-LED) at constant power (Shagerdmootaab and Moallem, 2015). An inner–outer loop control structure is designed by using an AC/DC flyback connected to LED. Double feedback control loop and input current are used to adjust LED power. The input voltage and duty cycle of the flyback power supply are used to estimate the LED power without measuring it from the secondary side or the secondary winding side of the flyback power supply, which effectively simplifies the peripheral circuit design. At the same time, the amplitude analysis method of input current is given, and the output power can be adjusted by changing the amplitude of current.

Wei–Cheng Su of National Cheng Kung University reduced the total harmonic distortion of the PSR system in the critical conduction mode and improved the power factor through the digital variable real-time feedback control scheme (Liang et al., 2017). Minggang Chen et al. of the University of California, proposed a digital pre-feedback control method without feedback resistance, and described the stability of the feedback control method and its influence on the dynamic response of the system. The design scheme of the power switch reverse guide pass was proposed, and the feasibility of the proposed control scheme was verified by FPGA to further improve the application flexibility of primary-side feedback (Liu et al., 2021). In the same year, Yeran Liu of the University of London proposed a parameter estimation method suitable for the bidirectional induction power transmission primary-side system. This method can estimate the inductance value when the circuit is started and monitor the secondary winding change continuously during the operation. The response speed and output precision of the system are optimized through necessary feedback information. In addition, a circuit analysis model based on the superposition principle and current mutual inductance is proposed to describe the concept of current decoupling (Memon et al., 2018).

In 2021, Tang et al. (2021b) proposed a PSR CV flyback based on the seamless mode switch control scheme with a capacitor-less self-adaptive startup, which minimized the peripheral components and increased the system stability for a full-load range. PFM and DPWM are adapted to reduce the standby power, and the seamless control scheme assures the continuity during the mode switch period. An ultralight load is realized at 0.008 A, while the output voltage accuracy is within ±0.98% under different input voltages and loads, and the acceptable peak power efficiency is 88.52%. In 2023, Li et al. (2023) proposed an adaptive multimode control scheme for higher average efficiency and wider power range applications, without having to compromise on other system performance. The average efficiency was 88.52%, whereas peak efficiency can reach 89.65%. The deviation of the output voltage was within ±2.33%.

According to the development of PSR technology, in addition to the advantages of high output accuracy, low standby power consumption, and low noise, the power supply system also needs to have a wider input and output range, high integration, and high efficiency, so the primary-side feedback technology still has a great space for development and necessary research.

The remainder of the paper is organized as follows. The system design of the chip is described in Section 2. The detailed circuit implementation is shown in Section 3. Section 4 reveals the simulation results. Finally, the conclusion is presented in Section 5.

## 2 System design

Figure 1 shows the application structure of the chip peripheral circuit, which is the structure of Shen et al. (2011). This is a flyback power management system based on pulse modulation technology working in the current discontinuous mode.

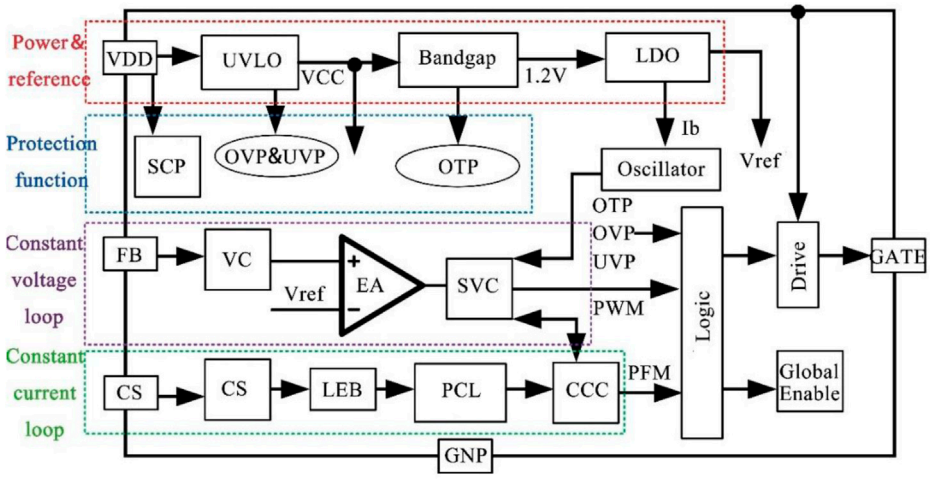


FIGURE 1
Chip internal architecture.

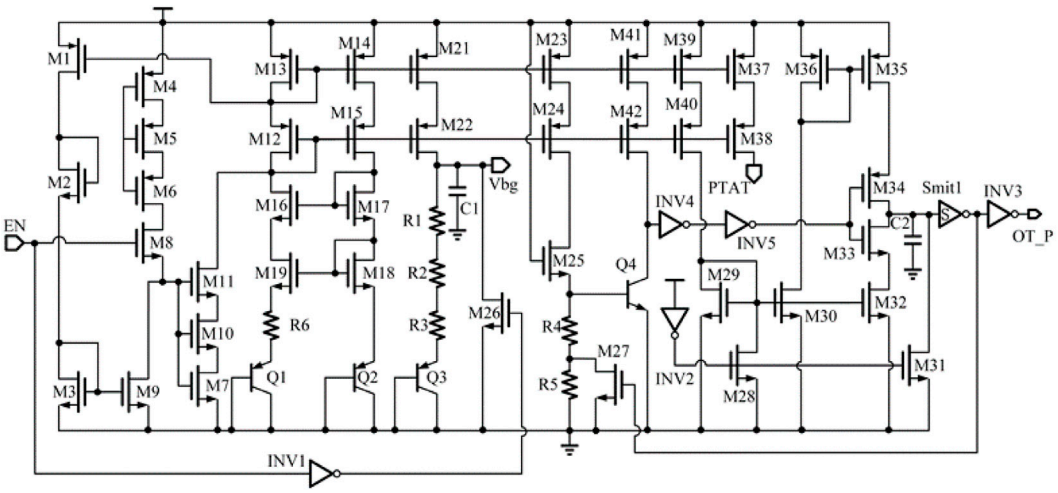


FIGURE 2
Over-temperature protection bandgap reference source circuit.

The chip leads to five pins, among which the CS pin mainly reflects the output current information as the main feedback end of the chip's internal peak current limiting circuit and constant current control circuit. The FB end comes from the auxiliary winding LA partial voltage, mainly reflects the output voltage information, and serves as the feedback input end of the error amplifier in the constant voltage control circuit inside the chip. In the selection of the switching power transistor, the SMIC process is used to customize NMOS devices, which show excellent performance such as high voltage resistance and high temperature resistance, and are integrated in the chip. Meanwhile, the number of passive devices on the peripheral circuit of the chip is small, which can minimize the PCB area and reduce the difficulty of layout and routing, and has a high degree of integration, which effectively reduces the parasitic inductance effect caused by too many PCB wiring layers.

When the circuit is in the first stage of power, through the bridge rectifier circuit AC/DC conversion, the rectifier circuit is composed of four diodes in series, which will be 220 V AC mains power conversion system used by the DC voltage. $L_1$ and $C_2$ constitute a basic RC filter circuit to reduce voltage ripple. Resistor $R_1$ is the startup resistor with a resistance value of 2 MΩ. When the system starts up at the beginning, this resistor will play a role of current limiting and the voltage divider to provide a relatively stable startup voltage for the chip. At this time, capacitor $C_3$ is charged. When the $C_3$ potential gradually increases to the threshold value of the internal startup circuit of the chip (the startup circuit of the chip is the under-voltage latch circuit), the chip starts to work, and the output voltage will start to increase. The starting branch

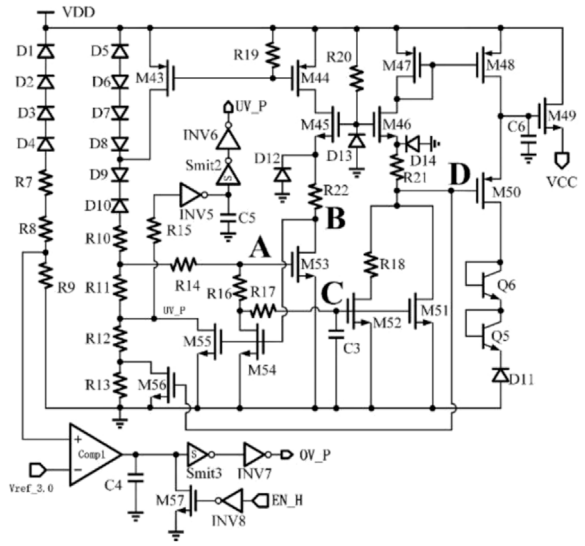


FIGURE 3
Fast positive feedback over-voltage protection and under-voltage lockout circuit.

of the chip is a high-power DC branch input from high voltage to ground. During the operation of this branch, resistance $R_1$ will cause large thermal noise, which is not conducive to the stability of the chip power supply. On the other hand, this large resistance has a high temperature coefficient, which will generate more heat energy and greatly increase the power consumption while working under high pressure for a long time. In order to solve this problem, the system designs another power supply branch of the chip. When the chip works stably, the high-voltage branch will not be used to provide voltage. At the output end FB, the chip is powered by the small voltage of the auxiliary winding LA. This energy recovery method not only ensures the stability of the chip power VDD but also effectively improves the energy utilization rate and saves power consumption.

The RCD absorption network of the flyback switching power supply system is composed of resistance $R_6$, $C_{out}$, and Zener diode $D_6$, which can effectively absorb the peak and peak current generated by the leakage inductance effect at the moment of the end of the primary inductor excitation, and prevent it from causing breakdown to the chip and the switching power transistor. The output end of the auxiliary winding $L_{aux}$ is connected to the chip power supply VDD, and no chip provides a part of power consumption, while $R_4$ and $R_5$ constitute partial voltage sampling as the input of the chip FB port.

Figure 1 shows the internal architecture of the chip, from which we can see the connection relationship between the core sub-modules and how they work (Li and Chen, 2013).

When the supply voltage VDD began to produce electricity, to 18 V, the UVLO circuit begins to produce 6 V and stable internal dc power supply, and at the same time will open the over-voltage protection and under-voltage latch function, when the power supply voltage stability can trigger the logic circuit in the global circuit and bandgap reference circuit began to offset for each module and the reference voltage or current. Each sub-module circuit began to work normally after the benchmark was established.

In the initial stage of power up, in order to establish the static working point as soon as possible, the system will enter the constant current mode and use the maximum output efficiency to initialize the internal capacitor. At this time, the output voltage will gradually rise and the FB feedback voltage will also change. When the output of EA is flipped, the system will enter the constant voltage mode. The voltage feedback loop starts to adapt to changes in load.

When protection signals such as over-voltage protection, under-voltage lock, and over-temperature protection are triggered, the system logic circuit immediately shuts down the system to ensure safety and starts to power on the system within the preset recovery range.

# 3 Circuit implementation

## 3.1 Power supply module

### 3.1.1 Over-temperature protected bandgap reference voltage source circuit

Figure 2 shows the bandgap reference voltage source circuit, which provides the over-temperature protection circuit. $M_1$–$M_{11}$

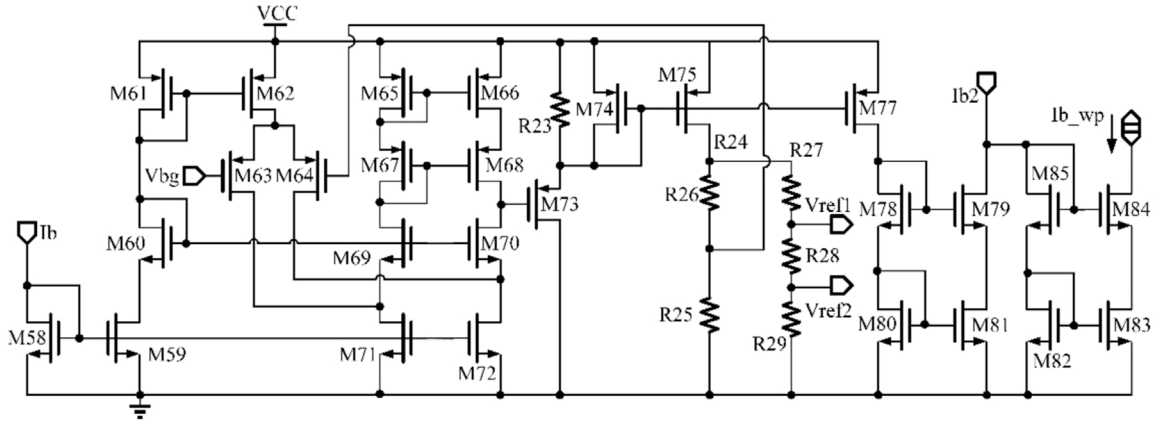


FIGURE 4
Buffer-LDO circuit.

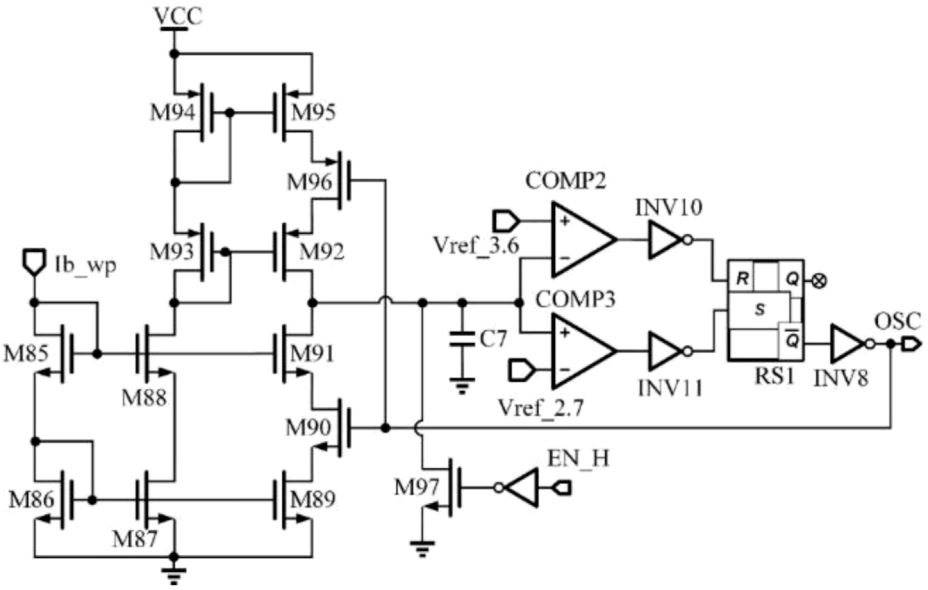


FIGURE 5
Clock signal generation circuit.

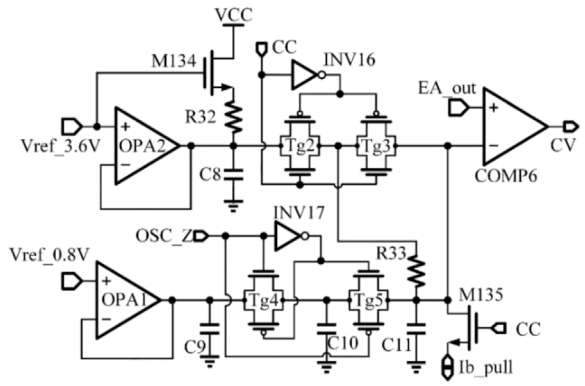


FIGURE 6
Constant voltage control circuit.

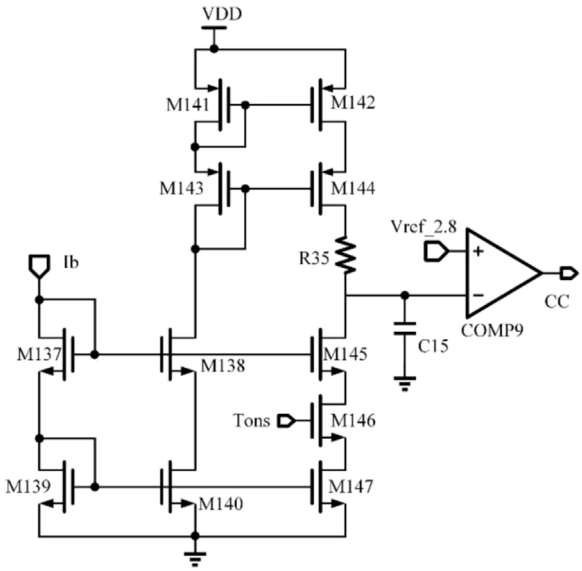


FIGURE 7
Constant current control circuit.

and $M_{26}$ are the starting circuits of the module. When the enable signal EN_H is high, $M_8$ conducts on and pulls down the gate potential of $M_{11}$, and the bias circuit starts to work. $M_{12}$–$M_{19}$ is a folded common-source common-gate current structure, in which $M_{13}$ and $M_{12}$ use long channel devices to reduce noise. This structure lends four overdrive voltages in exchange for gain and through the current mirror feedback effect to make the bipolar transistor $M_{18}$ and $M_{19}$ source level potential equal to improve the output accuracy of the circuit. $Q_2$ is eight triodes in parallel, and $Q_3$ and $Q_1$ are the same as the output branch. When the circuit is working, the base-emitter voltage of the three-stage tube meets the following formula.

$$V_{BE1} + IR_6 = V_{BE2}, \tag{1}$$

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = IR_6 = V_I 1n8, \tag{2}$$

where $R_6$ is the cross-voltage resistance, so the output voltage $V_{bg}$ is

$$V_{bg} = \frac{V_I 1n8}{R_6}(R_1 + R_2 + R_3) + V_{BE3}. \tag{3}$$

The bandgap circuit uses the PTAT current source proportional to absolute temperature to achieve the function of over-temperature protection. $Q_4$ is used as the input reference current for comparison with the output current of $M_{42}$. When temperature increases, the output current is increased by $M_{42}$ more than $Q_4$ can undertake after

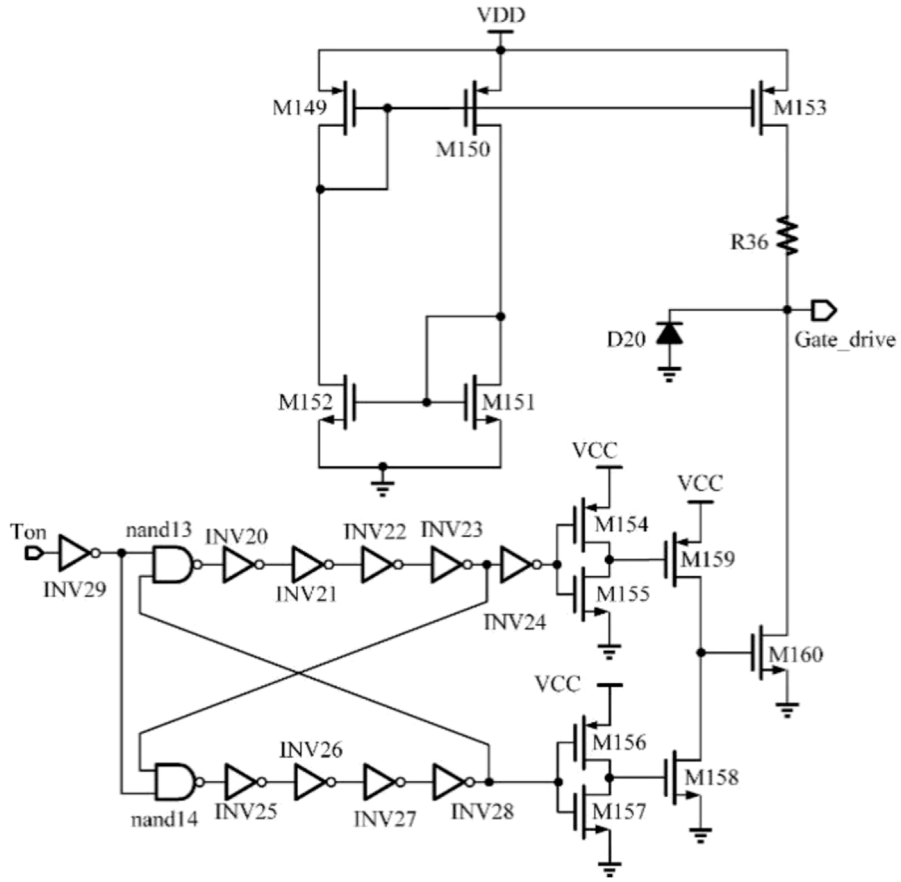


FIGURE 8
Driving circuit based on non-overlapping clock.

the maximum current because $M_{42}$ grid potential for fixed bias only cuts $M_{42}$ drain voltage increase channel modulation effect reduced to adapt to the reference output current; when the temperature reaches set threshold, the inverter INV4 level began to turn; $M_{32}$–$M_{35}$ adopts the push–pull amplification structure to enhance the load capacity of the turn-off signal. $R_5$, $M_{27}$, and $M_{31}$ are temperature reset circuits, and the recovery temperature point is set according to $R_5$. After the protection action starts, the $M_{27}$ gate voltage becomes low and cuts off, $Q_4$ base potential is raised, and the reference current threshold is changed. When the temperature drops to the new threshold, power is on again. It should be noted that the temperature protection point and the recovery point should not be the same because at the same time, the electricity passes through the temperature and restores to the temperature of the protection point and starts to work. If the temperature rises again, the circuit will be directly shut off, so the recovery point should be set lower than the protection point. The recovery point of this circuit is set 20 °C below the protection point.

### 3.1.2 Positive feedback quickly starts the under-voltage latch circuit

The circuit design of UVLO is shown in Figure 3, where EN_H is the enable signal and the high level is active. $D_1$–$D_{10}$ are 7.4 V Zener diodes, which are connected in series with resistors $R_9$–$R_{14}$ as the voltage divider sampling circuit of the power supply. The UVLO circuit improves response speed through its double feedback loop. The 7.4-V Zener diode has a predictable reverse breakdown (avalanche breakdown) voltage, which has good temperature stability. These diodes usually have very low noise if kept in a low temperature range, and its forward conduction voltage is 0.6 V. The Zener diode forward and reverse conduction modes are connected in series with the resistance to obtain the over-voltage protection threshold point OVP and the under-voltage protection threshold point UVP by the VDD stable voltage division, and meet the following formula.

$$OVP \cong (VDD - 4 \times 7.4)\frac{R_9}{R_9 + R_8 + R_7}, \tag{4}$$

$$UVP \cong (VDD - 2 \times 7.4 - 4 \times 0.6)\frac{R_{10}}{R_{10} + R_{11} + R_{13}}. \tag{5}$$

The number of diodes used depends on the turning point of the comparator and the threshold voltage of M53. The reasonable configuration meets the preset opening and closing thresholds. When the VDD voltage is very high, OVP potential rises as the input of the comparator, and compared with the reference voltage $V_{REF}$, the comparator output reverses. Comparator output through Schmidt trigger and $C_4$ hysteresis filter ripple and output control level. For the under-voltage protection circuit, the sampling voltage

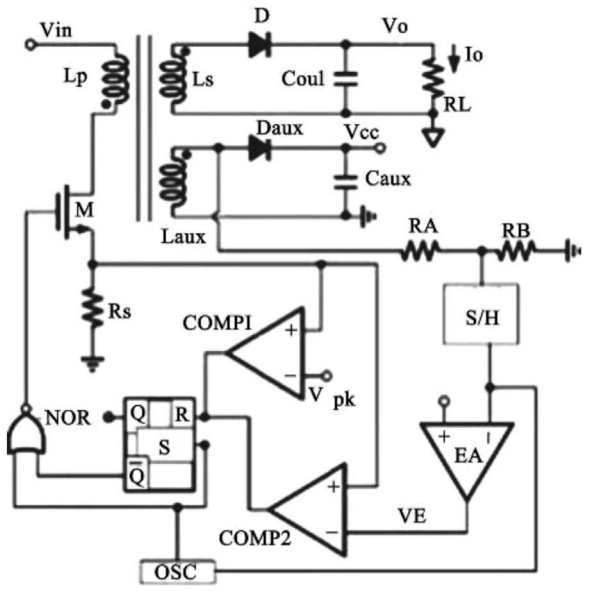


FIGURE 9
Constant voltage and constant current switching circuit.

decreases with the decrease of VDD, and the secondary circuit adopts Schmitt trigger structure to realize hysteresis and then realizes the protection function.

Two positive feedback loops are used to enhance the transient response of the UVLO circuit to improve the power-on speed of the circuit. After the circuit is energized, VDD climbs the slope and rises. When the potential of point A is enough for $M_{53}$ to conduct, the potential of point B is greatly reduced by the action of the common-source stage reverse amplifier, and $M_{55}$ cuts off to further raise the potential of point A. At the same time, $M_{51}$ and $M_{52}$ are on, and the potential of point D is directly pulled to the ground potential to make $M_{56}$ cut off, and the potential of point A is raised again. After $M_{50}$ is on, the circuit outputs VCC, the internal power supply of the chip. $R_{17}$ and $C_3$ are the basic RC filter circuits, and the filtered ripple generates delay. In this way, the potential of point C and point D will change after the potential of point A increases, ensuring that there is enough voltage margin at point A, when the VCC output is established to ensure the stability of the system. $D_{14}$, $D_{11}$, and $D_{12}$ as 6-V voltage regulators have the functions of clamping the input voltage peak, maintaining the voltage between the M49 grid and source to not exceed 6 V, and preventing internal power fluctuations.

### 3.1.3 LDO circuit

The circuit structure of LDO is shown in Figure 4. $V_{bg}$ is the 1.2 V bandgap reference voltage, and $M_{63}$–$M_{72}$ acts as a folded common-source common-gate high-gain amplifier. The feedback voltage of $R_{25}$ and $R_{26}$ is compared with $V_{bg}$, and the power-modulated transistor $M_{75}$ is driven to adjust the output voltage. This circuit incorporates an adaptive source follower structure, consisting of $M_{73}$–$M_{75}$ and $R_{23}$. The source follower has a very low output resistance, thus increasing the load capacity of the LDO. $M_{74}$ and $M_{75}$ are proportional current mirror structures, and the width length ratio of $M_{74}$ is set as 1/5 of $M_{75}$. Under light load, $R_{23}$ provides bias voltage for $M_{73}$ to prevent linearity of $M_{73}$ due to very small output current. Under the heavy load condition, the $M_{74}$ drain current increases and $M_{73}$ source potential increases to enhance the current load capacity. After adding the buffer, the load capacitance of the error amplifier is effectively reduced, and its static power consumption is reduced. It is easier to make the secondary point $P_2$ close to the zero point $Z_0$, thus improving the loop stability. However, the third pole is introduced. When the load resistance $R_L$ decreases, the main pole moves to the right, and the system stability will decline. Therefore, the third pole will appear outside GBW as far as possible to prevent the adjacent poles from being too close and unstable. In addition, under the condition that the current of the

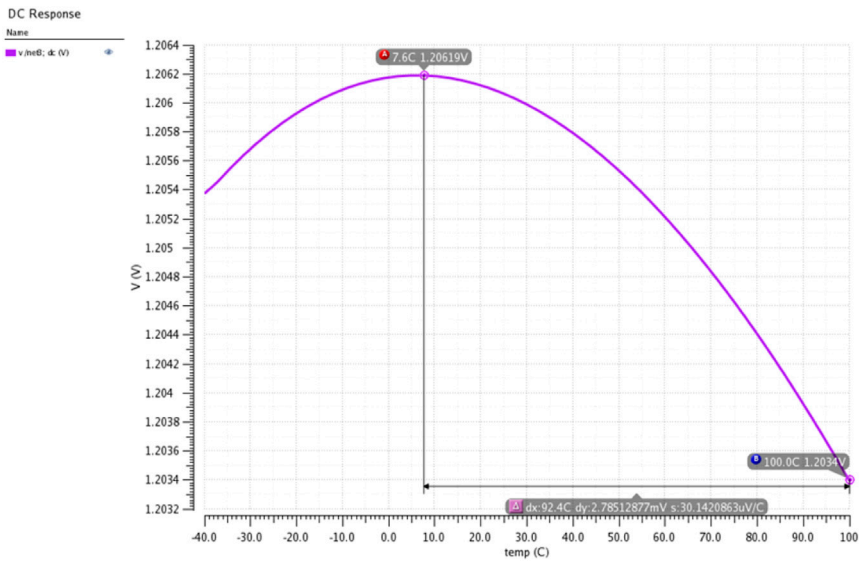


FIGURE 10
Simulation of the temperature coefficient of the bandgap reference voltage.

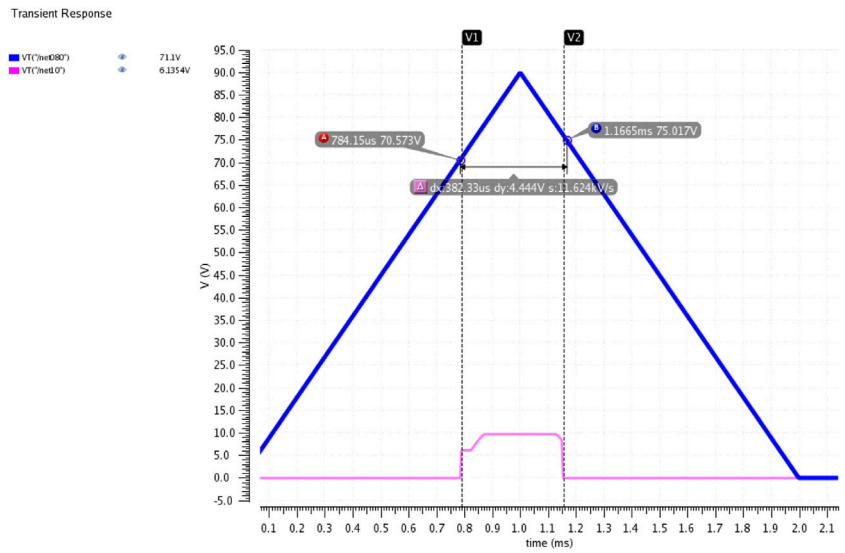


FIGURE 11
Simulation of over-voltage protection and under-voltage protection of the UVLO circuit.

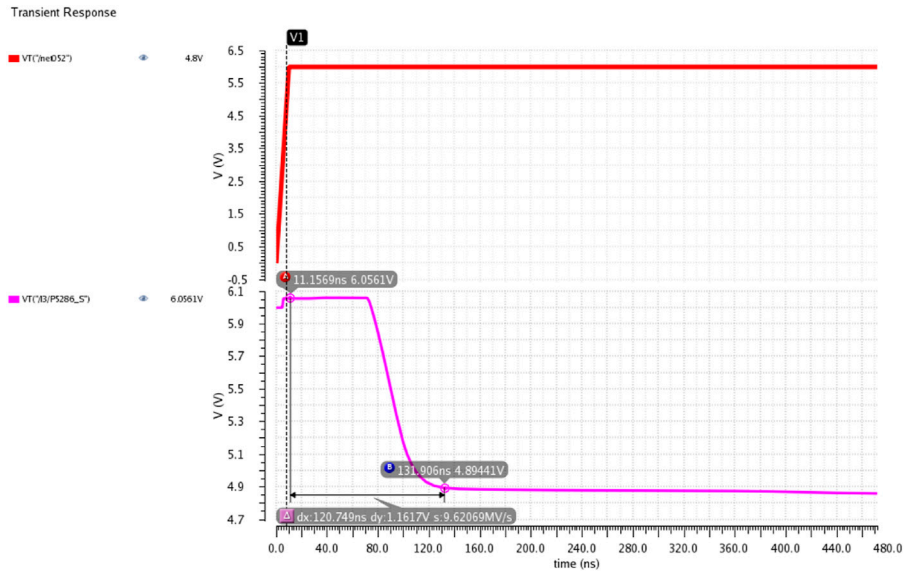


FIGURE 12
LDO transient response speed simulation.

smaller $R_L$ buffer is as large as possible, the system stability is improved, but the efficiency is reduced under light load.

## 3.2 Clock signal generation module

Figure 5 shows the system clock signal generation circuit of the AC/DC control chip in this paper. This module design uses stable low-temperature drift current to charge the capacitor, and controls the charge and discharge loop, according to the feedback logic to generate periodic stable sawtooth wave signals. The high-gain comparators COMP2 and COMP3 are used in the module design. The amplitude of oscillation is determined by the reference input of the two comparators. The high-gain comparator has the advantages of fast and stable transient response, which is suitable for the design of the oscillation circuit.

## 3.3 Constant voltage control module

Figure 6 shows the schematic diagram of constant voltage circuit design. The constant voltage control module can adapt

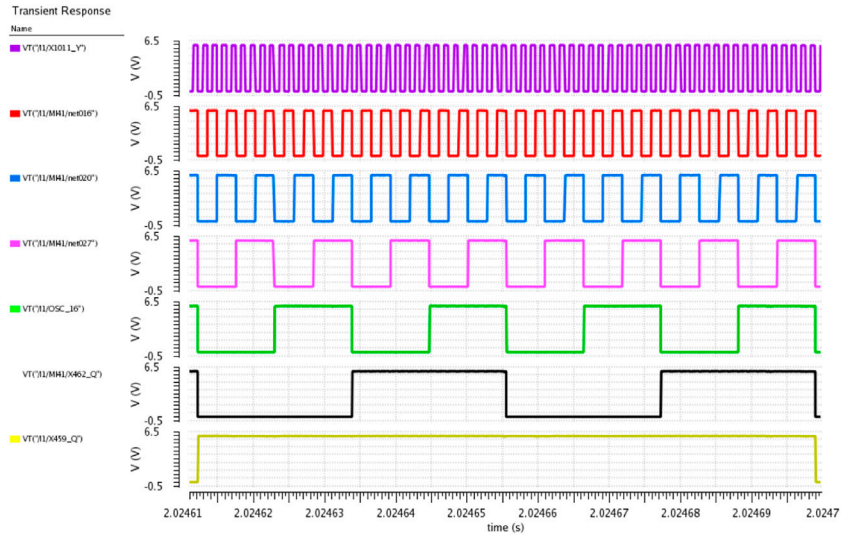


FIGURE 13
Simulation of the oscillator and the frequency division circuit.

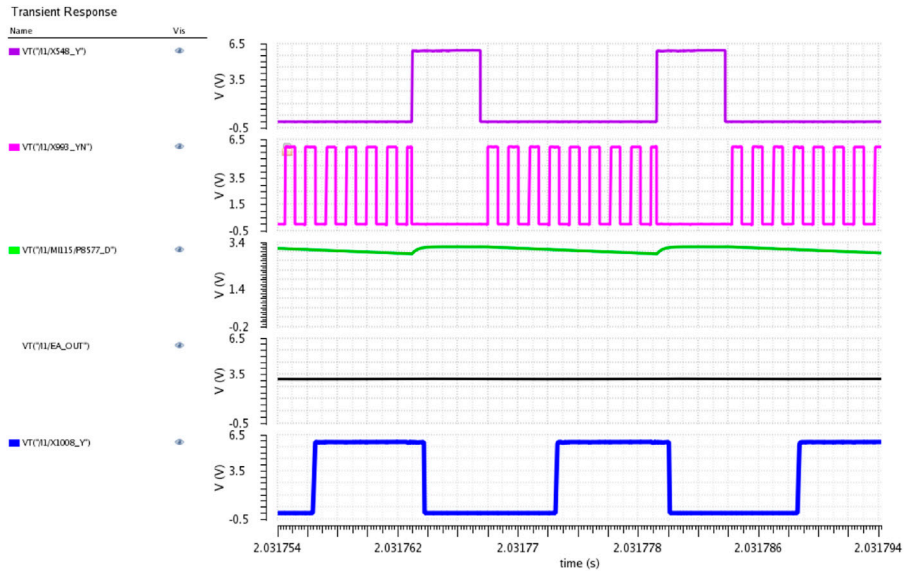


FIGURE 14
Transient simulation of the constant voltage control circuit.

to load frequency conversion modulation, when the error amplifier output is greater than 3.7 V, the circuit from the $C_C$ constant current mode to $C_V$ constant voltage mode. The constant piezoelectric routing PWM comparator COMP6, frequency switch transfer gates Tg4 and Tg5, and capacitors $C_9$–$C_{11}$ composed of a sampling hold circuit and a secondary source amplifier clamp circuit OPA1 and OPA2. The fixed-frequency fluctuation of 3.6 V and 0.8 V reference voltages through the transmission gate is used as the reference frequency voltage. In the process of circuit startup, in order to quickly initialize the digital circuit inside the chip, after the internal power supply VCC is powered on, the secondary amplifier OPA and $M_{134}$ will quickly charge $C_8$ and $C_{11}$ to initialize. $C_C$ is the constant current control circuit output signal; the system loop and constant pressure loop separation is not independent, even if the circuit works in the constant voltage mode, and the $C_C$ signal also can adapt to the load output feedback and adjust at any time, and produce adaptive variable frequency of reference voltage; when the load changes hours, the constant current circuit needed to maintain large offset current, expand the $C_C$ signal pulse width, and control the discharge time of the capacitor $C_{11}$ so that the reference frequency reference voltage fluctuates between 0.8 and 3.6 V.

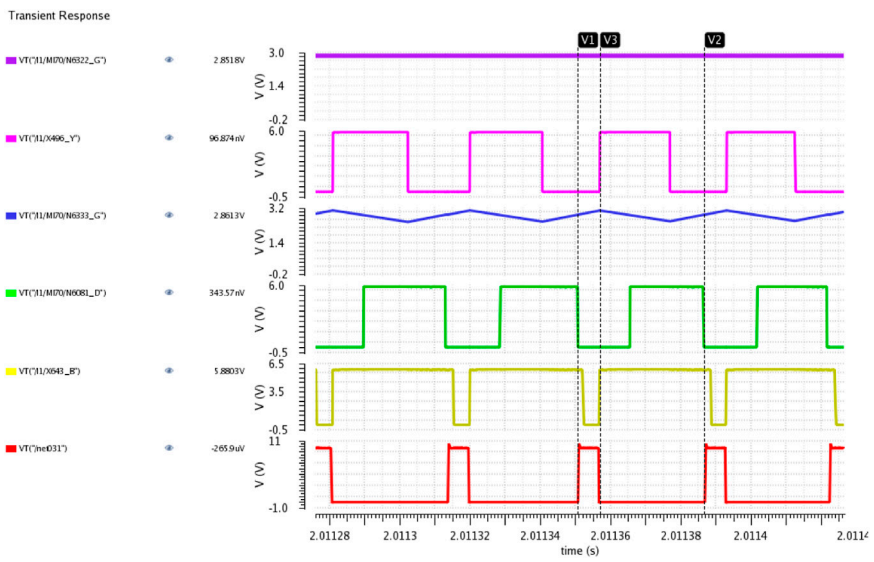


FIGURE 15
Transient simulation of the constant current control circuit.

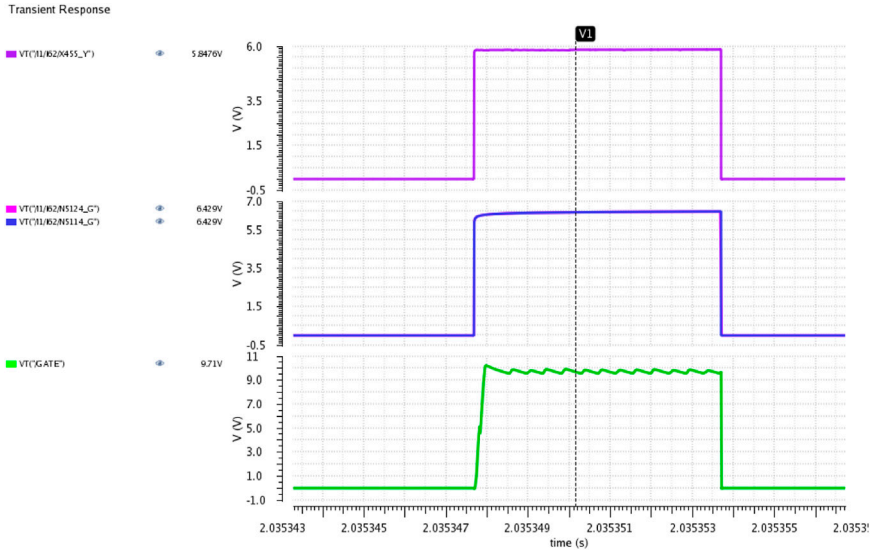


FIGURE 16
Simulation of the drive circuit.

## 3.4 Constant current control module

Figure 7 shows the design of the constant current control circuit. Based on the structure of proportional current mirror, fixed sawtooth wave signals are realized for capacitor charge–discharge. The charging branch of the capacitor is composed of $M_{142}$ and $M_{144}$, and the discharge branch is composed of $M_{145}$, $M_{147}$, and discharge control tube $M_{146}$. The charging branch does not design the input of the charging switch signal but sets the width and length ratio of $M_{145}$ and $M_{147}$ as twice that of the current mirror input tubes $M_{137}$ and $M_{139}$; in other words, the single discharge current is twice the size of the charging current. When TONS is low, the current mirror charges the capacitor. When the capacitor is charged to a reference voltage of 2.8 V, the comparator COMP9 outputs the reversed level. At this time, the power switching transistor is turned on again, generating TON signal rising edge, ending the cycle. At this point, the capacitor starts to discharge, and the discharge current is the sum of $M_{142}$ and $M_{144}$–$M_{147}$ branch current. The same charging current and discharge current are maintained, and waited until the primary inductor excitation ends and the TONS reaches a low level to start the next charging cycle. In other words, the peak current limiting module determines the pulse width of TON, that is, the length of

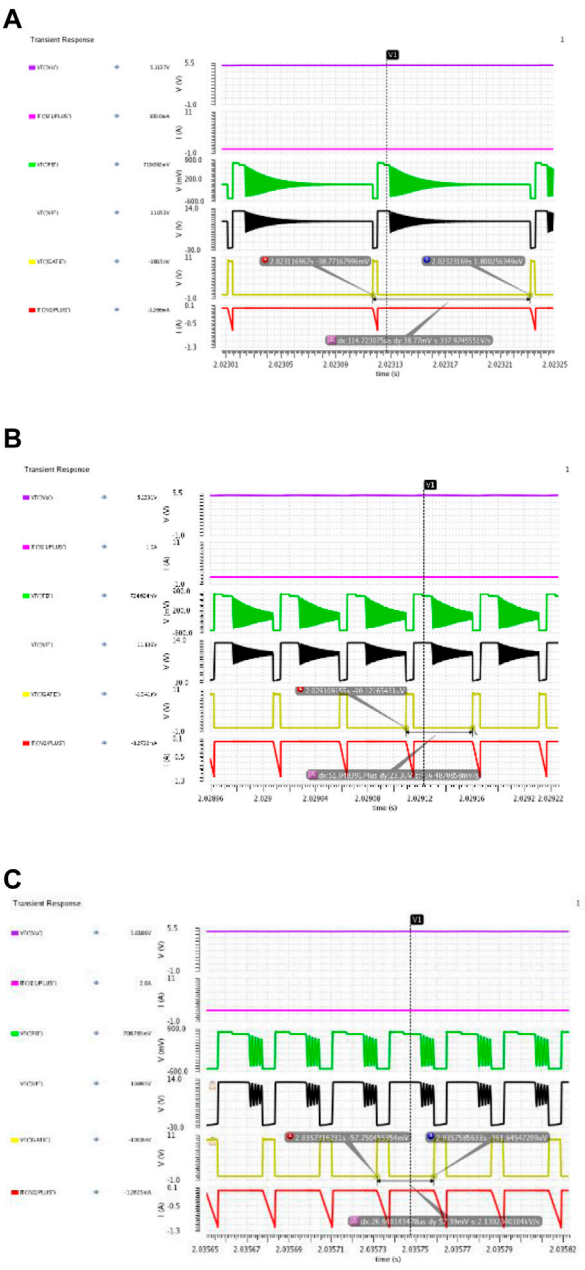


FIGURE 17
System simulation of the constant voltage mode under different load conditions: **(A)** 100 mA load, **(B)** 1 A load, and **(C)** 2 A load.

time when the power switching transistor is turned on, while the constant current control circuit realizes PFM modulation and determines the time point when the power switching transistor is turned on, thus producing the system output constant current.

## 3.5 Driving module

The current mirror buffer structure is designed for the driving circuit, and the power supply voltage of $M_{149}$–$M_{153}$ is used as the power domain of the driving circuit, as shown in Figure 8. $M_{140}$ is set as a 10-mA reference current source branch, and the width length ratio of the driving branch $M_{153}$ is 13 times that of $M_{140}$. The model is selected as a 70-V high-voltage resistant device model to prevent the breakdown caused by the high instantaneous voltage of the VDD when it is powered on, and the 130-μA drive current is provided, which is converted into the gate voltage required by the switching power transistor through $R_{36}$. In general, if the TON signal is loaded to the input end of the push–pull amplifier alone, when the rising edge or falling edge of the signal is in the intermediate stage of conversion, the intermediate level of about 3 V will lead to the simultaneous conduction of NMOS and PMOS in the push–pull amplifier, which will directly short-circuit the power supply to the ground breakdown device.

## 3.6 Constant voltage and constant current mode switch modules

The constant current and constant voltage modes are switched by the constant current control comparator and constant voltage control comparator working independently in two different loops, as shown in Figure 9. COMP2 is a constant voltage comparator, COMP1 is a constant current comparator, and the positive input of the two comparators is the limited voltage $V_{pk}$ of peak current. The feedback voltage maintains $V_O$ information detected by the auxiliary winding Laux at a fixed potential through the sampling-holding module and linearly amplifies the output $V_E$ signal through the error amplifier. $V_E$ actually represents the size of $V_O$. When the power supply uses the maximum constant current direction to charge the load, when the system is in the constant current mode, the negative input voltage $V_{pk}$ of COMP1 will reach a peak due to the role of the peak current limiting circuit. In the constant current mode, the output of COMP2 is also in the low level, and COMP1 plays a major role. As the load resistance gradually increases, the voltage signal maintained in the constant current mode will gradually exceed the reference voltage $V_{ref}$, and the output of error amplifier will flip and pull down the negative input of COMP2, which starts to output the high level. At this time, COMP2 plays a major role in the system entering the constant voltage mode. After integrated waveform by $R_S$ flip-flop set 0, NOR gate, and OSC frequency modulation oscillator, the switch pulse frequency is adjusted according to $V_O$ feedback information.

# 4 Simulation results

## 4.1 Module simulation

Figure 10 shows the simulation waveform of the temperature drift coefficient of the bandgap reference voltage. The temperature scanning range is −40 °C–100 °C. The circuit outputs 1.2 V bandgap reference voltage, the temperature drift coefficient is 8 ppm, and the accuracy error is less than ±0.1%.

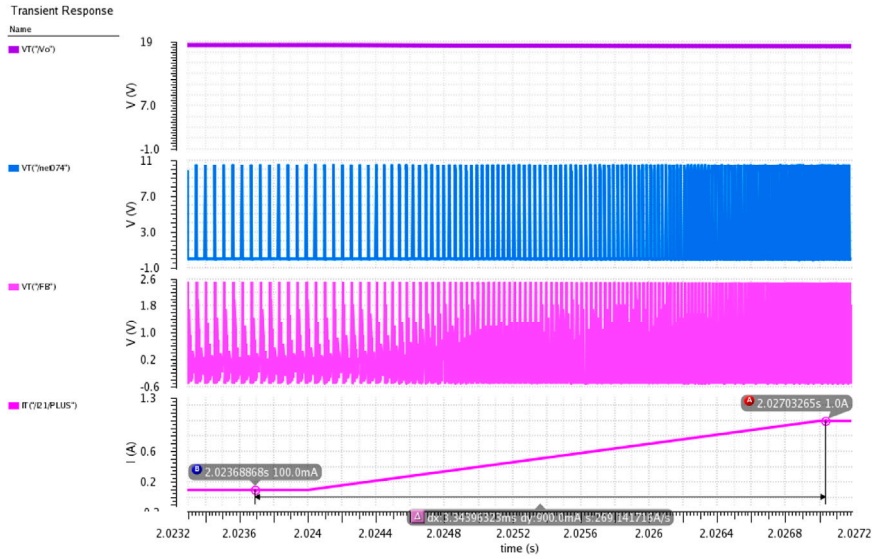


FIGURE 18
System simulation of the constant voltage mode under changing load conditions.

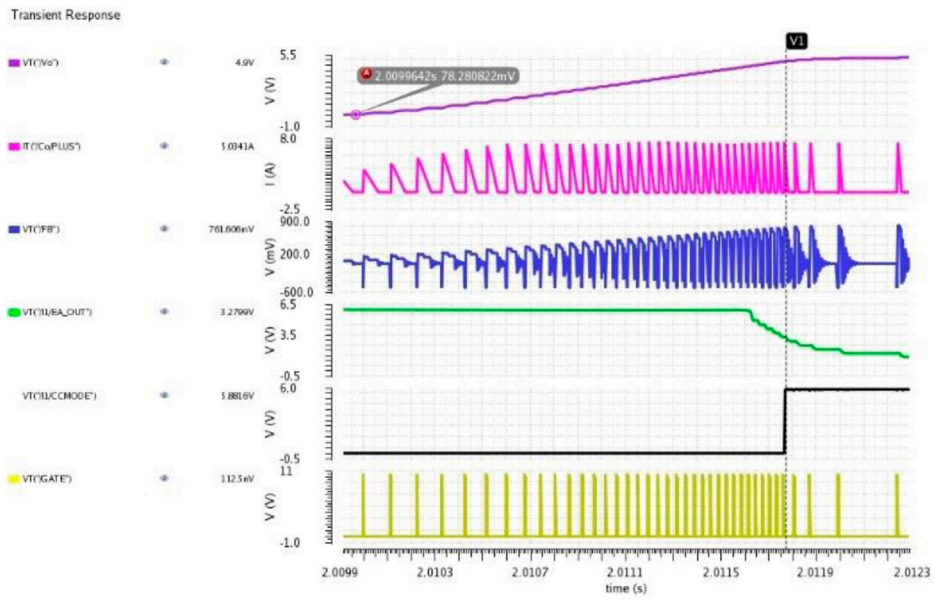


FIGURE 19
Simulation of conversion of the constant voltage mode and constant current mode.

Figure 11 shows the simulation of UVLO circuit over-voltage protection and under-voltage protection. VDD increases from 0 V to 90 V within 1 mS and decreases to 0 V scanning at 2 mS. When the VDD is 70 V, the circuit activates protection measures, and the circuit is powered on again when the step-down returns to 65 V.

Figure 12 shows the simulation of the LDO transient response. When the power supply VCC rises to 6 V within 10 nS, the output response time is 57 nS and reaches stability within 120 nS, indicating a fast response speed.

Figure 13 shows the joint simulation of the oscillator and the frequency division circuit, as shown in the following figure. The output nodes of D flip-flop d1–d7 are extracted by simulation, and the accuracy and stability of the frequency division circuit are good.

**TABLE 1 Primary-side feedback AC/DC control chip performance comparison.**

| Parameter | OB2530P | FM2539D | Tang et al. (2021b) | Li et al. (2023) | This work |
|---|---|---|---|---|---|
| Process (nm) | 180 | 130 | 180 | 180 | 180 |
| Operating voltage range(V) | 8–25 | 11–27 | 20–32 | 90–265 | 18–70 |
| Maximum output current(A) | 1 | 1 | 0.8 | 5 | 2 |
| Maximum rated power(W) | 12 | 10 | NA | NA | 10 |
| Switching frequency range (Hz) | 400–72 K | N/A | 20 K–100 K | 550–69 K | 10–100 K |
| Voltage ripple (mVPP) | <60 | <100 | NA | NA | <80 |
| Output accuracy error (%) | <1.5 | <1 | <±0.98 | <±2.33 | <1 |
| Power consumption(W) | <75 | <75 | 25 | 30 | <70 |
| Peak efficiency (%) | 77 | 86 | 88.52 | 89.65 | 87 |
| Valley efficiency (%) | NA | NA | 65 | 85.63 | 73 |
| Year | 2017 | 2019 | 2021 | 2023 | 2023 |

Figure 14 shows the simulation waveform of the PWM comparator under the condition of 1 A output current, $C_C$ signal and integration waveform are normal, and sawtooth wave and EA output produce the modulation frequency signal.

Figure 15 shows the simulation of the module working in constant current mode when the system is powered on. When the peak current limit output is high, the power switch transistor shuts off. When the comparator of the constant current control circuit outputs a low level, the power switch transistor is switched on, and within each cycle, the cut-off time is fixed in proportion to the period.

Figure 16 shows the simulation of the driving circuit. $T_{ON}$ is a high-level signal of 6 V, GATE_driven output is maintained at about 10 V, and the driving capacity is sufficient to meet the design requirements. After the arrival of $T_{ON}$, the non-overlapping clock drives the rising edge and falling edge of $M_{158}$ and $M_{159}$ signals, respectively. The two-stage push–pull amplifier works stably and does not open at the same time.

## 4.2 System simulation

When the load is 100 mA, 1 A, and 2 A, Figure 17 shows that the system maintains constant voltage 5 V output. In order to adapt to different loads, the system achieves constant voltage output by changing the switching frequency. According to the calculation, the working efficiencies of the chip under different loads are 73%, 79%, and 87%, and the efficiency value meets the requirements.

Figure 18 shows the transient simulation of load current rising from 100 mA to 1 A. With the increase of load current, the switching frequency of the system increases accordingly, thus ensuring that the output voltage of the system remains unchanged.

Figure 19 shows the conversion of the constant voltage mode and constant current mode during startup. When the power VDD comes, the circuit module starts to work and $V_O$ keeps rising and continues to charge the capacitor $C_C$. At this time, the chip works in the constant current mode, and the average current is 2 A. When the capacitor $C_C$ is full, the output voltage rises to 5 V and remains constant, entering the constant voltage mode. The mark line $V_1$ is the dividing point between constant current and constant voltage switching. At this time, the EA output becomes low, the comparator flips, and the mode control signal changes from low level to high level. When the output voltage reaches the set threshold, that is, when the EA output voltage is lower than 3.2 V, mode switching occurs.

The research results of this paper will be compared with other studies, and OB2530P and FM2539D, two popular primary AC/DC products in the market, are selected for comparison. The comparison results are shown in Table 1.

As can be seen from Table 1, the primary-side feedback power management chip designed in this paper has a maximum efficiency of 87% and a wider adaptive frequency modulation range. The peripheral circuit design of auxiliary winding feedback power supply makes the static power consumption of the product less than 75 mW, and the output ripple of the circuit is small and high precision, which has certain advantages compared with other products.

# 5 Conclusion

This paper designs a flyback primary-side feedback AC/DC switching power supply chip, which is mainly suitable for the lithium battery-charging adapter. Based on the SMIC 0.18-μm CMOS process, the system simulation results are as follows: the system operating voltage range is from 18 V to 70 V, the switching frequency range is from 10 Hz to 100 KHz, the peak efficiency is 87% with 2 A load, and the static power consumption of the system is less than 75 mW. The output ripple of the circuit proposed in this paper is smaller and has higher precision, which has certain advantages compared with other products.

## Data availability statement

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

## Author contributions

Conceptualization, ZZ and MR; methodology, MR; software, TG; validation, TG; writing—original draft preparation, ZZ; supervision, MR; project administration, MR; funding acquisition, MR. All authors contributed to the article and approved the submitted version.

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## Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

## Publisher's note



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