

A High Power Quality Buck-H Auxiliary Power Converter in Railway Applications

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DC voltage utilization and AC voltage harmonics are important evaluation indexes for Auxiliary Power Converter in Railway Applications. To improve the above two indicators, a novel switchmode modulation method and quasi-PR control strategy for Buck-H three-phase inverter is proposed in this paper. The Buck-H three-phase inverter integrates the AC side filter circuit into the DC Buck circuit, which reduces the volume of the filter capacitor and improves the filtering effect. This novel switch-mode modulation method uses only one high frequency switch per phase, which reduces the switching losses and thereby increases overall efficiency. In addition, this switch-mode modulation absence of shoot-through menace eliminates the dead time requirement. Meanwhile, the quasi-proportional-resonance (PR) controller and its control parameters are optimized to improve the AC voltage tracking performance. The influence of PR control parameters on system performance is analyzed in detail. The proposed switchmode modulation method and control method can effectively reduce the harmonic distortion rate of the system. The effectiveness is verified through the StarSim hardware-in-the-loop experimental results.

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INTRODUCTION

Auxiliary power converter is widely used in electrical fields such as power supplies, renewable energies, motor drives, and uninterruptible power supplies (Xu et al., 2016; Costa et al., 2018). Among various converter topologies, the three-phase inverter based on the three-phase bridge structure has been extensively studied for its simple structure, flexible control, and interconnection with the grid. DC voltage utilization and AC voltage harmonics are important evaluation indexes for three-phase bridge inverters. The DC voltage utilization is closely related to the efficiency of the inverter. Advances in the utilization of DC voltage can improve the load capacity of the inverter and reduce the voltage stress of the power device (Rahman et al., 2019). Additionally, for some high-end equipment such as auxiliary power supply of EMU, uninterruptible power supplies, aerospace power systems, and variable-speed AC machine drives, AC voltage with a lower harmonic distortion rate is necessary (Raymundo et al., 2017). However, the conventional three-phase bridge inverter and its modulation strategy are limited to improving the DC voltage utilization and reducing the harmonic distortion rate (Xiao et al., 2014; F. Jiang et al., 2021), which are essential performance evaluation indexes of inverters. Therefore, the conventional three-phase bridge inverters are not suitable for these particular applications, and a new topology structure or control strategy is urgently needed.

In (Shukla et al., 2018; Kalair et al., 2017), the sinusoidal pulse width modulation (SPWM) is used, and the maximum DC voltage utilization of the three-phase inverter is only 0.866. In (Pan et al.,



2020), the space vector pulse width modulation method (SVPWM) is proposed to experiment the control of inverter. In (Li et al., 2019), the superiority of SVPWM in controlling inverters is then verified theoretically and experimentally. Compared with SPWM, utilization of DC voltage of SVPWM can be increased by 15.47% (Nallamekala et al., 2016; Choi et al., 2015). The bridge inverter based on PWM modulation has a theoretical maximum DC voltage utilization of 1, but the higher utilization is limited.

As for the harmonic distortion rate of AC voltage on the inverter's output side, a multi-level converter topology is proposed in (Wang et al., 2015; Feng et al., 2019). The AC voltage levels in the multi-level inverter is more than or equal to three. The more the AC voltage levels, the closer the voltage wave to a sine wave and the fewer harmonics. However, as the voltage levels increase, the system structure and controller become more complicated, resulting in poor reliability and stability (Li et al., 2016). In addition (Karwatzki et al., 2018), propose the use of LCL filter to reduce the harmonics of inverter. Although LCL filter can eliminate some harmonics, it tends to cause resonance problems, which reduces the stability of the inverter (Gautam et al., 2017). Therefore, a simple three-phase inverter and its corresponding control method are highly desirable for a three-phase grid-connected system with high efficiency and reliability.

The purpose of this paper is to propose a novel switch-mode modulation method and quasi-PR control strategy for Buck-H three-phase inverter. The novel switch-mode modulation method integrates the AC side filter circuit into the Buck circuit, so that the AC output side does not need passive filter components such as inductors and capacitors. Compared with the traditional inverter filter capacitor, the DC filter capacitor in this topology is smaller and has a better filtering effect.

1) Compared with the conventional inverter filter capacitor, the DC filter capacitor in the novel Buck-H three-phase inverter topology is smaller and has a better filtering effect.



- 2) The H-bridge in the inverter topology is designed to be controlled synchronously with the power frequency of 50 Hz to solve the shoot through problem and reduce reverse recovery lose. This design method effectively reduces the harmonic distortion rate of the AC voltage.
- 3) A quasi-PR control method and its control parameters are designed to improve the inverter's DC voltage utilization.

The rest of this paper is organized as follows. In *Topology and Working Principle*, the novel switch-mode modulation method for the Buck-H three-phase inverter is presented. The working principle and switching method for the Buck-H inverter are introduced in detail. In *Control Strategy and Parameter Design*, a quasi-PR control method for the Buck-H three-phase inverter is proposed. Simulation results are shown in *Simulation Analysis* and Experimental results are provided in *Experimental Verification*. Finally, *Conclusion* concludes this paper.

TOPOLOGY AND WORKING PRINCIPLE

Topological Structure

This paper takes the three-phase auxiliary inverter in the traction drive system of CRH5 EMU as the research object, as shown in **Figure 1**. Among them, the three-phase inverter converts the front DC into 380 V AC for the normal operation of auxiliary equipment in the carriage (such as air conditioning, lighting, etc.). However, the traditional three-phase inverter topology is usually composed of H-bridge circuit, which is difficult to provide high-quality power quality. This paper proposes a novel switch-mode



modulation method for Buck-H three-phase inverter is shown in **Figure 2**; V_s represents the input DC power supply. L and C are the filter inductor and capacitor respectively, and $Q_{11}-Q_{31}$ are the switches.

The front end of each phase of the inverter is a Buck converter, as shown in **Figure 3** its steady-state output voltage is:

$$v_c = \alpha V_s \tag{1}$$

Where α is the on-duty ratio of the Buck converter power switch, and V_s is the input DC voltage.

Assuming the DC voltage is constant, the duty cycle α will change regularly with the inverting fully rectified sinusoidal (as shown in **Figure 4A**) by controlling the switching frequency change:

$$\alpha = |\sin\left(\omega t\right)| \tag{2}$$

Therefore, the output voltage at the output end of the power switch S_{T1} is an equivalent sine half-wave PWM as shown in **Figure 4B**.

Then through the LC filter in the Buck circuit, only the sinusoidal positive half-cycle DC pulsation waveform is output

as shown in **Figure 4C**. The following H bridge is synchronized with the power frequency of 50 Hz, so there is no reverse recovery lose and the shoot through problem. The inverting fully rectified sinusoidal is transformed into a standard sine wave through the alternate conduction of Q_{11}/Q_{14} and Q_{12}/Q_{13} as shown in **Figure 4D**.

However, in a conventional H bridge inverter, the dead time is necessary to prevent the short circuit and damage caused by the simultaneous conduction of the switches. It is set between the driving signals of two switches in the same branch. Nevertheless, the introduction of the dead time will increase the harmonic voltage.

Although there are many switches for the Buck-H threephase inverter using the switching mode proposed in this paper, only ST1, ST2, and ST3 power switches work at high frequency. The other switches in the H-bridge circuit are zero voltage switching and zero current switching, namely soft switching. And little or no loss is produced in this switch state. The switching loss of the inverter mainly comes from high-frequency switches. The high-frequency switches in the Buck-H three-phase inverter are half less than the conventional three-phase H bridge inverter, which dramatically reduces the switching loss. Furthermore, the utilization of DC voltage is improved to a certain extent.

Working Principle

Principle Analysis

If the PWM waveforms of S_{T1} , S_{T2} and S_{T3} change with the inverting fully rectified sine wave and have a phase difference of 120°, it can be seen from **Eq. 2** that the duty ratios of the power switch S_{T1} , S_{T2} and S_{T3} in **Figure 1** also follow the inverting fully rectified sine wave with a phase difference of 120°. So the duty ratios of S_{T1} , S_{T2} , and S_{T3} in the three-phase inverter are:



$$\begin{cases} \alpha_1 = m |\sin \omega t| \\ \alpha_2 = m |\sin (\omega t - 120^\circ)| \\ \alpha_3 = m |\sin (\omega t + 120^\circ)| \end{cases}$$
(3)

Where *m* is the modulation factor, its expression is: $m = V_o/V_s$, V_o is the inverter's output voltage and V_s is the input DC voltage. When the steady-state is reached, the output side voltage of the Buck converter in the three-phase inverter is:

$$\begin{cases} V_{c1} = \alpha_1 V_S \\ V_{c2} = \alpha_2 V_S \\ V_{c3} = \alpha_3 V_S \end{cases}$$
(4)

Combining Formula (3), Eq. 5 can be obtained:

$$\begin{cases} V_{c1} = mV_s |\sin \omega t| \\ V_{c2} = mV_s |\sin (\omega t - 120^\circ)| \\ V_{c3} = mV_s |\sin (\omega t + 120^\circ)| \end{cases}$$
(5)

It can be seen from the above formulas that the voltages V_{c1} , V_{c2} , and V_{c3} applied to the capacitor at the three-phase Buck circuit only contain a positive half-cycle waveform of the sine wave, which is a constant flow. Therefore, the capacitors C₁, C₂, and C₃ can be designed based on DC type (such as an electrolytic capacitor). Compared with the voltage on the filter capacitor in the conventional H bridge inverter, which is AC component, the DC filter capacitor with the same capacity has the advantages of small volume, low price, and good filtering effect. So the output voltage harmonic content of the filter is less (Lei et al., 2016). Then the four switches Q₁₁/Q₁₄ and Q₁₂/Q₁₃ of H bridge switch on at a frequency of 50 Hz. For example, when t = 0, Q₁₁/Q₁₄ is turned on and Q₁₂/Q₁₃ is turned off; when t = T/2, Q₁₁/Q₁₄ is turned off, and Q₁₂/Q₁₃ is turned on. The rest of B and C are similar. The output voltage V_o after transformation is:

$$\begin{cases} V_{o1} = mV_S \sin \omega t \\ V_{o2} = mV_S \sin (\omega t - 120^{\circ}) \\ V_{o2} = mV_S \sin (\omega t + 120^{\circ}) \end{cases}$$
(6)

Equation 6 shows that the obtained voltage is a quality sine wave with very low harmonic contents. When connected to a balanced three phase resistive load; this topology acts as a three-phase voltage source inverter supplying a perfect three phase balanced sinusoidal voltage waveform. Neutral connection is optional and thus it can also work as a three-wire system.

The four switches of each phase in the H-bridge operate at a certain frequency (50 Hz) and work in a soft-switching state. Therefore, there is almost no loss in this switching state, thus improving the efficiency of the whole system to a certain extent. The voltage in **Eq. 6** is the phase voltage with a phase difference of 120°, and the maximum phase voltage peak value is V_s . As the three phases are symmetric, the line voltage can be deduced from **Eq. 6** as follows:

$$\begin{cases} V_{o1} = m\sqrt{3}V_{S}\sin(\omega t + 30^{\circ}) \\ V_{o2} = m\sqrt{3}V_{S}\sin(\omega t - 90^{\circ}) \\ V_{o2} = m\sqrt{3}V_{S}\sin(\omega t + 150^{\circ}) \end{cases}$$
(7)

Therefore, when the modulation ratio is 1, the maximum line voltage peak value can be obtained as $\sqrt{3}V_s$. If the DC voltage is

310*V*, the effective value of the output line voltage is 380*V*. According to the definition of DC voltage utilization:

$$\gamma = \frac{V_L}{U_{dc}} \tag{8}$$

Where V_L is the peak value of the output line voltage, U_{dc} is the DC power supply voltage.

So the maximum DC voltage utilization of the Buck-H inverter is $\sqrt{3}\approx 1.73$. However, when SPWM is used in the traditional H bridge three-phase inverter, the maximum DC voltage utilization is only 0.866. Even with SVPWM modulation or third harmonic injection, the maximum DC voltage utilization can be achieved only 1 (Arshadi et al., 2016). Therefore, the Buck-H three-phase inverter using the switching mode proposed in this paper has a significant advantage over the traditional H bridge three-phase inverter in DC voltage utilization.

Switch Mode Analysis

There are four switching modes for each phase of five power switches. Taking A-phase as an example, the current loop and equivalent circuit in each switching mode are shown in **Figure 5** respectively.

In mode 1 (as shown in **Figure 5A**): S_{T1} is on, Q_{11} and Q_{14} are on, Q_{12} and Q_{13} are off. At this point, current flows through V_S , S_{T1} , L_I , R_a , Q_{11} and Q_{14} to form a circuit, while the DC power supply charges capacitor C_I to supply power to the load.

In mode 2 (as shown in **Figure 5B**): S_{T1} is off, Q_{11} and Q_{14} are on, and Q_{12} and Q_{13} are off. At this point, current flows through VD₁, L_1 , R_a , Q_{11} and Q_{14} to form a circuit. Meanwhile capacitor C_1 is discharged, and VD₁ plays the role of free-wheeling.

In mode 3 (as shown in **Figure 5C**): S_{T1} is on, Q_{11} and Q_{14} are off, and Q_{12} and Q_{13} are on. The current forms a loop through V_s , S_{T1} , R_a , Q_{14} , and Q_{13} . At the same time, the DC power supply charges capacitor and supply power to the load.

In mode 4 (as shown in **Figure 5D**): S_{T1} is off, Q_{11} and Q_{14} are off, and Q_{12} and Q_{13} are on. At this time, the current forms a loop through VD₁, L_I , Q_{14} , R_a and Q_{13} , the capacitor C_I discharged, and VD₁ continues to flow.

The H-bridge following the Buck converter consists of four switches $(Q_{11}-Q_{14})$. H-bridge is used to realize the function of synchronous inverting with reference voltage, as shown in **Figure 6**.

At $0 \sim T/2$ and $T \sim 3/2T$, the switch Q_{11} and Q_{14} are on while the switch Q_{12} and Q_{13} are off; at $T/2\sim T$ and $3/2\sim 2T$, the switch Q_{12} and Q_{13} are on, while the switch Q_{11} and Q_{14} are off. Therefore, the capacitor voltage V_c at the output side is turned into the standard sinusoidal output voltage V_{oa} .

CONTROL STRATEGY AND PARAMETER DESIGN

Quasi PR Control

The traditional PI controller is composed of proportional and integral links. Its transfer function is:





$$G_{\rm pI}(s) = k_{\rm p} + \frac{k_{\rm i}}{s} \tag{9}$$

Its gain at the fundamental frequency ω_0 is

$$\left|G_{\rm pI}(j\omega_0)\right| = \sqrt{k_{\rm p}^2 + \left(\frac{k_{\rm i}}{\omega_0}\right)^2} \tag{10}$$

It can be seen from **Eqs 9**, **10** that the PI controller is a linear controller. The gain at the fundamental frequency is a limited value. So it can only track the DC value accurately. If PI control is to be used in three-phase AC system, complex coordinate transformation of abc/dq or $\alpha\beta/dq$ must be carried out to change AC into DC to realize static error free tracking control.

To overcome the defects of the PI controller, the PR controller is proposed in (Parvez et al., 2020; Alemi et al., 2016). The transfer function is:

$$G_{\rm PR}(s) = k_{\rm p} + \frac{2k_{\rm r}s}{s^2 + \omega_0^2}$$
(11)

$$|G_{\rm PR}(j\omega_0)| = \sqrt{k_{\rm p}^2 + \left(\frac{2k_r\omega_0}{-\omega_0^2 + \omega_0^2}\right)^2}$$
(12)

The root locus analysis shows that the PR controller is compared with the PI controller. The transfer function adds two closed-loop poles of fixed frequency on the imaginary axis of the s-plane to form resonance. So it can realize static error-free tracking control of AC at this frequency (Pan., 2018). Compared with the PI controller, the gain of the PR controller at a certain frequency is infinite. As a result, it can realize static error-free tracking control of AC at a specific frequency. In the control design of the current inner loop, there is no need for complex dq coordinate transformation and coupling relation between dq axes. Hence the control system design is simplified. However, in the actual power grid, the bandwidth of the ideal PR controller is narrow due to the frequency fluctuation of the power grid. Therefore, it cannot adapt to the actual power grid fluctuation. A quasi-PR controller is proposed to solve this problem. Its transfer function is:

$$G(s) = k_{\rm P} + \frac{2k_{\rm r}\omega_{\rm c}s}{s^2 + 2\omega_{\rm c}s + \omega_0^2}$$
(13)

Compared with the PR controller, a zero point in the transfer function of the PR controller is added to the quasi-PR controller, which increases the bandwidth of the controller and adapts to the power grid with actual frequency fluctuation. Hence the problem of poor control performance caused by frequency fluctuation is solved effectively.

Analysis of Control Parameters

It can be seen from **Eq. 13** that the transfer function of quasi-PR controller contains three variables k_p , ω_c and k_r . To investigate the effect of each parameter on the inverter output performance, the effect of three variables on the system performance is analyzed using the control variable method.





1) Set $k_p = 1$, $\omega_c = 1$, k_r as variable, draw the Bode diagram of the corresponding transfer function (as shown in **Figure** 7) to study the influence of k_r on the performance of controller.

It can be seen from the above figure that as the k_r parameter increases, the gain of the controller also increases, while the bandwidth of the control does not change. Therefore, the k_r parameter only affects the gain of the controller, not the bandwidth. The gain of the controller is proportional to k_r . The larger k_r is, the larger the gain is and the smaller the steady-state error is. However, if k_r is too large, the harmonic component will be amplified, thus reducing the quality of the grid-connected current. Therefore, when selecting k_r , it is necessary to ensure that the system has sufficient gain near the fundamental frequency, and there should be a certain attenuation effect away from the fundamental frequency.

2) Set $k_p = 1$, $k_r = 1$, ω_c as variable, draw the Bode diagram of the corresponding transfer function (as shown in **Figure 8**) to study the influence of ω_c on controller performance.

It can be seen from **Figure 7** that the gain and bandwidth of the controller increase with ω_c increases. But the gain at the fundamental frequency does not change. Therefore, ω_c not only affects the gain of controller, but also affects the bandwidth. In the







selection of ω_c parameters, large bandwidth cannot be blindly pursued. Because the larger ω_c is, the larger bandwidth will be. Hence the harmonics far away from the fundamental frequency will also be amplified.

Set ω_c = 1, k_r = 1, k_p as variable, draw the Bode diagram of the corresponding transfer function (as shown in Figure 9) to study the influence of k_p on the performance of controller.

It can be seen from **Figure 8** that the k_p parameter affects the gain at all frequencies, which affect the overall performance of the whole control system. Therefore, in the design of PR controller parameters, factors such as steady-state performance and the

interaction among parameters should be considered comprehensively to determine the final parameters.

Therefore, in engineering application, the design steps of quasi-PR controller parameters are as follows: Determine the controller bandwidth according to the allowable fluctuation range of frequency, and then select ω_c ; k_r is selected according to the current quality and the gain requirement near the fundamental wave frequency of the control function; According to the harmonic impedance design k_p , the steady-state performance and anti-interference performance of the system meet the requirements of the interaction between the parameters k_p and k_r should be considered comprehensively when setting.

Overall Control Strategy

This section simplifies the overall control strategy using phase A as an example. The control strategy of each phase is shown in **Figure 10**. The other phases B and C are similar except that the phase difference of the reference signal is given at 120°.

To enable the three-phase inverter output voltage amplitude constant and frequency when the inverter AC load fluctuates, a closed-loop control strategy is used (as shown in **Figure 10B**). Firstly, the phase angle θ is obtained by integrating the given frequency reference value f_{ref} . Then the final reference voltage U_{ref} is obtained by multiplying the given voltage amplitude U by $sin\theta$. The equation is expressed as:

$$U_{ref} = U\sin\left(\omega t\right) \tag{14}$$

Then the output AC voltage U_{oa} is directly fed back to controller to form a closed-loop control. The reference voltage U_{ref} is compared with the output voltage U_{oa} , and the error signal is sent to the quasi-PR controller. So that the PR controller can track the error signal without static error. From **Eq. 2**, it can be seen that to make the output voltage of the Buck converter vary regularly as the inverting fully rectified sine wave, the output signal U_k of the PR controller needs to be processed by absolute value operation and normalization. Then it can be fed to the PWM generator for pulse width modulation with a triangular wave. Then the phase A modulation signal is:

$$u_A = \frac{|U_k|}{V_s} \tag{15}$$

Through PWM modulation, the control signal of high frequency switch S_{T1} of Buck converter is obtained. H-bridge circuit is used to realize the synchronous reversal of DC pulse voltage wave at the output of Buck converter in 50 Hz. Therefore, the control signal generation method of the four switches of each phase H-bridge is shown in **Figure 10B**. The reference voltage U_{ref} of 50 Hz is compared with 0 respectively. When the reference voltage is greater than 0, the switches Q_{11} and Q_{14} are on, while the switches Q_{12} and Q_{13} are off. So the output voltage is positive half-cycle waveform of sinusoidal voltage. When the reference the output voltage is a negative half-cycle waveform of a sine wave voltage.

SIMULATION ANALYSIS

The simulation model of the Buck-H three-phase inverter was built in MATLAB/Simulink. The simulation parameters are as follows (take phase A as an example): DC power supply voltage is 311 V. The effective values of inverter output phase voltage and line voltage are 220 and 380 V with 50 Hz respectively. The load resistance is 20Ω , and the inductance of Buck circuit is 6 mH. The capacitance is 10uF, and the switching frequency is 10 kHz. The parameters of the quasi-PR controller are $\omega_c = 3$, $k_p = 1.5$, $k_r = 100$.

Constant Voltage and Constant Frequency Operation

Normal Operating Conditions

Figure 11 shows the A-phase voltage and current waveforms of the Buck-H three-phase inverter under PI control and Quasi PR control respectively. It can be seen from **Figure 11A** that the output voltage of the inverter is a standard 50 Hz AC. The output voltage peak value is stabilized at 311 V after 0.01 s, thus realizing constant voltage and frequency control. However, the system output voltage and current waveform fluctuates at the over-zero point under PI control, and smooth switching cannot be achieved. Secondly, the amplitude of the output voltage is only 305 V and the current size is only 12 A.

Load Mutation

In the simulation, the load is suddenly doubled at 0.2 s to verify that the inverter can still achieve constant voltage and frequency output. The dynamic process of its output phase voltage and current is shown in **Figure 12**.

Figure 12 shows the dynamic waveforms of output voltage and current by the Buck-H three-phase inverter when the load is changed suddenly under PI control and Quasi PR control respectively. As shown in **Figure 12A**, the peak value of the output phase current increases from 15.5 to 31 A when the load suddenly doubles in 0.2 s, namely, the output power is also doubled. When the load suddenly doubled, the output threephase phase voltage of the inverter fluctuated at 0.2 s, from a peak value of 311–330 V. However, the 50 Hz AC steady-state output of peak value of 311 V is restored shortly after 0.22 s. In this way, a steady-state output of constant voltage and frequency can be realized in the case of load mutation. However, under the same operating conditions, the output voltage and current waveforms under PI control cannot be smoothly transitioned at the over-zero point, and the overall effect is worse than that of quasi-PR control.

Comparison of DC Voltage Utilization

Figure 13 shows the output three-phase voltage waveform of three-phase inverters in different modes. It can be seen from **Figure 13** that the peak value of line voltage in Buck-H three-phase inverter is about 538 V. However, when the DC power supply is 311 V, and traditional three-phase inverter is modulated with SPWM. The maximum peak value of output line voltage is:







(A) Output line voltage of three phase bridge inverter modulated by SPWM, (B) Output line voltage of three phase bridge inverter modulated by SPWM, (C) Output line voltage of Buck-H three phase inverter, (D) Comparison of output line voltage of three phase inverter with different switching modes.

$$\frac{\sqrt{3}}{2}V_S \approx 0.866V_S = 269.33\,(\text{V}) \tag{16}$$

Even if the SVPWM modulation or third harmonic injection method is adopted, the maximum peak value of output line voltage in a three-phase inverter is only 311 V. Therefore,



compared with the conventional three-phase inverter with SPWM, the DC voltage utilization of this Buck-H three-phase inverter is improved by two times. Similarly, the DC voltage utilization is 1.73 times higher than the SVPWM.

Comparison of Harmonic Distortion Rate

With the same filter inductance and capacitance, the harmonic content of output current in the conventional three-phase H-bridge inverter and Buck-H three-phase inverter is compared, as shown in **Figure 14**.

It can be seen from **Figure 14A** that the total harmonic distortion (THD) of the output current in a conventional three-phase H-bridge inverter is 2.31%. However, the THD of the Buck-H three-phase inverter proposed in this paper is only 0.52%, and the maximum single harmonic content is less than 0.3%. The results show that the Buck-H three-phase inverter can significantly reduce the harmonic content compared to the conventional H-bridge three-phase inverter. The simulation results are consistent with the conclusions drawn from the above operating principle analysis.

EXPERIMENTAL VERIFICATION

To further verify the correctness of the topology and control strategy proposed in this paper, the hardware in the loop simulation platform of the Buck-H three-phase inverter system is built shown in **Figure 2**. The primary circuit model is built in Simulink software, and the host computer StarSim HIL software of Modeling Tech is used to make the primary circuit run on the FPGA board in the StarSim MT6016 chassis. The controller adopts TMS320F28335 of the C2000 series of TI company. The host computer and the controller realize signal interaction through the interface box to form a closed-loop system.

TABLE 1 | Experimental platform parameters.

Parameters	Value
DC voltage	311 V
Filter inductance	6 mH
Filter capacitor	10uF
Load resistance	20Ω
Switching frequency	10 kHz
Quasi PR parameter	$k_p = 1.5, k_r = 100, \omega_c = 3$



Among them, the control circuit is completed by DSP, and the hardware circuit is completed on the hardware in the loop (HIL) real-time simulation platform. The limit interval value of the analog output/input of the main circuit in StarSim HIL real-time simulator is (-10,10) V, and the limit interval of the digital output/ input of the DSP controller is (0,3.3) V. The main circuit topology is consistent with **Figure 1**, and the main parameters of the experimental platform are shown in **Table 1**. Since the voltage ranges of I/O ports of HIL is [-10,10] V, it is necessary to multiply the electrical quantity to be measured by the corresponding proportional coefficient before output and detect it by oscilloscope. The experimental platform is shown in **Figure 15**.

Experimental Verification of Symmetrical Load and Asymmetric Load

Three symmetric load and asymmetric load with a resistance value of 20Ω are connected for comparative experimental to verify the overall performance of the proposed Buck-H threephase inverter. According to the experimental waveform as shown in **Figures 16**, **17**, it can be seen that the output voltage of the Buck-H inverter is the standard 50Hz AC, and the peak output voltage is stable at 311 V. Then double the A-phase load, as can be seen from **Figure 16**, when the A-phase load suddenly doubles, the peak value of the output A-phase current increases from 15.5 to 31 A, so the output power also doubles. When the A-phase load is doubled suddenly, the output three-phase voltage of the inverter fluctuates at the



FIGURE 16 | Voltage and current waveform of phase A under symmetrical load.



FIGURE 17 | Voltage and current waveform of phase A under asymmetric load.



moment of sudden change, but the 50 Hz AC steady-state output with a peak value of 311 V is quickly restored.

Experimental Verification of Different Control Strategies

The comparison experiment between SPWM modulation and SVPWM modulation was conducted on the experimental platform to verify the correctness and effectiveness of the proposed control strategy. The experimental waveforms are shown in **Figures 18–20**.





According to the experimental waveforms, it can be seen that the output line voltage peak of the Buck-H three-phase inverter using the proposed control strategy is about 538 V. When the DC power supply is 311 V, and the SPWM modulation is adopted for the conventional three-phase inverter, the maximum output line voltage peak value is 269 V. Even if the SVPWM modulation method or three harmonic injection methods are introduced, the maximum output line voltage is only 311 V. Therefore, the Buck-H three-phase inverter using the switching mode proposed in this paper significantly improves the utilization of DC voltage compared with the conventional three-phase inverter.

CONCLUSION

In this paper, a novel switch-mode modulation method and quasi-PR control strategy for Buck-H three-phase inverter is proposed. The novel switch-mode modulation method for Buck-H three-phase inverter is introduced, along with the

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Alemi, P., Bae, C.-J., and Lee, D.-C. (2016). Resonance Suppression Based on PR Control for Single-phase Grid-Connected Inverters with Filters. *IEEE J. Emerg. Sel. Top. Power Electron.* 4 (2), 459–467. June 2016. doi:10.1109/jestpe.2015. 2464699 working principle and switching mode. The quasi-PR control is constructed for the Buck-H topology, which can improve the system's dynamic performance. The following conclusions can be drawn from the theoretical and experimental results.

- 1) Compared with the conventional SPWM and SPVWM in the H-bridge inverter, the DC voltage utilization in the novel Buck-H three-phase inverter is improved by 2 times and 1.73 times, which significantly enhances the load-carrying capacity of the inverter.
- 2) The novel switch-mode modulation method for Buck-H three-phase inverter has a lower harmonic distortion rate. By integrating the AC side filter circuit into the Buck circuit, reducing the introduction of harmonics to a certain extent.
- 3) The novel switch-mode modulation method can reduce the system volume and cost. The capacitor voltage in the Buck circuit is DC. Compared with the conventional inverter, the DC filter capacitor in this paper has a smaller volume and better filtering effect.

DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

AUTHOR CONTRIBUTIONS

Conceptualization, ZL and FW; methodology, ZL, FW, and JZ; software, ZL and FW; validation, ZL, FW, JZ, and DH; formal analysis, ZL, FW, JZ, and DH; investigation, ZL, FW, JZ, and DH; resources, ZL; data curation, FW; writing—original draft preparation, ZL, FW, and DH; writing—review and editing, ZL, FW, and JZ; visualization, XY and FX; supervision, JZ and FX; funding acquisition, ZL. All authors have read and agreed to the published version of the manuscript.

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