



High-Gain Seven-Level Switched-Capacitor Two-Stage Multi-Level Inverter

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Due to the low voltage of the PV module and to enable AC module technology, where every PV module has its own DC-AC converter, this paper introduces a new high step-up seven-level two-stage multilevel inverter for a grid-connected Photovoltaic (PV) system. The introduced schematic consists of two stages. The first stage is a switched capacitor boost converter and the second stage is a seven-level seven-switches multilevel inverter. The first stage is designed to extract the maximum power of PV module and step-up its input voltage. The proposed seven-level seven-switches topology generates seven levels with only seven switches. Thus, the number of switches is reduced. The proposed inverter has eight valid switching states. In each switching state only three switches are ON at the same time. The proposed topology has some distinct features such as reduced number of switches and reduced conduction; total harmonic distortion (THD) of the current is 23% in case of pure resistive and with no filtration at the output and less than 3% using a small filter with integration into the grid. Due to the high boosting ability of the switched capacitor boost converter, a wide voltage gain is easily achievable. In this paper the system is tested at different voltage gains and the highest simulated efficiency was around 96%. The developed system is simulated in MATLAB/SIMULINK and in real time using DSPSPACE1202. Both simulation and real-time results are consistent with the theoretical analysis.

Keywords: photovoltaic, maximum power point, seven-level multilevel, switched capacitor boost converter, MPPT, high_Gain

INTRODUCTION

Renewable energy is now essential in order to reduce pollution and to keep climate change under control. Photovoltaic (PV) power generation is one of the leading forms of renewable power generation, especially in residential power generation. PV module-generated voltage is small and requires a step-up converter to match with load requirement and extract the maximum power from the module. A DC-AC conversion stage is mandatory in case of AC grid integration. Different inversion topologies have been reported in the literature, however multilevel inverters are gaining more attention due to their inherent merits as their output voltage is in a staircase shape, which reduces filter requirements and enables the utilization of low rating switching devices (Jeevananthan et al., 2006; Mondal et al., 2009; Rahim et al., 2011).

Multilevel inverters are classified based on their structure into three main categories: Cascaded H-Bridge (CHB) topologies, Flying Capacitor (FC), and Neutral Point Clamped (NPC) (Rajeevan et al., 2011).

NPC inverters are widely used configurations in the industry and are well identified by academia, where DC-link voltage is split by means of a series of connected capacitors (Saeedifard et al., 2012; Tian et al., 2018). However, special consideration should be made to keep the balance of the split capacitors (Sebaaly et al., 2016; Akagi, 2017; Giri et al., 2017; Hu et al., 2017). FC is another style of multilevel topologies where floating capacitors are used to generate the required voltage levels. Similar to NPC, special care should be given to floating capacitors voltage balance as they are utilizing a large number of capacitors for higher voltage levels (Amini et al., 2016; Amini and Moallem, 2017; Lei et al., 2017). CHB multilevel configuration is implemented by a series of connections of H-bridges. Each H-bridge is connected to an isolated DC-voltage source. The number of bridges connected in a series are based on the required voltage level (Wu et al., 2017; Iqbal et al., 2020). Owing to the modularity of this structure and straightforwardness of its control, it is very convenient to use in high-power applications (Pulikanti et al., 2013; Wang et al., 2017; Siddique et al., 2021). One disadvantage of such a structure is the number of isolated DC-DC sources increases with any increasing number of voltage levels (Babaei and Hosseini, 2009; Malinowski et al., 2010; Gautam et al., 2017).

Switched Capacitor Multilevel Inverter (SCMLI) is a good candidate for PV applications, due to its boosting ability. In SCMLI, capacitors are charged from the PV module and discharge their energy into the load in different series and parallel combinations to achieve higher voltage at the output (Roy et al., 2021). SCMLI presented in Taghvaie et al. (2018) works on reducing the maximum voltage stress of switches by eliminating the h-bridge part. However, it utilized a bigger number of switches to achieve the required voltage level. Authors in Khoun Jahan et al. (2019) modified the CHB inverter by replacing the DC sources with switched capacitors. However, switches are controlled to sustain the balance of the switched capacitors. The seven-level SCMLI proposed in Siddique et al. (2020a) utilizes only two switched capacitors to realize the seven levels but with a large number of switching devices.

A general schematic of the proposed system is shown in **Supplementary Figure S1**. PV panel is connected to switched capacitor boost (SC-boost) converter. SC-boost converter extracts the maximum power from the PV panel and generates a three-level output voltage: V_{co1} , V_{co2} , and V_{co3} . The voltage on the three switched capacitor is utilized by the novel seven-level multilevel inverter to provide high-quality output voltage or to be integrated with the grid voltage. A control system is also divided into two parts: The maximum Power Point Tracking (MPPT) control part, which is used to control the SC-boost DC/DC converter to extract the maximum power from the PV panel, and the PI control with level-shift PWM to control the switches of the proposed seven-level multilevel inverter to control the output voltage in case of islanded operation or control the output current in case of grid integration case.

PROPOSED SWITCHED CAPACITOR SEVEN LEVEL MULTILEVEL INVERTER

The structure of the proposed two-stage switched-capacitor boost multilevel inverter is shown in **Supplementary Figure**

TABLE 1 | Switching states of the seven-level multilevel inverter.

| state | S ₂ | S ₃ | S ₄ | S ₅ | S ₆ | S ₇ | S ₈ | Output |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|--|
| V ₀ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | V _{co1} |
| V ₁ | 0 | 1 | 0 | 1 | 0 | 0 | 1 | V _{co1} + V _{co2} |
| V ₂ | 1 | 0 | 0 | 1 | 0 | 0 | 1 | V _{co1} + V _{co2} + V _{co3} |
| V ₃ | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| V ₄ | 0 | 0 | 1 | 0 | 1 | 1 | 0 | -V _{co1} |
| V ₅ | 0 | 1 | 0 | 0 | 1 | 1 | 0 | -(V _{co1} + V _{co2}) |
| V ₆ | 1 | 0 | 0 | 0 | 1 | 1 | 0 | -(V _{co1} +V _{co2} +V _{co3}) |
| V ₇ | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

S2. SC-Boost converter developed in (Tran et al., 2018; Farhadi-Kangarlu and Marangalu, 2019) is used as the first stage to boost PV voltage to a higher voltage level and extract maximum power from the PV panel; its three output switched capacitor is used as input to the proposed seven-level multilevel inverter. The proposed multilevel inverter is shown in **Supplementary Figure S3**.

It consists of seven switches, one of them, switch S₃, is without an antibody diode. Two switches are operating at a fundamental frequency, S₅ and S₇, and are operating in a complementary manner. In each switching state, only three switches are conducting at the same time. Output voltage is a staircase of seven levels. The inverter has eight valid switching states, as shown in **Supplementary Figure S4** and **Table 1**.

Mode 1 takes place by activating switches S₄, S₅, and S₈ and deactivating switches S₂, S₃, S₆, and S₇. Output voltage is equal to capacitor C_{o1} voltage V_{co1} (see **Supplementary Figure S4A**).

Mode 2 In order to achieve this mode, switches S₃, S₅, and S₈ are ON, while switches S₂, S₄, S₆, and S₇ are OFF. Output voltage is equal to the sum of capacitor C_{o1} voltage and capacitor C_{o2} voltage, V_{co1}+V_{co2} (see **Supplementary Figure S4B**).

Mode 3 occurs by activating switches S₂, S₅, and S₈ and deactivating switches S₃, S₄, S₆, and S₇. Output voltage is equal to the sum of capacitor C_{o1} voltage, capacitor C_{o2} voltage, and capacitor C_{o3} voltage, V_{co1} + V_{co2}+V_{co3} (see **Supplementary Figure S4C**)

Mode 4 represents a freewheeling mode, where the output voltage is zero. As illustrated in **Supplementary Figure S4D**, switches S₅ and S₆ are ON, while switches S₂, S₃, S₄, S₆, and S₇ are OFF.

Mode 5 takes place by activating switches S₄, S₆, and S₇, and deactivating switches S₂, S₃, S₅, and S₈. Output voltage is equal to the negative of capacitor C_{o1} voltage V_{co1} (see **Supplementary Figure S4E**).

Mode 6 occurs by triggering switches S₃, S₆, and S₇ ON and triggering switches S₂, S₄, S₅, and S₈ OFF. Output voltage is equal to the negative of the sum of capacitor C_{o1} voltage and capacitor C_{o2} voltage, switches, while switches, -(V_{co2}+V_{co1}) (see **Supplementary Figure S4F**) of capacitor C_{o1} voltage, capacitor C_{o2} voltage, and capacitor C_{o3} voltage., -(V_{co2}+ V_{co3}+V_{co1}) (see **Supplementary Figure S4G**).

Mode 8 is a freewheeling mode; output voltage is zero. Switches S₇ and S₈ are ON, while switches S₂, S₃, S₄, S₆, and S₅ are OFF (see **Supplementary Figure S4H**).

TABLE 2 | Comparison between different 7-level multilevel converters.

| | [21] | [22] | [23] | [24] | Proposed |
|---------------------|------|------|------|------|----------|
| Switches | 18 | 12 | 14 | 16 | 8 |
| Diodes | 0 | 0 | 0 | 0 | 5 |
| Floating capacitors | 2 | 1 | 2 | 1 | 0 |
| Voltage boosting | no | No | no | No | Yes |

Table 2 is a comparison between previously published 7-level inverters and the proposed one. The proposed converter has an optimum number of components plus the ability to step-up voltage.

The voltage gain of the converter is obtained considering the steady state analysis of the DC-DC converter, as below:

Charge state, which is illustrated in **Supplementary Figure S5A**, occurs when switch S_1 is turned on, activating the main switch capacitors C_1 , and C_2 to be connected in parallel with output capacitors C_{o1} and C_{o2} , and the main characteristic equation of this mode is as follow,

$$v_L = V_{pv} \quad (1)$$

$$V_{C1} = V_{Co1} \quad (2)$$

$$V_{C2} = V_{Co2} = V_{Co1} \quad (3)$$

Discharge state, which is illustrated in **Supplementary Figure S5B**, occurs when main switch S_1 is turned off. Inductors and supply are charging the output capacitors; main characteristic equation of this mode as follow:

$$v_L = V_{pv} - V_{Co1} \quad (4)$$

$$V_{Co3} = V_{Co2} = V_{Co1} \quad (5)$$

Considering the two modes, the voltage gain of the converter is given as:

$$M = \frac{V_o}{V_{in}} = \frac{3}{1-D} \quad (6)$$

A graph of the converter voltage gain is illustrated in **Supplementary Figure S6**, where the converter step-up ability is 3 times that of a traditional boost converter. Voltage and current stress of circuit-switching devices are illustrated in **Table 3**.

CONTROL APPROACH

A block diagram of the control system is depicted in **Supplementary Figure S7A**. As illustrated in the figure, PV voltage and current are measured and an MPPT control technique is applied to extract the maximum power from the PV. MPPT algorithm generates a reference signal to the PI controller. The reference signal generated by the MPPT is multiplied by unity amplitude sinusoidal waveform. PI controller is used to control the output voltage of the

TABLE 3 | Circuit parameters.

| Circuit parameters | |
|----------------------------|--------|
| Switching Frequency | 30 KHz |
| L | 1 mH |
| L_f | 3 mH |
| $C1 = C2$ | 400 uF |
| $C_{o1} = C_{o2} = C_{o3}$ | 400 uF |
| PV Module Specification | |
| Short Circuit Current (A) | 4.2 |
| Current at MPP(A) | 3 |
| Open Circuit Voltage (V) | 25 |
| Voltage at MPP(V) | 17.8 |

multilevel inverter in case of islanded operation or control the output current in case of a grid-connected system.

Level-Shift Pulse Width Modulation (LS-PWM) is generated to control the 7-level inverter proposed in this paper (Baksi and Behera, 2021), see **Supplementary Figure S7B**. Switching pattern of different switching devices is depicted in **Supplementary Figure S8**.

RESULTS AND DISCUSSIONS

In order to validate the proper operation of the proposed system, the system is simulated using MATLAB/SIMULINK platform; system parameters are given in **Table 3**. PV panel is controlled to generate its maximum power under different operating conditions. P&O algorithm is applied to the DC-DC converter to extract the maximum power from the PV panel. The algorithm introduces a perturbation ΔD in the duty succession and henceforth a modification in the going power is sensed. The increase in output power indicates that the controller becomes close to the maximum power point. Consequently, in the succeeding sampling cycle, the direction (slope) of perturbation is kept the same and the duty cycle is further increased by an amount ΔD .

Once the algorithm reaches near the MPP, the process will go backward and forward around the MPP (see **Supplementary Figure S9**). PV panel is operating at its maximum power under different environmental conditions (see **Supplementary Figure S9**), an abrupt change in solar radiation takes place, and the controller extracts the maximum power in an efficient way. In **Supplementary Figure S10A**, the system is investigated under a resistive load. Output voltage is a staircase with seven levels, same as the load current. Capacitors C_{o1} , C_{o2} , and C_{o3} voltages are also displayed in the same graph. **Supplementary Figure S10B** is another case study with inductive load, output voltage, current, and capacitors voltage depicted in the graph. The grid integration case of the study is also considered; the proposed system is connected to the grid and its output is depicted in **Supplementary Figure S11**.

In order to investigate the system performance and assure its proper operation, the system is experimentally demonstrated using DSPICE 1202. Different cases of studies are investigated

and the results are depicted in **Supplementary Figure S12**. **Supplementary Figure S12A** represents the output where the load is resistive and **Supplementary Figure S12B** represent an inductive load case. The obtained results are consistent with simulation results. In order to test system efficiency under different step up-points, the system is simulated at different power levels and different step-up ratios. Simulated efficiency results are illustrated in **Supplementary Figure S17**.

CONCLUSION

Two-stage boost multilevel inverter is presented in this paper. The first stage is based on SC-Boost converter to boost PV low voltage and extract maximum power from the PV panel, and its switched capacitor serves as input sources to the second stage. The second stage of the two-stage inverter is constructed from a novel seven-level multilevel inverter to generate seven-level output voltage. The proposed seven level inverter has some distinct features such as its compact size, low cost, reduced number of switches, and less condition loss. This is because it is constructed from only seven switches and has eight possible switching states. In each switching state, three switches are ON at the same time. Level shift PWM is implemented to drive the switches of the multilevel inverter. Different case studies have been considered in simulation and in real-time simulation, with resistive load, inductive load, and a grid-connection case (Tian et al., 2018; Saeedifard et al., 2012; Wang et al., 2017; Pulikanti et al., 2013; Siddique et al., 2021; Siddique et al., 2020b; Iqbal et al., 2020; Wu et al., 2017).

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DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/**Supplementary Material**, further inquiries can be directed to the corresponding authors.

AUTHOR CONTRIBUTIONS

OA-R designed and performed the simulations and obtained the results; OA-R, HY, and ZM analyzed the obtained results. OA-R and ZM wrote the paper, which was further reviewed by HY. All authors have read and agreed to the published version of the manuscript.

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SUPPLEMENTARY MATERIAL

The Supplementary Material for this article can be found online at: <https://www.frontiersin.org/articles/10.3389/fenrg.2022.869662/full#supplementary-material>

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