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Design, Validation, and Economic Behavior of a Three-Phase Interleaved Step-Up DC–DC Converter for Electric Vehicle Application

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Due to the increasing number of direct current (DC) loads in electric vehicles (EVs), DC–DC converters are widely used in EV applications. Hence, a DC distribution system with DC–DC converters is more efficient. A three-phase interleaved step-up DC–DC converter (ISC) has been proposed for use in electric vehicles. Other uses of the proposed ISC converter include aircraft, satellites, industrial, and traction drives. The proposed converter is subjected to a thorough frequency response study, which is explained in detail. The design technique recommends the proper quantity of switches to be used in the system. The reduction in the number of switches results in a 94% increase in the efficiency of this converter. The economic aspects of ISC, such as cost analysis and its procedure, have been discussed. Design models were checked using MATLAB/Simulink, which was interfaced with the real-time simulator OPAL-RT (OP5700) to ensure that they were appropriate. The results have been presented in detail.

Keywords: step-up converter, interleaved converter, state space model, Bode plot, electric vehicles

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1 INTRODUCTION

Recently, the scarcity of fossil fuel resources and rising global warming concerns have become global worries. As a result, electric vehicles (EVs) are the most reliable and realistic solution for adhering to rigorous environmental safety laws (Saadi et al., 2020). The majority of these vehicles are equipped with battery packs capable of powering EVs (Karthikeyan et al., 2019). Power control units like DC–DC converters are considered a vital feature of modern EV chargers and provide a DC link between the battery and the inverter circuit (Babaei et al., 2017; Athikkal et al., 2018). A three-phase interleaved step-up DC–DC converter [ISC] designed for electric vehicles (EV) has been proposed. Additionally, the proposed ISC converter could be used in airplanes, satellites, industrial applications, and traction motor systems. The proposed ISC converter integrates the concepts of boost converter [BC] and interleaved converter [IC] to increase the voltage gain (Bonab et al., 2018; Saravanan et al., 2020). The inputs and outputs are connected in parallel, which ensures a uniform distribution of power in the switching period. This is called interleaving (Guilbert et al., 2016; Zhuo et al., 2019a). The primary characteristics of the boost DC–DC converter topology are as follows: *1*) ease of meeting EMI requirements, *2*) affordability, and *3*) ease of control. The drawbacks of the boost DC–DC converter topology are as follows: *1*) large capacitors are required, *2*) gain in voltage <4:1, *3*) parallel devices are necessary at high power levels, and *4*) the rate of ripples is high. The primary characteristics of an interleaved DC–DC converter are as follows: *1*) reduced size of passive components and input current ripples, *2*) greater voltage gain, and *3*) easier to manage. The

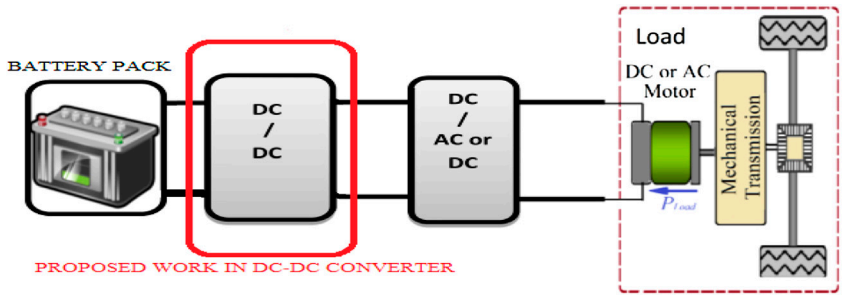

FIGURE 1 | Structure of electric vehicle.

drawbacks of the interleaved DC–DC converter topology include a larger component count and a significant switching loss. The proposed ISC is intended to overlook the limitations of existing converters. This work proposed an ISC converter to reduce the voltage stress and losses. This efficient method increases efficiency and voltage gain (Kolli et al., 2015; Babaei et al., 2018; Gupta et al., 2020). The proposed ISC converter is a three-phase interleaved step-up DC–DC converter [ISC]. This converter can be operated in a step-up mode of operation (Hegazy et al., 2012; Bharathidasan et al., 2022). Electric vehicle propulsion systems need high input voltage. Electric vehicles are designed and manufactured with high-energy battery packs to store the energy required to produce the required torque and speed (Guilbert et al., 2015; Zhuo et al., 2019b). The semiconductor switch with high resistance in the converter drops the input voltage (Hegazy et al., 2012; Yao et al., 2018). Therefore, semiconductor switches should be used with low equivalent resistance in electric vehicle propulsion applications (Wang et al., 2014a). MOSFETs and diodes have low equivalent resistance, making them ideal for use in converter circuits (Wang et al., 2014b; Padala and Yeddula, 2022). Furthermore, the conduction losses in the windings account for a greater proportion of the voltage drop than in other semiconductor devices in the converter (Kabalo et al., 2012; Wen and Su, 2015). The existing interleaved boost converter topology is similar to interconnecting multiple boost converter topology, which has been used in electric vehicles (Hasan et al., 2017; Zhang et al., 2020). The existing DC–DC converter topology for EVs may be a boost converter, buck-boost, and interleaved converter. These are widely used due to the downsizing features of battery packs. Once the battery packs are downsized, they will reduce the rated voltage (Lee et al., 2000; Khan et al., 2020). Aside from that, the battery pack provides rated voltage, which is enhanced by the DC-DC converter and is used to connect the battery to the transmission unit (Kirubakaran et al., 2009; Kabalo et al., 2013; Reddy and Sudhakar, 2018), as illustrated in **Figure 1**.

The single-phase interleaved converter in electric vehicles is incapable of supplying sufficient voltage to the transmission system (electric motor) (Chakraborty et al., 2019; Khan et al., 2021a). The proposed topology incorporates a three-phase interleaved boost converter that supplies the electric motor unit with sufficient voltage (Zaid et al., 2020; Khan et al., 2021b). The

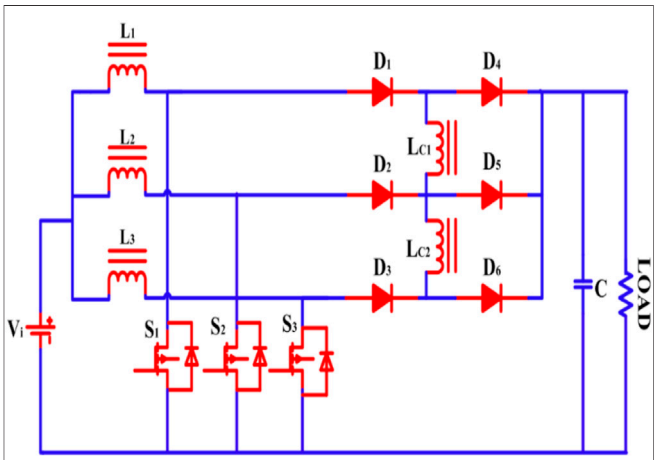

FIGURE 2 | Proposed three-phase interleaved step-up DC–DC converter [ISC].

voltage gain, voltage stress, and duty cycle of the ISC converter and the conventional interleaved boost converter are compared (Khan et al., 2021c; Zaid et al., 2021). A PI controller is constructed to achieve the closed response characteristics for the proposed converter (Maalandish et al., 2017; Khan et al., 2021d). The proposed converter's construction components are compared with the existing DC–DC converters (Li et al., 2012; Khalilzadeh and Abbaszadeh, 2015; Meier et al., 2018). Economic behavior is discussed in terms of a cost analysis of the proposed ISC converter (Aghdam and Abapour, 2016; Krishnachaitanya and Chitra, 2021). Hence, a high step-up is possible with the proposed ISC converter topology shown in **Figure 2**.

The converter topology is designed to combine a three-winding transformer between two phases, and the overall design makes a five-winding transformer. The high step-up operation produces a high output voltage to supply the motor propulsion and overcome the back emf produced in the drive. The windings L_1, L_2, and L_3 are directly connected to the battery. The central windings L_{C1} and L_{C2} are connected to the cathodes of the diodes D_1, D_2, D_3, and the anodes of the diodes D_4, D_5, and D_5. Additionally, the ISC converter design consists of three power semiconductor switches (S_1, S_2, and S_3) and an output capacitor (C) connected

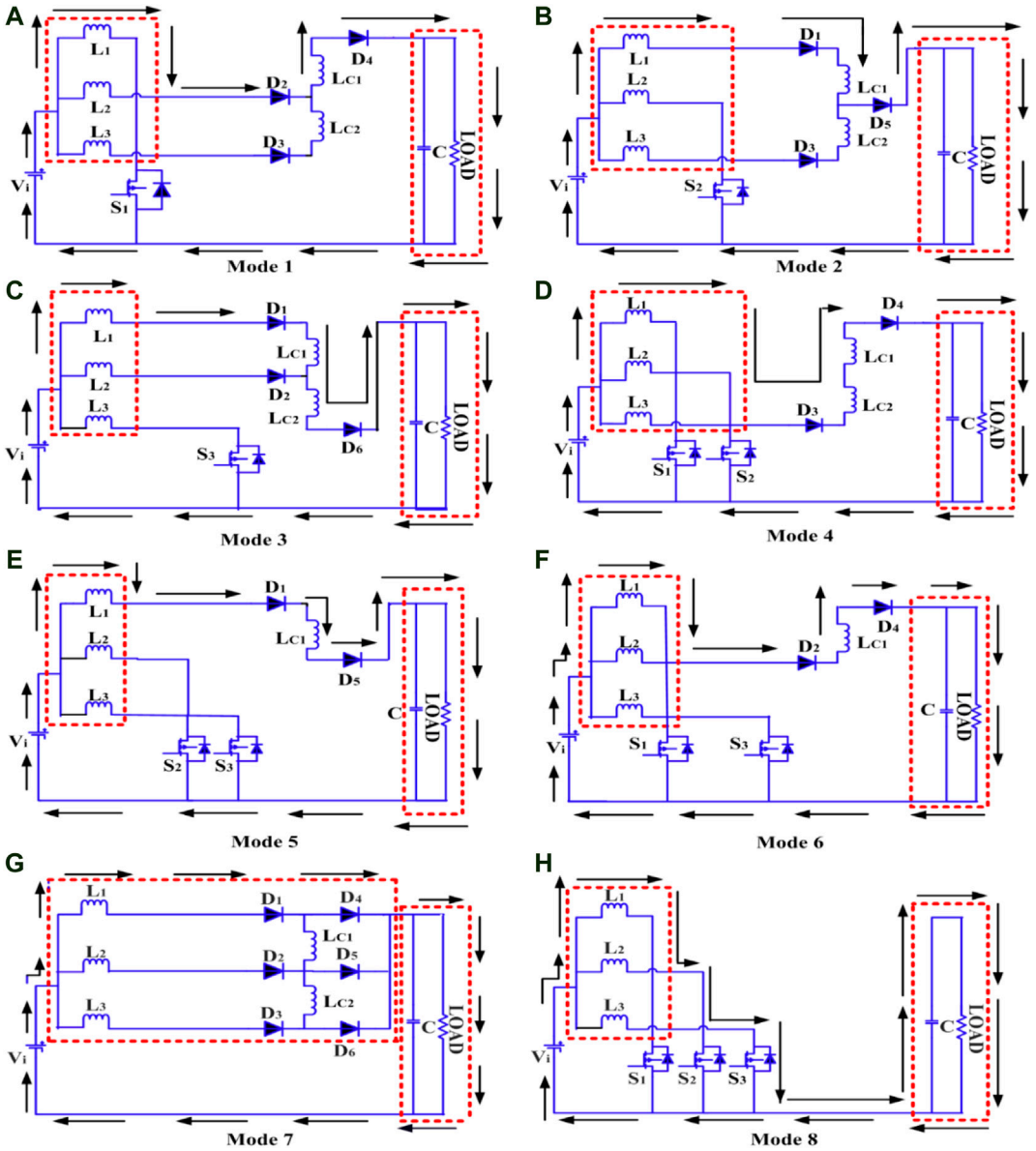

FIGURE 3 | Modes of operation.

across the load. Additionally, a freewheeling diode is connected across the switches to freewheeling the leakage current through the switch. In this work, the three-phase interleaved boost converter is designed and validated. The steady-state analysis and state space model of this converter topology is derived. Frequency response analysis is also derived from the state space model of this converter, which proves the converter's stability. In addition to that, the number of switches is reduced by this topology. Hence, switching losses are also being reduced in the ISC converter topology. The proposed ISC converter topology is capable of producing 139 V of output voltage and producing a power range of 881 W. Hence, this converter design attains high voltage gain and is suitable for medium and high-power applications. This proposed ISC converter design is simulated by the MATLAB/Simulink model and interfaced with the real-time simulator OPAL-RT (OP5700). The simulated outcomes clearly show that the proposed DC–DC converter is more competent and highly reliable when compared to other DC–DC converter topologies. The operational modes of the proposed ISC converter are presented in **section 2**. The steady-state analysis, which explains both voltage gain and voltage stress calculations, is described in **section 3**. In **section 4**, the proposed ISC converter's state space representation is explained. For stability analysis, frequency domain calculations are conducted based on state space modeling. The experimental results and discussions are presented in **section 5**, economic behaviors are interpreted in terms of cost analysis in **section 6** and the article is concluded in **section 7**.

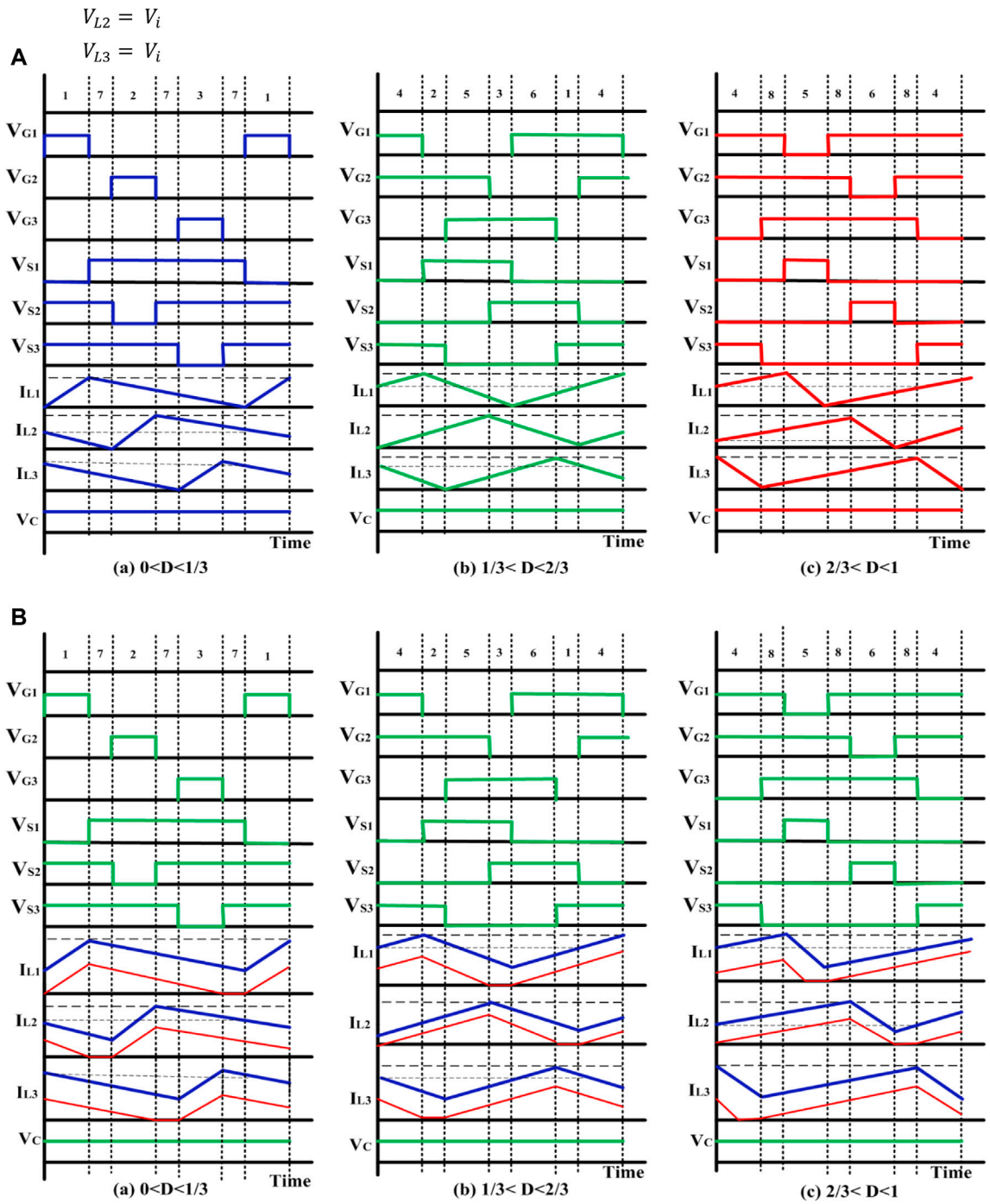

FIGURE 4 | Characteristics waveforms **(A)** BCM **(B)** CCM (blue line) and DCM (red Line).

2 OPERATING MODES OF THE PROPOSED ISC CONVERTER

The structure of ISC is shown in **Figure 2**. The proposed ISC converter modes of operation are discussed in **Figure 3**. The characteristic waveforms of BCM are depicted in **Figure 4A**, whereas the characteristic waveforms of CCM and DCM are depicted in **Figure 4B**. The turn's ratio is the ratio of the number of turns in the central winding (N_{c1}&N_{c2}) to the number of turns in the external winding (N_{e1}, N_{e2}&N_{e3}).

$$N = \frac{N_c}{N_e}. \tag{1}$$

Mode 1: as shown in **Figure 3A**, switch S1 is initially turned on, while switches S_2 and S_3 are turned off. Current from the battery flows through the winding L_1 and switch S_1. The battery current also conducts L_2 and L_3. Current flows through L_2 to D_2, L_{C1}, D_4, C, and the load. Current flows through L_3 to D_3, L_{C2}, L_{C1}, D_4, C, and the load. The voltage equation is given as

$$V_{L1} = V_i, \tag{2}$$

$$V_{L2} = V_i + V_{Lc1} - V_o,$$
$$V_{L2} = V_i + N(V_{L1} - V_{L2}) - V_o,$$
$$V_{L2}(1+N) = V_i(1+N) - V_o,$$
$$V_{L2} = \frac{V_i(1+N) - V_O}{(1+N)}, \tag{3}$$

$$V_{L3} = V_i + V_{Lc1} + V_{Lc2} - V_o,$$
$$V_{L3} = V_i + N(V_{L1} - V_{L2}) + \mathrm{N}(V_{L2} - V_{L3}) - V_o,$$
$$V_{L3}(1+N) = V_i(1+N) - V_o,$$
$$V_{L3} = \frac{V_i(1+N) - V_O}{(1+N)}. \tag{4}$$

Mode 2: as **Figure 3B** depicts, initially the switch S_2 is ON, and S_1 and S_3 are in an OFF condition. Current from the battery flows to the switch S_2 through the winding L_2. The battery current also conducts L_1 and L_3. Current flows through L_1 to D_1, L_{C1}, D_5, C, and the load. Current flows through L_3 to D_3, L_{C2}, D_5, C, and the load.

$$V_{L1} = \frac{V_i(1+N) - V_O}{(1+N)}, \tag{5}$$

$$V_{L2} = V_i, \tag{6}$$

$$V_{L3} = \frac{V_i(1+N) - V_O}{(1+N)}. \tag{7}$$

Mode 3: as shown in **Figure 3C**, the switch S_3 is initially turned on, while the switches S_1 and S_2 are turned off. Current from the battery flows through the winding L_3 and switch S_3. The battery current also conducts L_1 and L_2. Current flows through L_1 to D_1, L_{C1}, L_{C2}, D_6, C, and the load. Current flows through L_2 to D_2, L_{C2}, D_6, C, and the load.

$$V_{L1} = \frac{V_i(1+N) - V_O}{(1+N)}, \tag{8}$$

$$V_{L2} = \frac{V_i(1+N) - V_O}{(1+N)}, \tag{9}$$

$$V_{L3} = V_i. \tag{10}$$

Mode 4: as shown in **Figure 3D**, the switches S_1 and S_2 are initially turned on, while S_3 is turned off. Current from the battery flows through the winding L_1 and switch S_1, and through the winding L_2 and switch S_2. The battery current also conducts L_3, D_3, L_{C2}, L_{C1}, D_4, C, and the load. The voltage equation is given as

$$V_{L1} = V_i, \tag{11}$$

$$V_{L2} = V_i, \tag{12}$$

$$V_{L3} = \frac{V_i(1+N) - V_O}{(1+N)}. \tag{13}$$

Mode 5: as shown in **Figure 3E**, the switches S_2 and S_3 are initially turned on, and S_1 is turned off. Current from the battery flows through the winding L_2 and switch S_2, and through the winding L_3 and switch S_3. The battery current also conducts L_1, D_1, L_{C1}, D_5, C, and the load. The voltage equation is given as

$$V_{L1} = \frac{V_i(1+N) - V_O}{(1+N)}, \tag{14}$$

$$V_{L2} = V_i, \tag{15}$$

$$V_{L3} = V_i. \tag{16}$$

Mode 6: as **Figure 3F** depicts, initially S_1 and S_3 are turned ON, and S_2 is turned OFF. Current from the battery flows through the winding L_1 and switch S_1, and through the winding L_3 and switch S_3. The battery current also conducts L_2, D_2, L_{C1}, D_4, C, and the load. The voltage equation is given as

$$V_{L1} = V_i, \tag{17}$$

$$V_{L2} = \frac{V_i(1+N) - V_O}{(1+N)}, \tag{18}$$

$$V_{L3} = V_i. \tag{19}$$

Mode 7: as **Figure 3G** depicts, all three switches S_1, S_2, and S_3 are turned OFF. The battery current conducts the winding L_1, L_2, and L_3. Battery current conducts through the windings L_1 to D_1, D_4, C, and the load. Through L_2 current conducts D_2, D_5, C, and the load. Through L_3 current conducts D_3, D_6, C, and the load.

$$V_{L1} = V_i - V_o, \tag{20}$$

$$V_{L2} = V_i - V_o, \tag{21}$$

$$V_{L3} = V_i - V_o. \tag{22}$$

3 STEADY-STATE ANALYSIS

3.1 Continuous Conduction Mode (CCM)

Phase difference $\Phi = \frac{360^0}{n}$, $\Phi = 120^\circ$ (n = 3) (23).

The flux produced in the inductor winding is given as

$$\Phi_{c1} = \Phi_1 - \Phi_2, \tag{24}$$

$$\Phi_{c2} = \Phi_2 - \Phi_3. \tag{25}$$

The relationship between the central winding and external winding voltage is given as

$$V_{LC1} = N(V_{L1} - V_{L2}), \tag{26}$$

$$V_{LC2} = N(V_{L2} - V_{L3}). \tag{27}$$

Voltage gain (M) is the ratio of output voltage to the input voltage is given as

$$4V_iDT + 4V_i(1-D)T - \frac{3V_o}{1+N}(1-D)T - V_o(1-D)T = 0,$$
$$4V_i = V_o\left(\frac{3(1-D)}{1+N} + (1-D)\right),$$
$$\frac{V_o}{V_i} = \frac{4(1+N)}{(4+N) - D(4+N)}.$$

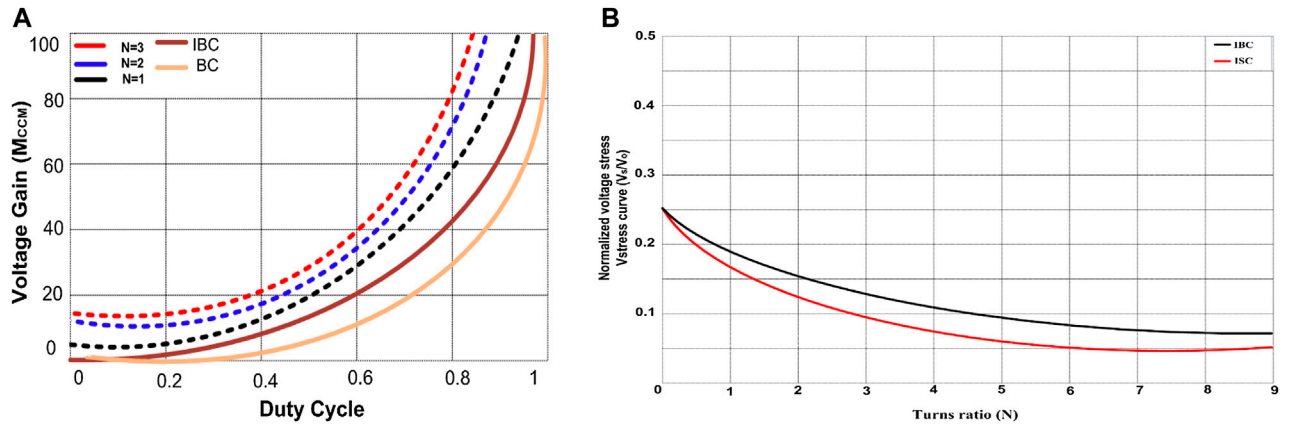

FIGURE 5 | (A) Duty cycle Vs Voltage gain with different turns ratio **(B)** Relationship between turns ratio and switch voltage stress.

The expression for the voltage gain is given as

$$M_{CCM} = \frac{V_o}{V_i} = \frac{4(1+N)}{(1-D)(4+N)}. \tag{28}$$

Figure 5 shows the relationship between voltage gain and duty cycle for the proposed ISC converter with different turns ratio. The curve clearly shows that the proposed ISC converter can provide higher output voltage than the conventional interleaved boost converter and conventional boost converter.

3.2 Switch Voltage Stress Calculation

The known inductor and capacitor voltages can be used to calculate all of the voltage stress on semiconductor components. The voltage stresses of the power switches and diodes are identical and they are calculated as follows:

$$\frac{V_o}{V_i} = \frac{4(1+N)}{(1-D)(4+N)},$$
$$V_o = \frac{4(1+N)V_i}{(1-D)(4+N)}. \tag{29}$$

The total voltage across the capacitor is

$$V_c = \frac{4(1+N)\,V_i}{(1-D)(4+N)},$$
$$V_c = V_o. \tag{30}$$

Since the capacitor is connected in parallel to the load, the voltage across the capacitor is equal to the output voltage.

$$Voltage\ stress\ of\ the\ switches\ \mathrm{V_s} = \frac{(1-D)V_o}{(4+N)D}. \tag{31}$$

Voltage stress of the diodes (V_d) is given as

$$V_d = V_o - V_s = \frac{4(1+N)V_i}{(1-D)(4+N)} - \frac{(1-D)V_o}{(4+N)D}, \tag{32}$$
$$V_d = \frac{4(1+N)(4-N)}{(1-D)(4+N)}. \tag{33}$$

Figure 5A shows the Duty cycle Vs Voltage gain with different turn ratios and **Figure 5B** shows the relationship between voltage stress and turns ratio, N. All of the component voltage stress is lower than the output voltage Vo. The voltage stress on the power switches and diodes is less than 0.5 V. As a result, the proposed ISC converter's semiconductor components are subjected to low voltage stress.

3.3 Input Current Ripples

The difference between the inductor's maximum ($\Delta i_{L,max}$)) and minimum ($\Delta i_{L,min}$) values of current are the ISC converter's input current ripple (Δi_{Ln}).

$$\Delta i_{Ln} = \Delta i_{L,max} - \Delta i_{L,min},$$
$$= \frac{V_i D}{L_n f} - \frac{V_o D(1-D)^2(4+N)^2}{4(1+N)}.$$

Under identical inductor current, output voltage, and input voltage conditions, the duty cycle of the ISC converter and the conventional three-phase interleaved boost converter (IBC) may be represented as

$$D = D_T - \sqrt{(D_T-3)(D_T-5)}\,. \tag{34}$$

The proposed ISC converter's reduction in input current ripple when compared to IBC can be represented as

$$\Delta i_T - \Delta i_{Ln} = \frac{V_i D_T}{L f} - \frac{V_i D}{L_n f},$$
$$= \frac{V_i D_T}{L_1 f} - \frac{V_i\left[D_T - \sqrt{(D_T-3)(D_T-5)}\,\right]}{L_1 f},$$
$$= \frac{V_i\sqrt{(D_T-3)(D_T-5)}}{L_1 f}, \tag{35}$$

where Δi_T is the input ripple of the IBC and D_T is the duty of the IBC.

3.4 Design of the Inductor and Capacitor

The current ripple is used to design inductors, and the voltage ripple is used to design capacitors. Current ripples of

the inductors and the value of inductance are given in **Eqs 37**, **38**.

$$\text{Input current ripples of the inductors } \Delta i_{Ln} = \frac{V_i D}{L_n f}, \tag{36}$$

$$\text{Range of inductor } L_n = \frac{V_i D}{\Delta i_{Ln} f}. \tag{37}$$

The capacitors are chosen based on the switching frequency and the output voltage ripple allowed across the capacitance-voltage connection, and other parameters are as follows:

$$\text{Output voltage ripple across the capacitance} - \text{voltage } \Delta V = \frac{V_O D}{RCf}, \tag{38}$$

$$\text{Range of capacitor } C = \frac{V_O D}{\Delta V R f}. \tag{39}$$

The value of the inductor and capacitor is calculated by using **Eqs 37**, **39**.

3.5 Discontinuous Conduction Mode (DCM)

The converter is analyzed in both continuous conduction mode and discontinuous conduction mode. In DCM, Current through the inductors can be calculated.

Mode 1: this mode is the same as CCM's mode 1 when switch S_1 is ON. The peak currents through the inductors L_1, L_2, and L_3 can be obtained as

$$i_{L1} = \frac{V_i}{L_1} DT, \tag{40}$$

$$i_{L2} = \frac{V_i (1+N) - V_o}{(1+N) L_2} DT, \tag{41}$$

$$i_{L3} = \frac{V_i (1+N) - V_o}{(1+N) L_3} DT. \tag{42}$$

Mode 2: this mode is the same as CCM's mode 2 when switch S_2 is ON. The peak currents through the inductors L_1, L_2, and L_3 can be obtained as

$$i_{L1} = \frac{V_i (1+N) - V_o}{(1+N) L_1} DT, \tag{43}$$

$$i_{L2} = \frac{V_i}{L_2} DT, \tag{44}$$

$$i_{L3} = \frac{V_i (1+N) - V_o}{(1+N) L_3} DT. \tag{45}$$

Mode 3: this mode is the same as CCM's mode 3 when switch S_3 is ON. The peak currents through the inductors L_1, L_2, and L_3 can be obtained as

$$i_{L1} = \frac{V_i (1+N) - V_o}{(1+N) L_1} DT, \tag{46}$$

$$i_{L2} = \frac{V_i (1+N) - V_o}{(1+N) L_2} DT, \tag{47}$$

$$i_{L3} = \frac{V_i}{L_3} DT. \tag{48}$$

Mode 4: this mode is the same as CCM's mode 4 when switch S_1 and S_2 are ON. The peak currents through the inductors L_1, L_2, and L_3 can be obtained as

$$i_{L1} = \frac{V_i}{L_1} DT, \tag{49}$$

$$i_{L2} = \frac{V_i}{L_2} DT, \tag{50}$$

$$i_{L3} = \frac{V_i (1+N) - V_o}{(1+N) L_3} DT. \tag{51}$$

Mode 5: this mode is the same as CCM's mode 5 when switch S_2 and S_3 are ON. The peak currents through the inductors L_1, L_2, and L_3 can be obtained as

$$i_{L1} = \frac{V_i (1+N) - V_o}{(1+N) L_1} DT, \tag{52}$$

$$i_{L2} = \frac{V_i}{L_2} DT, \tag{53}$$

$$i_{L3} = \frac{V_i}{L_3} DT. \tag{54}$$

Mode 6: this mode is the same as CCM's mode 6 when switch S_1 and S_3 are ON. The peak currents through the inductors L_1, L_2, and L_3 can be obtained as

$$i_{L1} = \frac{V_i}{L_1} DT\ , \tag{55}$$

$$i_{L2} = \frac{V_i (1+N) - V_o}{(1+N) L_2} DT, \tag{56}$$

$$i_{L3} = \frac{V_i}{L_3} DT. \tag{57}$$

Mode 7: this mode is the same as CCM's mode 7, when switch S_1, S_2, and S_3 is OFF. The peak currents through the inductors L_1, L_2, and L_3 can be obtained as

$$i_{L1} = \frac{V_i - V_o}{L_1} DT, \tag{58}$$

$$i_{L2} = \frac{V_i - V_o}{L_2} DT, \tag{59}$$

$$i_{L3} = \frac{V_i - V_o}{L_3} DT. \tag{60}$$

Mode 8: as **Figure 3H** depicts, all three switches S_1, S_2, and S_3 are turned ON, inductor current of the central windings L_{C1} and L_{C2} becomes zero. Battery current flows through the windings L_1 and S_1, through the windings L_2 and S_2, and through the windings L_3 and S_3. Furthermore, the capacitor C is discharged into the load. The voltage equation is given as

$$V_{L1} = V_i, \tag{61}$$

$$V_{L2} = V_i\ , \tag{62}$$

$$V_{L3} = V_i, \tag{63}$$

when switch S_1, S_2, and S_3 are ON. The peak currents through the inductors L_1, L_2, and L_3 can be obtained as

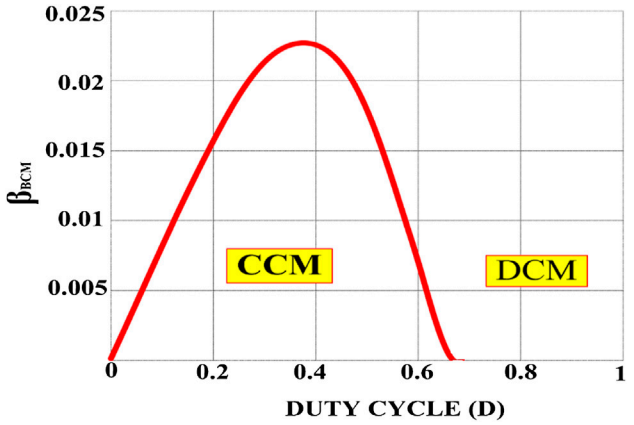

FIGURE 6 | Boundary normalized inductor time constant Vs duty cycle curve.

$$i_{L1} = \frac{V_i}{L_1} DT, \tag{64}$$

$$i_{L2} = \frac{V_i}{L_2} DT, \tag{65}$$

$$i_{L3} = \frac{V_i}{L_3} DT. \tag{66}$$

When the volt-sec balance principle is applied to the inductors, the following relationship is obtained:

$$D_1 = \frac{4D}{\frac{V_o}{V_i} - 4}, \tag{67}$$

$$\frac{2V_o}{R} = \frac{1}{2}(4+N)D(D+D_1)\frac{V_i}{Lf_s}, \tag{68}$$

$$\frac{V_o}{V_i} = \frac{(4+N)D(D+D_1)R}{4Lf_s}. \tag{69}$$

The normalized inductor time constant $\beta = \frac{4Lf_s}{R(4+N)}$.

With the use of **Eqs 67**, **69**, the following quadratic function can be calculated:

$$\left(\frac{V_o}{V_i}\right)^2 - 4\frac{V_o}{V_i} - \frac{4D^2}{\beta} = 0.$$

Voltage gain in DCM mode is given by

$$M_{DCM} = \frac{V_o}{V_i} = 1 + \sqrt{1 + \frac{D^2}{\beta}}. \tag{70}$$

3.6 Boundary Condition Mode Operation

This mode of operation allows the voltage gain of the CCM to be equivalent to the voltage gain of the DCM mode.

$$\frac{4(1+N)}{(1-D)(4+N)} = 1 + \sqrt{1 + \frac{D^2}{\beta}}.$$

Figure 6 depicts the boundary normalized inductor time constant β_{BCM} for CCM and DCM which is computed as follows:

$$\beta_{BCM} = \frac{D(1-D)^2(4+N)^2}{4(1+N)}. \tag{71}$$

3.7 Efficiency Calculation for the Proposed ISC Converter

The efficiency equation is computed by taking all losses into account. Input power is the sum of all the losses and the output power.

3.7.1 Power Loss in the Switches

Power loss in the switch is the sum of conduction loss and switching loss. Current through the switches S_1, S_2, and S_3 are 2.5, 2.1, and 2.9 A, respectively and the resistance of the switches is 0.3Ω. The total power loss in the switch is 9.4 W which can be computed by the following formula:

$$P_{con} = I_{s1}^2 R_{s1} + I_{s2}^2 R_{s2} + I_{s3}^2 R_{s3},$$

$$P_{sw} = \sum_{i=1}^{3} \frac{1}{2} I_{si} V_{si} t_{off} f. \tag{72}$$

3.7.2 Power Loss in the Capacitor

Current through the capacitor is 6.3 A and the resistance of the capacitor is 0.1Ω. The total power loss in the capacitor is 4 W which can be found by the following formula:

$$P_{capacitor} = I_c^2 R_c. \tag{73}$$

3.7.3 Power Loss in the Diodes

Current through the diodes is D_1 to D_6 is 2.5, 2.9, 3.1, 3.5, 2.8, 3.2 A and the resistance of the diodes is 0.4Ω. The total power loss in the diodes is 25.8 W which can be determined by the following formula:

$$P_{diodes} = \sum_{i=1}^{6} I_{Di}^2 R_{Di}. \tag{74}$$

3.7.4 Power Loss in the Inductor Winding

Current through the inductor is 3.2, 3.3, 3.1, 3.8, 3.6 A and the resistance of the inductor is 0.4Ω. The total power loss in the inductor is 23.2 W which can be determined by the following formula:

$$P_{inductor} = \sum_{i=1}^{3} I_{Li}^2 R_{Li} + \sum_{i=1}^{2} I_{Lci}^2 R_{Lci}. \tag{75}$$

3.7.5 Efficiency of the Proposed ISC Converter

The output-to-input power ratio is known as efficiency. The sum of all losses and output power equals the input power. The efficiency of the proposed ISC converter is 94% which is calculated by the following formula:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{switch} + P_{capacitor} + P_{diodes} + P_{inductor}}. \quad (76)$$

4 STABILITY ANALYSIS OF ISC

The state space model provides the dynamic performance of the converter circuit. It is the mathematical approach to the circuit represented in matrix form with a minimum number of equations called state variables. A state space approach is derived for both the ON and OFF states of the converter circuit. State space analysis is used to derive the transfer function of the ISC.

General state space equation of the system $\dot{X} = Ax + Bu$.

Output equation $Y = Cx + Du$.

Here, A = state matrix,

B = input matrix,

C = output matrix,

D = direct transmittance matrix,

x = state vector,

u = unit vector,

$\dot{X}$ = input vector,

y = output vector.

Applying KVL for mode 1 shown in **Figure 3A**,

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1},$$
$$\frac{di_{L2}}{dt} = \frac{V_{in}}{L_2} - \frac{V_o}{L_2} - \frac{V_o}{L_{c1}},$$
$$\frac{di_{L3}}{dt} = \frac{V_{in}}{L_3} - \frac{V_o}{L_3} - \frac{V_o}{L_{c1}} - \frac{V_o}{L_{c2}},$$
$$\frac{dV_o}{dt} = \frac{i_{L2}}{C} + \frac{i_{L3}}{C} - \frac{V_o}{\mathrm{RC}}.$$

State space derived for mode 1 is $\dot{X} = A_1x + B_1u$.

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} - \frac{1}{L_{c1}} \\ 0 & 0 & 0 & \frac{-1}{L_3} - \frac{1}{L_{c1}} - \frac{1}{L_{c2}} \\ 0 & \frac{1}{C} & \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} B_1 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ \frac{1}{L_3} \\ 0 \end{bmatrix}. \quad (77)$$

Similarly, mode 2 is $\dot{X} = A_2x + B_2u$.

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} - \frac{1}{L_{c1}} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_3} - \frac{1}{L_{c2}} \\ \frac{1}{C} & 0 & \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} B_2 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ \frac{1}{L_3} \\ 0 \end{bmatrix}. \quad (78)$$

Similarly, mode 3 is $\dot{X} = A_3x + B_3u$.

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} - \frac{1}{L_{c1}} - \frac{1}{L_{c2}} \\ 0 & 0 & 0 & \frac{-1}{L_2} - \frac{1}{L_{c2}} \\ 0 & 0 & 0 & 0 \\ \frac{1}{C} & \frac{1}{C} & 0 & \frac{-1}{RC} \end{bmatrix} B_3 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ \frac{1}{L_3} \\ 0 \end{bmatrix}. \quad (79)$$

Similarly, mode 4 is $\dot{X} = A_4x + B_4u$.

$$A_4 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_3} - \frac{1}{L_{c1}} - \frac{1}{L_{c2}} \\ 0 & 0 & \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} B_4 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ \frac{1}{L_3} \\ 0 \end{bmatrix}. \quad (80)$$

Similarly, mode 5 is $\dot{X} = A_5x + B_5u$.

$$A_5 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} - \frac{1}{L_{c1}} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{C} & 0 & 0 & \frac{-1}{RC} \end{bmatrix} B_5 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ \frac{1}{L_3} \\ 0 \end{bmatrix}. \quad (81)$$

Similarly, mode 6 is $\dot{X} = A_6x + B_6u$.

$$A_6 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} - \frac{1}{L_{c1}} \\ 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & \frac{-1}{RC} \end{bmatrix} B_6 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ \frac{1}{L_3} \\ 0 \end{bmatrix}. \quad (82)$$

Similarly, mode 7 is $\dot{X} = A_7x + B_7u$.

$$A_7 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ 0 & 0 & 0 & \frac{-1}{L_3} \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} B_7 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ \frac{1}{L_3} \\ 0 \end{bmatrix}. \quad (83)$$

Similarly, mode 8 is $\dot{X} = A_8x + B_8u$.

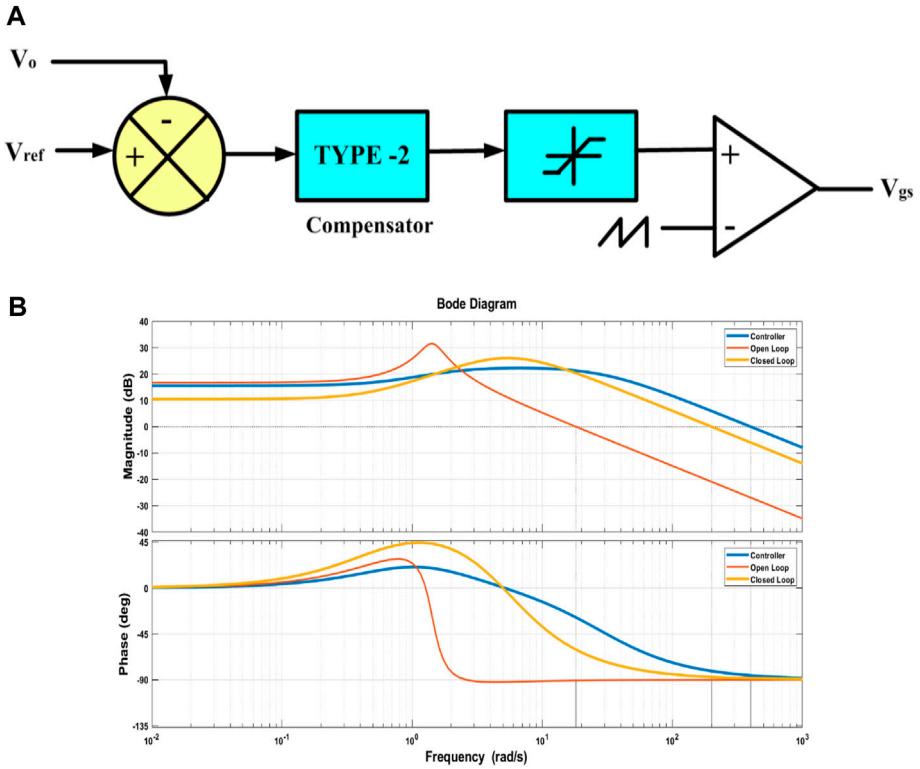

FIGURE 7 | (A) voltage control loop **(B)** Bode plot for open loop, closed loop, and compensator.

$$A_8 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{RC} \end{bmatrix} B_8 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ \frac{1}{L_3} \\ 0 \end{bmatrix}, \tag{84}$$

$$[A] = A_1d_1 + A_2d_2 + A_3d_3 + A_4d_4 + A_5d_5 + A_6d_6 + A_7d_7 + A_8d_8, \tag{85}$$

$$[B] = B_1d_1 + B_2d_2 + B_3d_3 + B_4d_4 + B_5d_5 + B_6d_6 + B_7d_7 + B_8d_8, \tag{86}$$

where duty cycle, $d = d_1 = d_2 = d_3 = d_4 = d_5 = d_6 = d_7 = d_8$.

The state space equation is $\dot{X} = Ax + Bu$.

$$\dot{X} = \begin{bmatrix} 0 & 0 & 0 & \left(\frac{-4}{L_1} - \frac{3}{L_{c1}} - \frac{1}{L_{c2}}\right)d \\ 0 & 0 & 0 & \left(\frac{-4}{L_2} - \frac{2}{L_{c1}} - \frac{1}{L_{c2}}\right)d \\ 0 & 0 & 0 & \left(\frac{-4}{L_3} - \frac{2}{L_{c1}} - \frac{3}{L_{c2}}\right)d \\ \frac{4d}{C} & \frac{4d}{C} & \frac{4d}{C} & \frac{-8d}{RC} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{8d}{L_1} \\ \frac{8d}{L_2} \\ \frac{8d}{L_3} \\ 0 \end{bmatrix} u. \tag{87}$$

The output equation is $Y = Cx + Du$.

$$Y = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ V_o \end{bmatrix} + 0\,u. \tag{88}$$

The closed loop transfer function can be derived for the proposed ISC converter topology from state space **Eqs 87**, **88** by MATLAB coding.

$$H(S) = \frac{0.212\,s + 0.201}{1.062s^4 + 1.23s^3 + 0.271s + 1.02}. \tag{89}$$

The transfer function and Bode plot are obtained by MATLAB coding from the matrices of the state space analysis. It is possible to observe the uncompensated bode plot and construct a suitable controller. Generally, a PI controller works best with lower-order systems. The uncompensated bode plot reveals that the system is stable, but contains zeros in the right half plane (Khan et al., 2021a). To maintain an appropriate phase margin, a compensator is designed to eliminate steady-state error and high-frequency disturbances. To optimize the performance of the proposed interleaved Step-up DC–DC converter [ISC], the voltage controller circuit depicted in **Figure 7A** evaluates both the reference and output voltages. **Figure 7B** shows the magnitude and phase plots of the interleaved step-up DC–DC converter [ISC]. In MATLAB, the dynamic response of an open loop and a closed loop is calculated. Although the bode plot of the uncompensated system is stable, the phase margin of the

TABLE 1 | Constructional components comparison of the DC–DC converters.

List of components	Component count			
	Khalilzadeh and Abbaszadeh (2015)	Li et al. (2012)	Meier et al. (2018)	Proposed ISC converter
Diode	6	6	8	6
Main switch	1	2	2	3
Inductor winding	3	6	2	5
Capacitor	6	5	5	1
Total components	16	19	17	15
Input current ripple	Low	High	High	Low
Voltage stress on the switch	$\frac{V_o}{2+n_2+n_3(2-D)}$	$\frac{V_o}{2(N+1)}$	$\frac{1}{2+nD}$	$\frac{(1-D)V_o}{(4+N)D}$
Voltage gain (V_o/V_i)	$\frac{2+n_2+n_3(2-D)}{1-D}$	$\frac{2(N+1)}{1-D}$	$\frac{2+nD}{1-D}$	$\frac{4(1+N)}{(1-D)(4+N)}$

TABLE 2 | Ratings of the components involved in the proposed topology.

Parameter		Range
Supply voltage	V_i	70 V
Duty cycle	D	30–40%
Switching frequency	*F*	50 kHz
Resistive load	R	40 Ω
Inductance winding	L_1	500 mH
	L_2	500 mH
	L_3	500 mH
	L_{C1}	500 mH
	L_{C2}	500 mH
Capacitor	C	3.7 mF
Output power	P_o	881 W

system is not desirable, which is 45°. For closed loop stability, the phase margin should be set at 79° to ensure the system has a suitable step response. Both the magnitude and phase plots of the interleaved step-up DC–DC converter are positive, indicating that the ISC circuit design will perform a stable operation. The proposed ISC converter has fewer switches, which decreases switching losses and lowers the circuit cost. The component quantity comparison is discussed in **Table 1**.

5 RESULTS AND DISCUSSION

To validate the performance of the ISC converter, an 881 W real-time simulation model is built in MATLAB/Simulink and interfaced with OPAL-RT (OP5700) with the specifications defined in **Table 2**. The converter is operated at a duty ratio of 30 and 40% in continuous conduction mode at a switching frequency of 50 kHz with a measured input voltage of 70 V and an output voltage of 139 V. The overall real-time interfacing setup using the OP5700 is shown in **Figure 8**. The characteristic waveform of the switch S_1, S_2, and S_3 are shown in **Figures 9–11**. The voltage across the switch S_1 is 52.9V, S_2 is 53.1 V and S_3 is 55.2 V. Voltage across the diode D_1 and the current waveforms of inductors IL1, IL2 and IL3 show that the converter is in the CCM mode of operation is shown in **Figure 12**. The inductor current achieves its maximum values linearly at 4.6, 3.9, and 4.2 A. Voltage across the diode D_2 and current through the coil

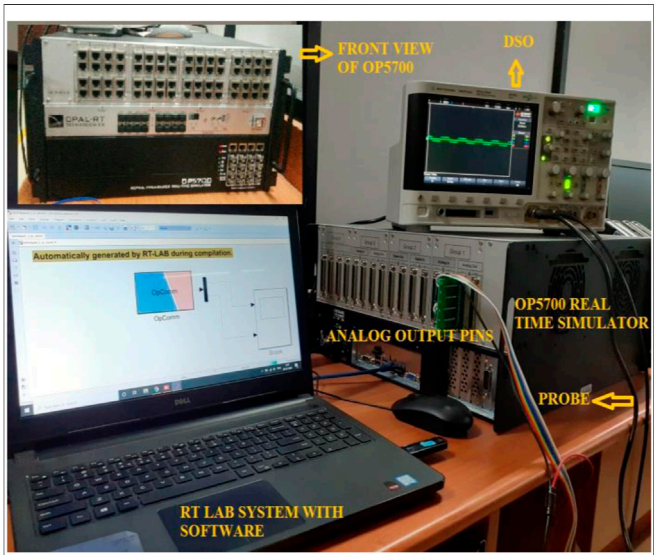

FIGURE 8 | Real-time setup using OP5700.

I_{LC1} is 3.8 A are shown in **Figure 13**. The converter's input voltage and the voltage across the diode D_3 **Figure 14**. The converter's input current and the voltage across the diode D_4 are shown in **Figure 15**. Capacitor voltage and the voltage across the Diode D_5 are shown in **Figure 16**. If the duty cycle increases from 0.3 to 0.4, the output voltage rises from 65 V to 145 V. The voltage across the capacitor is as same as the output voltage. The output voltage waveform with a measured voltage of 139 V of the converter and the voltage across the diode D_6 are shown in **Figure 17**. The current through the coil I_{LC2} is 3.6 A shown in **Figure 18**. The output current waveform with a measured current of 6.3 A for 40Ω is shown in **Figure 19**.

In **Figure 20A**, the efficiency of the converter is plotted against the output power, and when the output power increases, the efficiency gradually increases as well. The proposed converter's efficiency increases to 94% when the output power is increased from 400 to 881 W.

The loss distribution among semiconductor components is depicted in **Figure 20B**. According to the same chart, the highest power loss in the diodes (D_1 to D_6) is 41.6%. Switch losses (S_1, S_2,

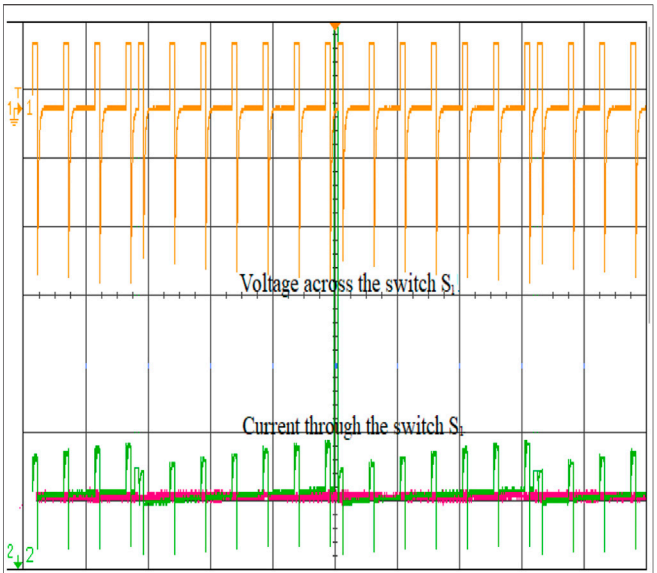

FIGURE 9 | Characteristics of switch S_1.

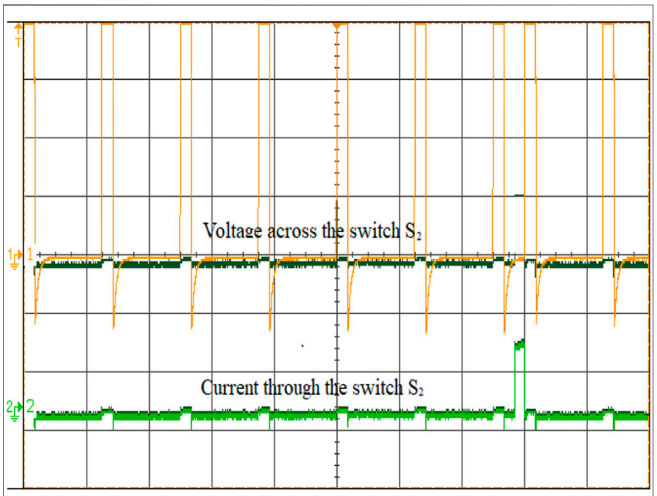

FIGURE 10 | Characteristics of switch S_2.

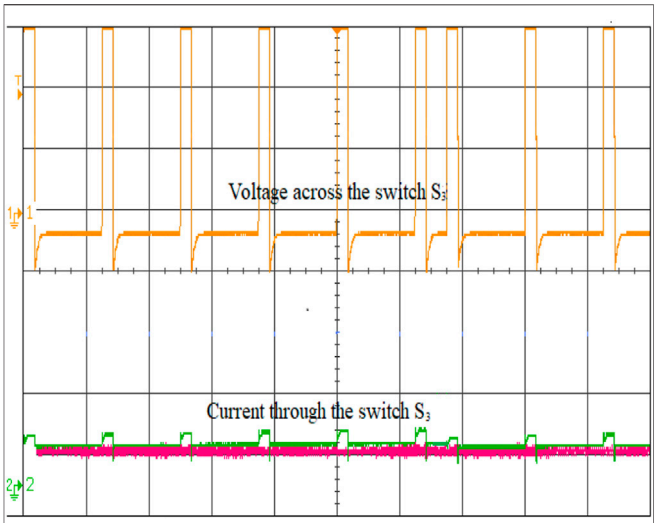

FIGURE 11 | Characteristics of switch S_3.

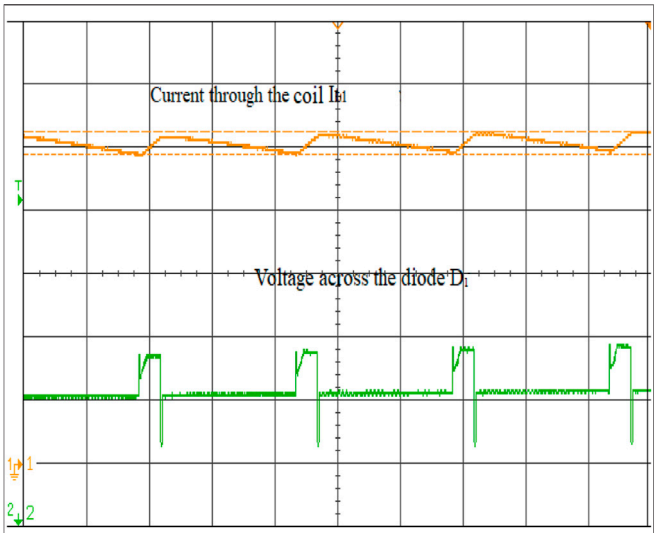

FIGURE 12 | Current through the coil I_{L1}.

and S_3) are 14.3%. Inductors and capacitors have total losses of 34.5 and 9.6%, respectively.

6 ECONOMIC BEHAVIOR OF THE ISC CONVERTER

Once examining economic behavior, it is necessary to take switching losses and the cost function into account. The number of power switches in the topology impacts the implementation cost. The performance of the equipment is proportional to its tangible cost. Costs are categorized as variable or fixed. The cost structure varies by product. The goal of this study is to determine the converter topology's cost. The variable cost of the product is related to the quantity manufactured, while the variable cost per unit is fixed. This results in a price discrepancy for the product; this is referred to as the "tangible cost," and it is used to estimate the price of the equipment.

However, because the fixed cost per unit changes according to the system, selecting products based on their fixed costs may result in economic loss. This is suited for products in modest quantities. The ISC converter's cost was estimated using a cost estimation tool that adheres to industry standards. The cost function of the ISC converter is proportional to the number of devices and DC voltage sources connected. Typically, the cost of electronics is dictated by the voltage, current, and power rating of the product. Thus, these are the components that contribute to

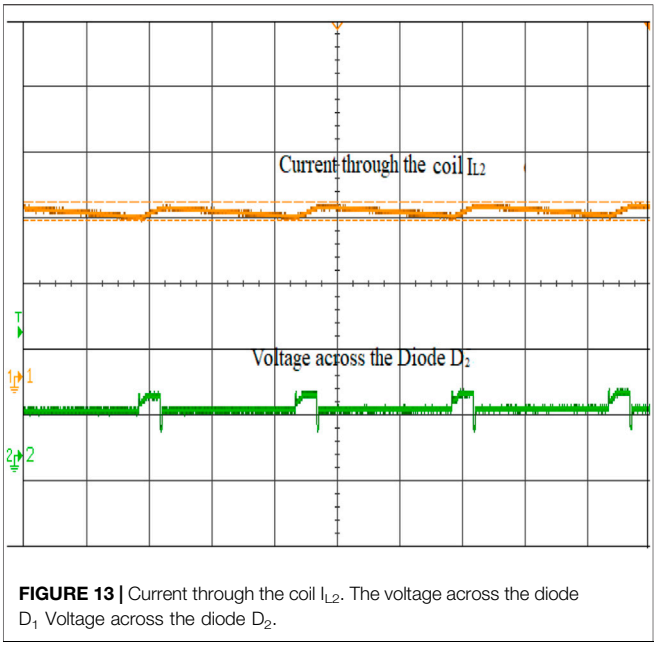

FIGURE 13 | Current through the coil I_{L2}. The voltage across the diode D_1 Voltage across the diode D_2.

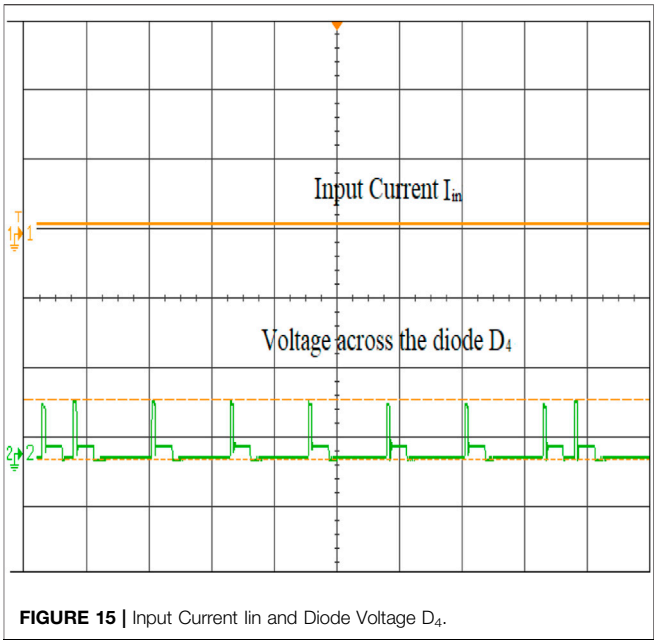

FIGURE 15 | Input Current Iin and Diode Voltage D_4.

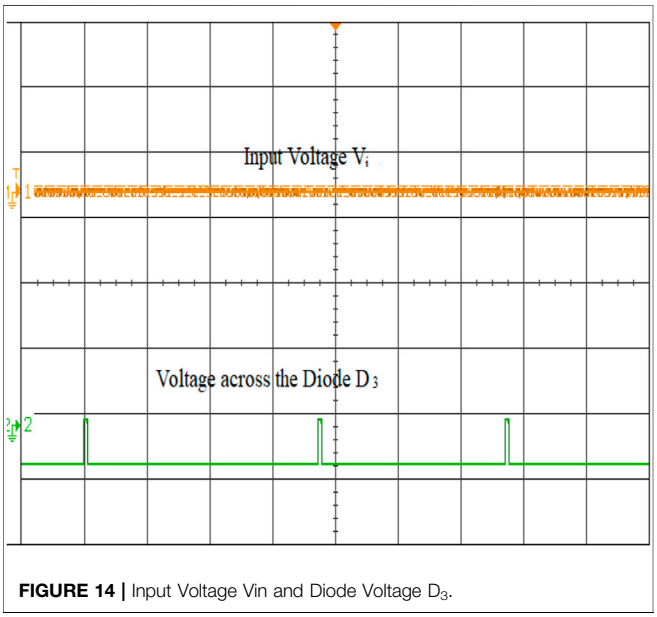

FIGURE 14 | Input Voltage Vin and Diode Voltage D_3.

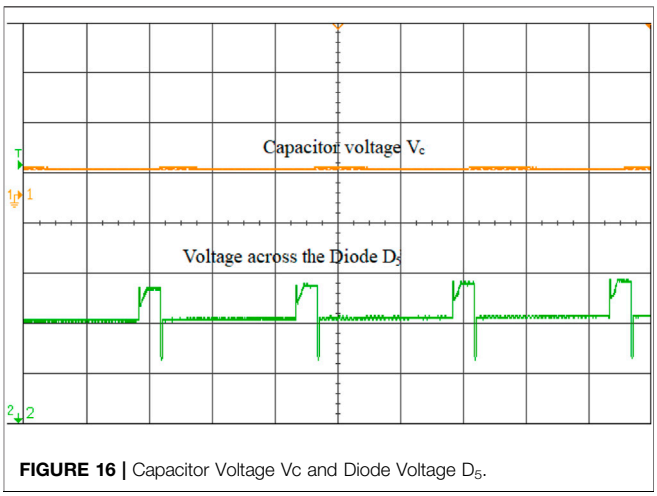

FIGURE 16 | Capacitor Voltage Vc and Diode Voltage D_5.

the cost assessment of the product. **Figure 21A** depicts the elements included in the proposed ISC converter's cost evaluation. The ISC Converter's implementation costs have been divided into four categories: primary level, secondary level, tertiary level, and final level. The entire sequence necessary to determine the cost of implementing the ISC is depicted in **Figure 21B**. ISC converter's total system cost comprises the initial installation cost, downtime costs, and power loss costs. The installation cost of the ISC converter comprises the investment in a power converter system. Three-phase ISC converters used in EV systems are composed of the following components: a battery, three power switches, six diodes, five inductors, and a capacitor. According to (Aghdam and Abapour, 2016), the cost of a single power MOSFET, a single inductor, a single diode, and a single capacitor is \$3.6, \$1.15, \$1.9, and \$1.5, respectively. As a result, the total cost of installation of three-phase ISC converters decreases.

$$C_{\text{install}} = (3.6 * N_{Sw}) + (1.9 * N_D) + (1.15 * N_{ind}) + (1.5 * N_c) + \text{battery cost}, \tag{90}$$

Where, N_{Sw} = number of switches, N_D = number of diodes, N_{ind} = number of inductors, and N_c = number of capacitors.

Downtime is defined as any period of time during which equipment is neither working nor producing. One week is necessary to replace the failed equipment. For a downtime period, a financial loss of \$2.5 per hour would be assumed. To

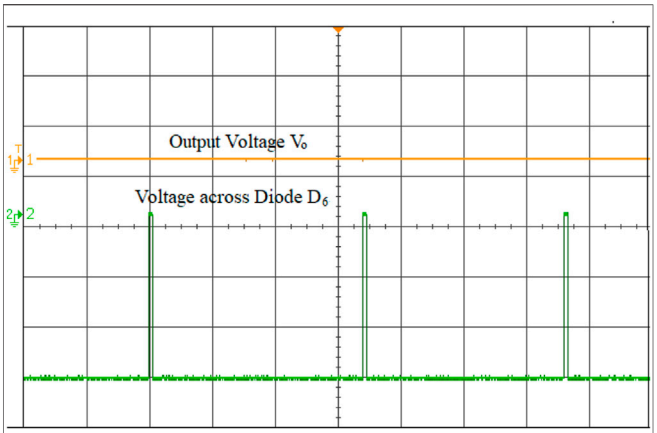

FIGURE 17 | Output Voltage Vo and Diode Voltage D_6.

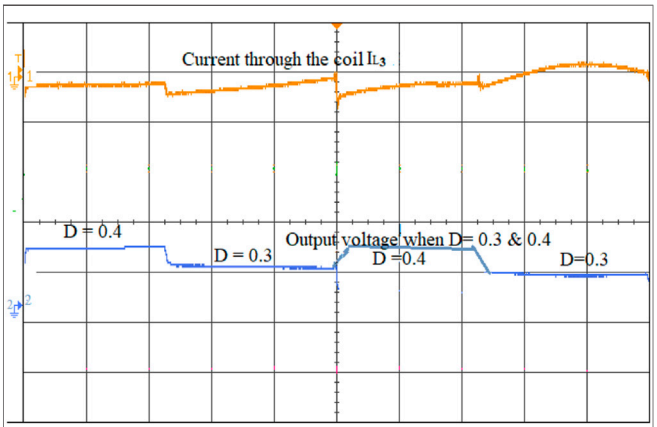

FIGURE 18 | Current through I_{LC2} and V_{out} at D = 0.3 and 0.4.

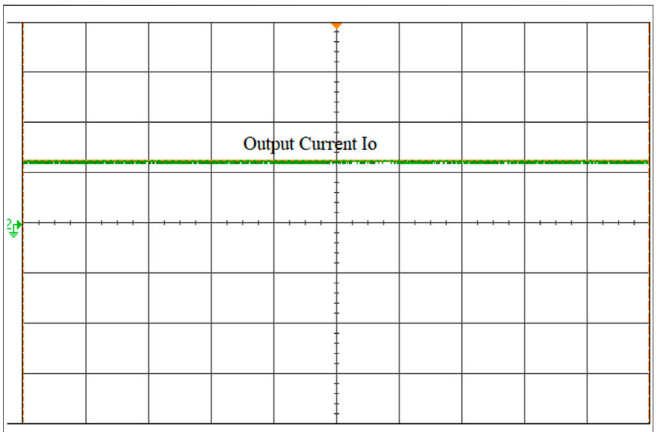

FIGURE 19 | Output current of the ISC converter.

calculate downtime costs, *N* years and mean time between failures (MTBF) are taken into account. MTBF is the average time between system failures.

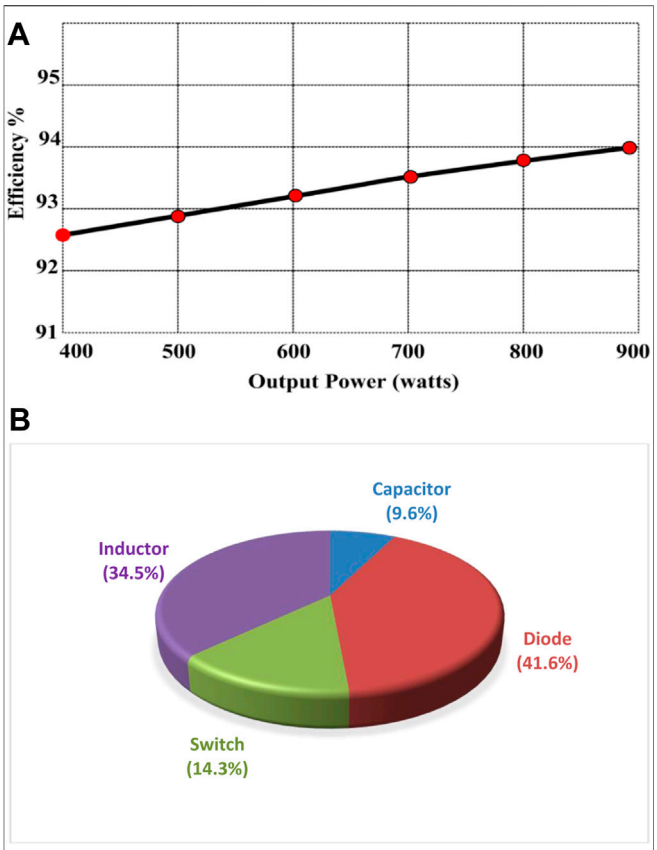

FIGURE 20 | (A) ISC converter's Efficiency with Various Output Power **(B)** Power Loss in various components.

$$C_{down} = \frac{N}{MTBF} * (24*7*2.5 + C_{install}). \quad (91)$$

Additionally, the cost of power loss is estimated to be $0.1 per kilowatt-hour. As a result, the total cost of power loss over 1 year is as follows:

$$C_{loss} = P_{loss}*365*24*0.1. \quad (92)$$

The following calculation can be used to determine the total cost of the ISC:

$$C_{tot} = C_{install} + C_{down} + C_{loss}.$$

The total cost of the proposed converter for 15 years is $1,211.3 and for 30 years $2387.1. Cost comparison of conventional interleaved converter Vs ISC is shown in **Table 3**. The calculated total cost of the proposed ISC is much lower than the conventional interleaved converter. Hence, it is economical.

The cost comparison clearly shows that the installation cost and the downside cost are nearly the same for both converters and that the cost of loss is higher in a conventional interleaved converter. In ISC, the cost of loss is very low than in conventional interleaved converters. Hence, the proposed ISC

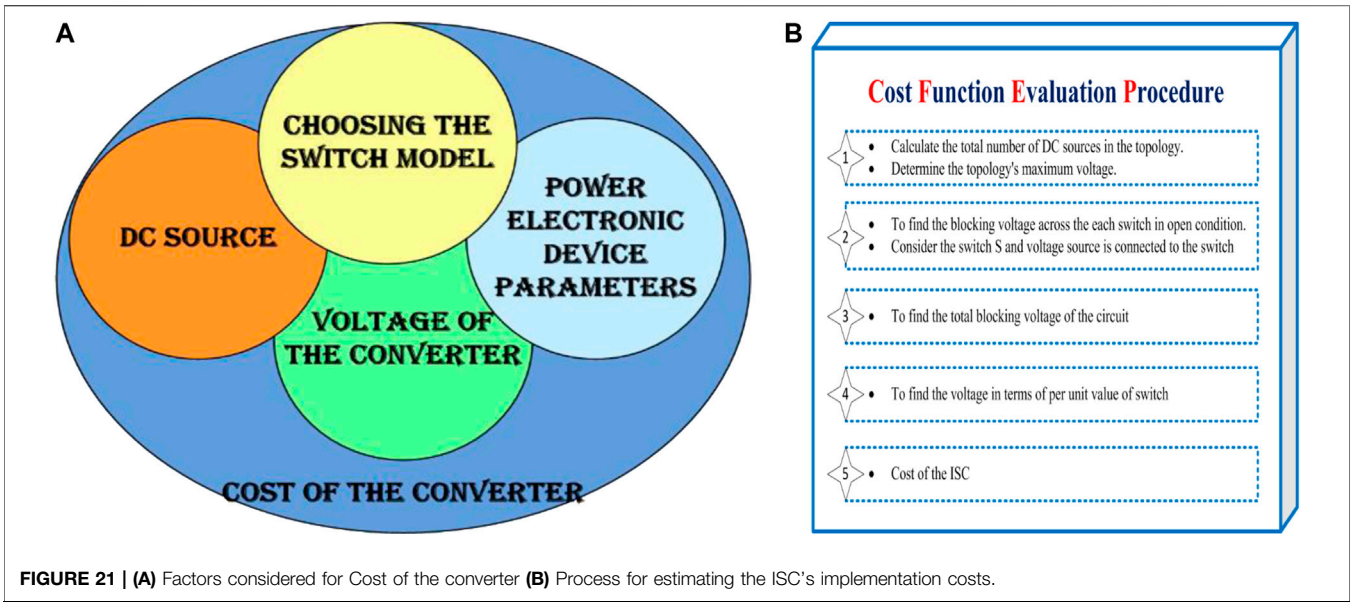

FIGURE 21 | (A) Factors considered for Cost of the converter **(B)** Process for estimating the ISC's implementation costs.

TABLE 3 | Cost comparison of conventional interleaved converter vs. ISC.

Interleaved converter topology	For 15 years				For 30 years			
	$C_{install}$	C_{down}	C_{loss}	C_{tot} ($)	$C_{install}$	C_{down}	C_{loss}	C_{tot} ($)
Conventional	29.3	449.3	984.7	1463.3	29.3	898.6	1969.4	2897.3
Proposed ISC	35.5	455.5	720.3	1211.3	35.5	911	1440.6	2387.1

reduces the cost of loss. As a result, the total cost is reduced for ISC. The proposed converter excels over conventional converters in terms of switching losses, efficiency, stability, and cost function. As a result, the proposed topology can be used in commercial applications because it is economically efficient.

7 CONCLUSIONS

The three-phase interleaved step-up DC–DC converter [ISC] has been proposed, and the topology performance has been validated by the analysis of stability in the frequency domain. The proposed converter operates in both closed and open loop modes, which results in the proposed converter ensuring stable operation. The operating concepts and theoretical analysis of CCM and DCM are thoroughly explored. The proposed topology has been compared to the existing topology in terms of its constructional features, which clearly shows the proposed converter has the minimum number of switches. Due to the reduction of switches in the proposed ISC converter, which reduces switching losses and lowers the cost of making the converter circuit. Hence, it is economically efficient. The implementation of the proposed topology has been performed in the environment of MATLAB/Simulink and interfaced with OPAL-RT (OP5700). It has also been demonstrated through experimental results that voltage stress on the semiconductor components is smaller than that of the output voltage. The real-time implementation of a maximum power rating of 881 W was tested, and the maximum efficiency was observed to be 94%. Additionally, it was revealed that decreasing the input voltage reduces efficiency due to increased conduction losses. The converter performed effectively under steady-state and dynamic-state behavior, and the experimental results were consistent with the theoretical predictions. The economic behavior of ISC has been discussed and compared with the conventional interleaved converter. The overall analysis clearly shows the proposed ISC is superior in terms of voltage gain, switching losses, efficiency, stability, and cost function. Since this topology is promising for EV applications.

8 FUTURE SCOPE

At a future point, a bidirectional version of the proposed ISC converter topology could be developed, with both step-up and step-down operations performed in the same circuit. At present, the converter is in step-up mode. The switches are connected in parallel with the diode. Once the main switch is turned off, the device enters step-down mode, and energy is saved in the battery, thereby achieving bidirectional operation. Bidirectional mode refers to the flow of power from the source to the load and *vice versa*. Furthermore, soft switching techniques are used. To minimize switching losses, soft switching approaches employ resonant mechanisms to turn on at zero voltage and turn off

at zero current. The reliability, stability, switching losses, economic efficiency, and economic behavior of the bidirectional version of the proposed ISC converter topology will be incorporated.

DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/Supplementary Materials; further inquiries can be directed to the corresponding author.

AUTHOR CONTRIBUTIONS

All authors listed have made a substantial, direct, and intellectual contribution to the work and approved it for publication.

SUPPLEMENTARY MATERIAL

The Supplementary Material for this article can be found online at: https://www.frontiersin.org/articles/10.3389/fenrg.2022.813081/full#supplementary-material

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