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MPC with Space Vector Phase-Shift PWM (SV-PSPWM) Technique with Harmonic Mitigation Strategy for Shunt Active Power Filters Based on H-Bridge Multilevel Converter

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This article presents a model predictive current control of a shunt active power filter based on 7-level cascaded H-bridge converters. By using the spacial vector modulation approach into the model predictive control, a considerable reduction of the computational burden is achieved and makes possible the real-time implementation in a custom experimental setup. Then, the current harmonics on the grid side, caused by non-linear loads connected to the point of common coupling, are compensated. The experimental results confirmed the feasibility and efficacy of the proposed controller.

Keywords: model predictive control, harmonics compensation, multilevel power converter, shunt active power filter, space vector mudulation

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INTRODUCTION

Nowadays, electrical distribution systems present a complex electrical scenario, where different dynamic load devices such as switching power supplies, rectifiers and AC motors are integrated (Habibullin et al., 2014; Mishra et al., 2020). This increasing number of connected devices causes problems such as increased reactive power and the harmonic distortion of the electrical current power grid. Consequently, other issues appear in the distribution grid, for instance, overheating of the conductors, current surges, high current consumption, which leads to resizing connections and possible damage to devices connected to the power grid (Motta and Faúndes, 2016; Das et al., 2020). Consequently, various types of equipment have been proposed to solve these power quality problems, namely.

- Shunt Active Power Filters (SAPF), to mitigate current harmonics (Jia et al., 2020).
- Static Distribution Compensators (DSTATCOM), to mitigate reactive power.
- Dynamic Voltage (DVR) to mitigate voltage unbalance disturbances (Ferreira et al., 2017).
- Unified Power Quality Conditioners (UPQC) to compensate for voltage and current quality problems (Irannezhad et al., 2012; Yang et al., 2021).

Within the SAPF literature, it has been studied extensively, from the different topologies of converters such as those based on Voltage Source Inverters (VSI), Neutral Point Clamped (NPC) and Cascade H-Bridge (CHB) converters (Jin et al., 2020; Po-Ngam, 2014). Depending on the configuration, they can consist of two levels or multilevel. CHB multilevel converters are increasingly seen as a promising solution due to their advantages, such as their high conversion

efficiency (Marzo et al., 2021), modular structure (Hekmati et al., 2021), scalability to extend to more levels (Ramos et al., 2020), and higher number of redundant switching states (Comparatore et al., 2017). Note that this system needs a DC-link that can be provided by using a power supply or capacitors. The power supply would increase the costs of the implementation since nine power supplies are required (Wang J. et al., 2020; Wong et al., 2020). For this reason, capacitors with a large capacitance are typically used to emulate a power supply (Qamar et al., 2020). However, the capacitors absorb and deliver energy at the Point of Common Coupling (PCC) point, and between the converters of the same phase, this causes fluctuations in the DC-link voltages and makes variations compared to the reference (Bosch et al., 2017; Tareen and Mekhielf, 2017).

From the control's point of view, the Proportional-Integral-Derivative (PID) and the Hysteresis control are the most applied techniques for power electronic converters. However, non-linear techniques such as the sliding mode control and the Model-based Predictive Control (MPC) have attracted attention in recent years. MPC has some advantages over the conventional linear current controller, such as important flexibility, including constraints and a suitable dynamic response (Rodas et al., 2021). However, MPC has one of its main disadvantages its high computational burden that makes it difficult to implement in complex systems. Also, MPC has a variable switching frequency that causes more significant stress on the switching devices and introduces non-linearities that propagate in the injected current. To solve MPC's variable switching behaviour, some modulation techniques such as Pulse-Width Modulator (PWM), Space Vector Modulation (SVM) (Li and Zhao, 2020; Ronanki and Williamson, 2018), and Modulated MPC have been included in the control scheme. Though, most of them are applied to two-level SAPF. On the other hand, for multilevel SAPF based on CHB, the most usual modulator are Phase-Shift PWM (PSPWM) and Level-Shift PWM (LSPWM). PSPWM has some advantages such as easy compression and that it performs a natural balancing of the capacitor voltages (Rao et al., 2020; Ferreira et al., 2017).

In what follows, some recent works carried out regarding the control and modulation techniques used in this work are presented. In (Tarisciotti et al., 2016), an MPC for a SAPF with the fixed switching frequency is proposed and named M2PC. The modulation is included in the MPC structure and then applied to the SAPF based on a two-level VSI to reduce THD currents. A fast multilevel SVPWM method based on the imaginary coordinate with direct control of redundant vectors or zero sequence components is proposed in (Yuan et al., 2020). This latter presents a modification of the SVPWM technique based on the imaginary coordinate system, which is applied to different topologies of multilevel converters. In (Li et al., 2021), a sliding mode SVPWM method for an HTS SAPF is studied. This non-linear controller is combined with the SVPWM technique to be applied to the two-level SAPF. A simplified 3-D NLM-Based SVPWM technique with voltage-balancing capability for three-level NPC cascaded multilevel converter is proposed in (Lin et al., 2019) that presents a modification of the SVPWM modulation technique based on the closest level modulation, applied to the multilevel NPC converter. The previous works show different applications of both the control and the modulation technique, where the proposal of this article is the MPC control technique in combination with the SVPWM modulation technique applied to a SAPF based on cascaded H-bridge converters of 7 levels. Then, in this paper, a method of reducing the switching states using the space voltage vectors consists of obtaining the switching states for the three-level configuration. Once the vectors are selected, they are projected for the 7 levels' configuration or more. The main advantage of this technique is the reduction of the computational burden by reducing the voltage vectors that allow the possibility of real-time implementation.

The main contribution of this research is the combination of the MPC with the SV-PSPWM technique applied to the 7-level CHB converter. In addition, a PI control is implemented to balance the DC-link voltages in the experimental platform. The proposed control scheme optimizes the prediction with voltage estimates in combination with the input and output signs of each CHB per phase, avoiding using a constant reference. The proposed MPC controller has been implemented in dSPACE-MicroLabBox platform. Also, tests of the control scheme have been carried out on the experimental bench using different operating points.

The article is organized as follows. In the following section, the mathematical model of SAPF applied in a three-phase system based on 7-level CHB SAPF topology is first presented. Subsequently, the current reference generator, the DC-link control, the predictive model, and the PSPWM modulation are presented. In **Section 3** the experimentalresults are shown and finally in **Section 4** the conclusions of the work are presented.

FUNDAMENTAL CONCEPTS, ISSUES, AND PROBLEMS

Three-phase SAPF Based on Multimodular CHB Converter Model

The right side of **Figure 1A** shows the general connection scheme of the multimodular SAPF based on 7-level CHB converters to a three-phase distribution power grid at the PCC point. Each CHB module is made up of a DC-link C_{dcx}^{ϕ} with a voltage v_{dcx}^{ϕ} and four SiC-MOSFET switching devices, connected 3 CHBs in series per phase. Each CHB cell consists of four trigger signals $S_{xy}^{\phi} = [0, 1]$, where S represents the trigger signals, $x = [1, 2, 3]$ the number of CHB corresponding per phase, $y = S_{11}, S_{12}, S_{31}$ and S_{32} represents the matrix of switching states according to Table 1, shown in **Figure 1C**, for phase a, performing the same analysis for the other phases and finally $\phi = [a, b, c]$ corresponds to the phases of the three-phase electrical power grid.

The mathematical model of the SAPF based on 7-level CHB converters is obtained by applying Kirchhoff's laws from the DC-link in the outgoing direction of the converter to the AC side of the electrical grid. The dynamics of the system is obtained:

$$\frac{\mathrm{d}i_c^{\phi}(t)}{\mathrm{d}t} = \frac{v_s^{\phi}(t)}{L_f} - \frac{v_c^{\phi}(t)}{L_f} - \frac{R_f i_c^{\phi}(t)}{L_f} \tag{1}$$

where i_c^{ϕ} represents the current injected by the filter at the PCC point in each phase, v_s^{ϕ} the voltages of the electrical power grid, L_f

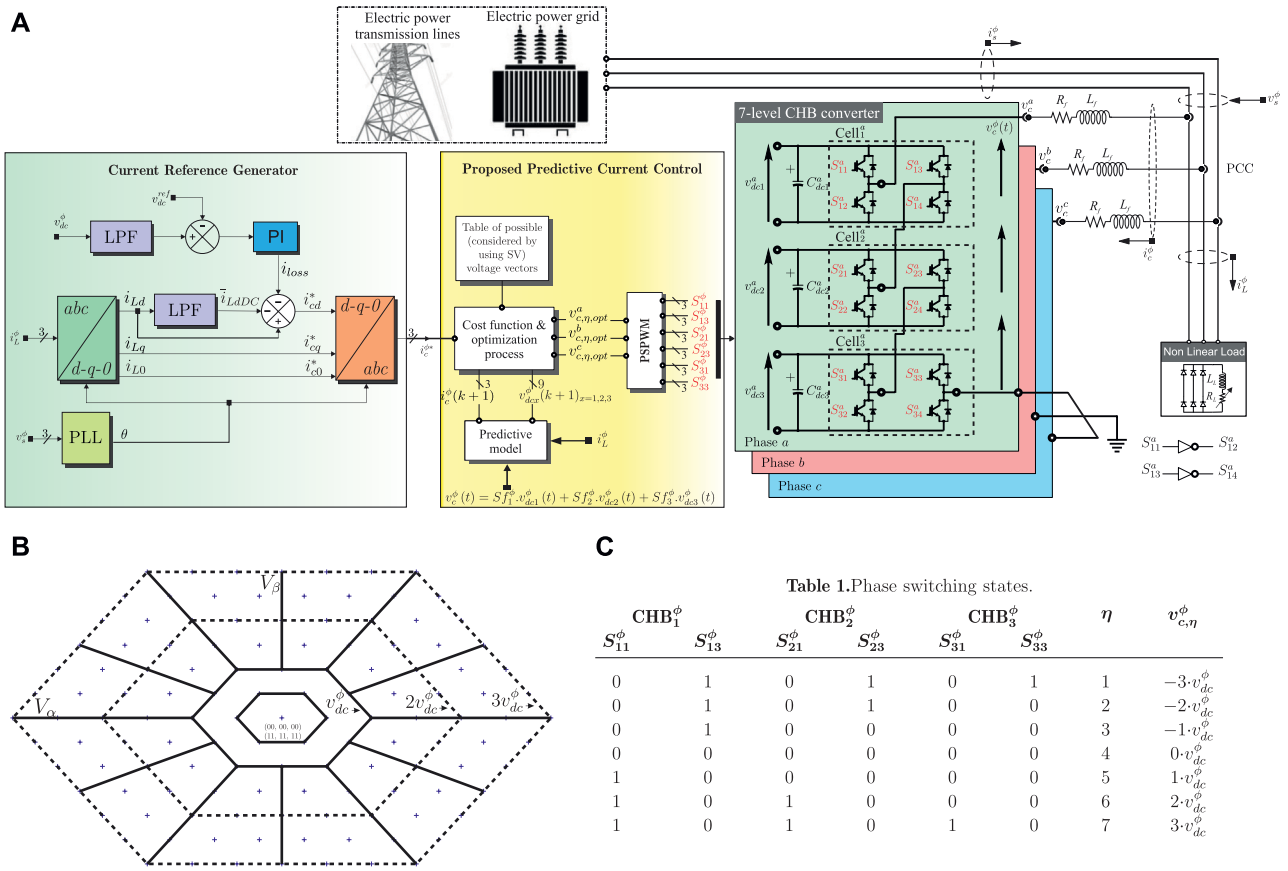

Table 1. Phase switching states.

CHB_1^ϕ		CHB_2^ϕ		CHB_3^ϕ		η	$v_{c,\eta}^\phi$
S_{11}^ϕ	S_{13}^ϕ	S_{21}^ϕ	S_{23}^ϕ	S_{31}^ϕ	S_{33}^ϕ		
0	1	0	1	0	1	1	$-3{\cdot}v_{dc}^\phi$
0	1	0	1	0	0	2	$-2{\cdot}v_{dc}^\phi$
0	1	0	0	0	0	3	$-1{\cdot}v_{dc}^\phi$
0	0	0	0	0	0	4	$0{\cdot}v_{dc}^\phi$
1	0	0	0	0	0	5	$1{\cdot}v_{dc}^\phi$
1	0	1	0	0	0	6	$2{\cdot}v_{dc}^\phi$
1	0	1	0	1	0	7	$3{\cdot}v_{dc}^\phi$

FIGURE 1 | (A) Control scheme for the 7-level APF based on H-Bridge converter. **(B)** 7-level space vector diagram in an $\alpha - \beta$ coordinate. **(C)** Phase switching states.

the output inductance of the filter, v_c^ϕ the output voltage of the converter and R_f the parasitic resistance of the inductance. Due to the CHB topology that uses independent DC-link using capacitors in combination with the activation signals, the model of the converter voltages is obtained:

$$v_c^\phi(t) = \left(Sf_{11}^\phi - Sf_{12}^\phi\right) v_{dc1}^\phi(t) + \left(Sf_{21}^\phi - Sf_{22}^\phi\right) v_{dc2}^\phi(t) + \left(Sf_{31}^\phi - Sf_{32}^\phi\right) v_{dc3}^\phi(t) \quad (2)$$

From this, the control model is obtained, avoiding using a fixed reference voltage. Instead, the measured voltages of each converter with its corresponding sign are used to get the real voltage outputs of the converter.

Current Reference Generation

The calculation of the reference currents $i_c^{\phi*}$ is based on the Synchronous Reference Frame (SRF). **Figure 1A** (left part) shows the detail procedure. First, the angle θ of the electrical power grid is obtained through a Phase Locked Loop (PLL). This angle is used to transform from $a-b-c$ plane to the $d-q-0$ plane, and viceversa. Then, a Low-Pass Filter (LPF) is used to eliminate the AC component of the load measurement current I_{Ld} (d-component).

Before the operation of the SAPF, all capacitors need to be charged to the reference voltage v_{dc}^{ref}. The SAPF during its operation can absorb or inject current into the electrical grid. This latter produces the charge and discharge of the C_{dcx}^ϕ capacitors of each CHB. Consequently, it causes the unbalance of the DC-link voltages (Li et al., 2017). To solve this issue, a Proportional-Integral (PI) controller is used that provides the loss current i_{loss} of the capacitors which is absorbed from the electrical grid (Sohagh et al., 2020). Therefore, the loss current represents the consumption currents in each phase of the C_{dcx}^ϕ capacitors, and the PI control is using to compensate this loss in such a way as to balance the voltage of the DC-link v_{dcx}^ϕ (Ray et al., 2017). The equations corresponding to the PI control in discrete time are shown below (Pandurangan et al., 2020; Zhou et al., 2020):

$$e^\phi(k) = v_{dc}^{ref} - v_{dc1}^\phi \quad (3)$$

$$i_{loss}^\phi = i_{loss}^\phi(k-1) + kp\left(e^\phi(k) - e^\phi(k-1)\right) + T_{PI}\, ki\, e^\phi(k) \quad (4)$$

$$i_{loss} = \frac{1}{3}\sum_{\phi=a,b,c} i_{loss}^\phi \quad (5)$$

where $e^\phi(k)$ represents the error between the reference and the previously filtered measured voltages v_{dc1}^ϕ. Then, the loss current i_{loss}^ϕ is calculated, $i_{loss}^\phi(k-1)$ being the loss current estimated in

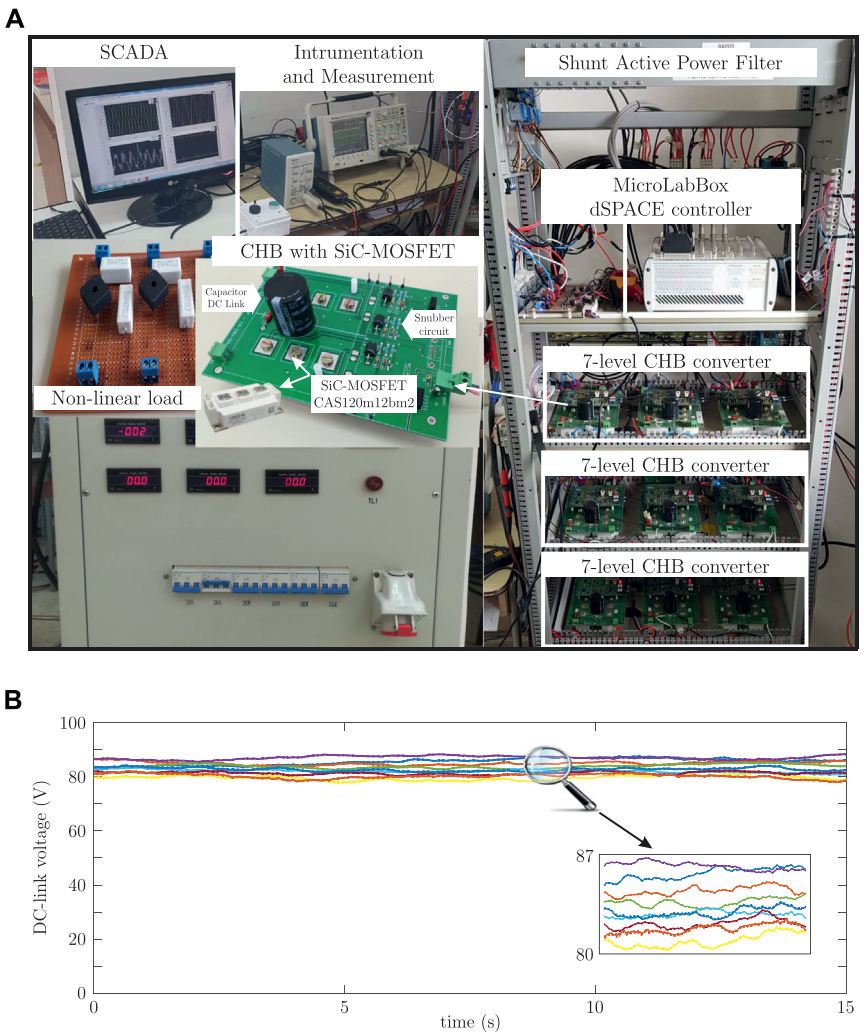

FIGURE 2 | (A) Picture of the experimental test bench. **(B)** DC-link voltage transient.

the previous instant, $e\,(k-1)$ the voltage error calculated during the last instant, T_{PI} represents the PI controller actuation time and finally i_{loss} which represents the average of the loss currents of each phase. Then, since the reference in d component of the current reference is obtained, the inverse Park transformation is applied to find the reference currents $i_c^{\phi *}$ to be used by the proposed model predictive current controller.

Predictive Model

The predictive model can be obtained from **Eq. 1** by using a forward-Euler discretization method (Boukezata et al., 2017). Euler's method is the most basic explicit method for numerical integration of ordinary differential equations and consequently carries a low computational burden, which benefits the experimental implementation (Jia et al., 2020). The SAPF discrete-time model is given by:

$$i_c^{\phi}(k+1) = \left(1 - \frac{R_f T_s}{L_f}\right) i_c^{\phi}(k) + \frac{T_s}{L_f}\left(v_c^{\phi}(k) - v_s^{\phi}(k)\right) \qquad (6)$$

where k identifies the actual discrete-time sample, T_s is the sampling time, and $i_c^{\phi}(k+1)$ is a prediction of the SAPF phase currents made at sample k. Also, In **Eq. 6**, $i_c^{\phi}(k)$ corresponds to the measured current at the output filter in the current sampling time k. While $v_s^{\phi}(k)$ corresponds to the measured phase voltage in the electrical grid at the same sampling time k. Then, these measured values are used by the predictive. Last, $v_c^{\phi}(k)$ is computed at each sampling instant using the discrete-time version of **Eq. 2**, and uses the measured DC-link capacitor voltages $v_{dc1}^{\phi}(k)$.

Cost Function and Optimization Process

In MPC technique, a cost function is calculated for different switching state conditions of a system under study to find the most suitable voltage vector. In other words, for all feasible switching state conditions, the cost function is computed, and then, the one that minimizes a pre-defined cost function is selected and applied during the next sampling time to the system. In this paper, the cost function is defined as the error between the prediction and the reference. In the three-phase

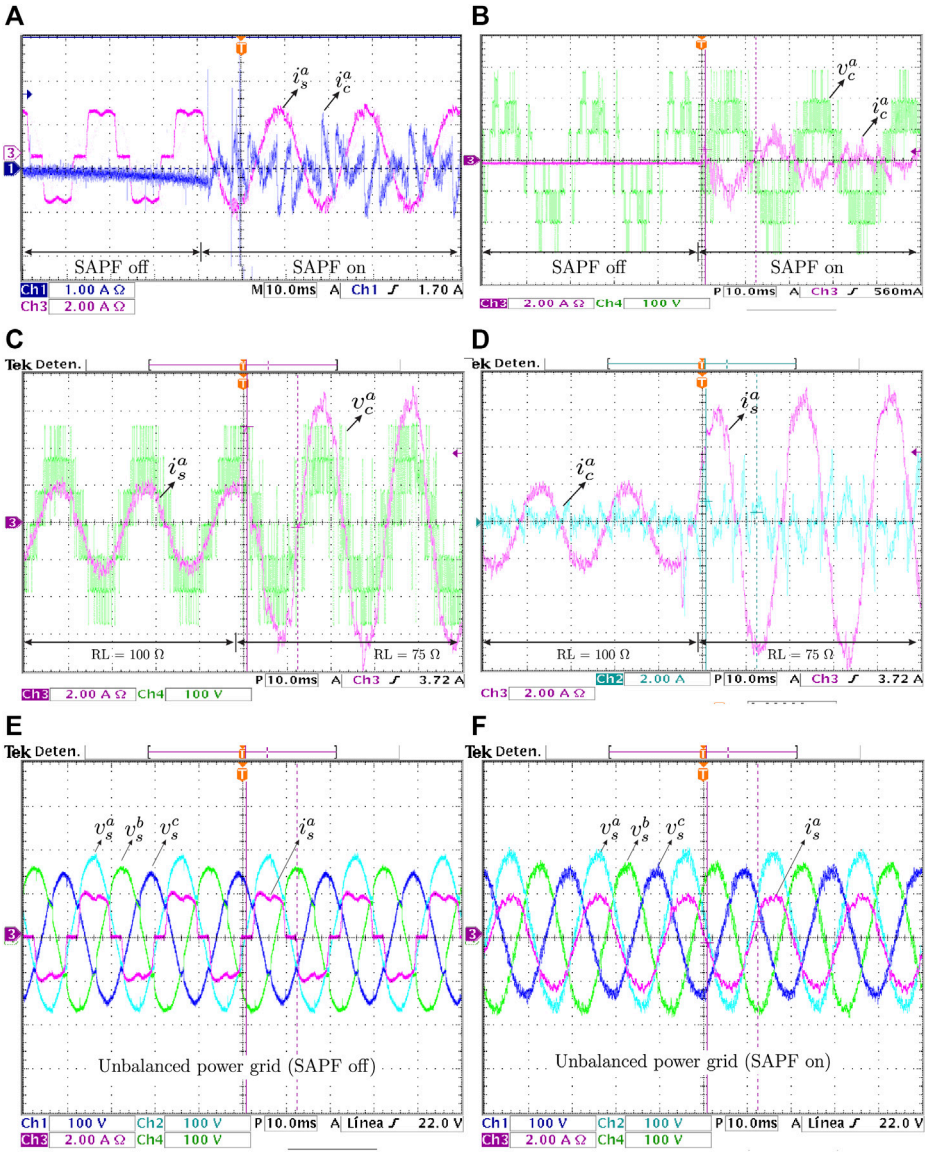

FIGURE 3 | Transient behavior of SAPF **(A)** source current harmonics compensation, **(B)** voltage and current output of SAPF, **(C)** current i_s^a and voltage v_c^a for instantaneous load resistance changes, **(D)** current i_c^a and i_s^c for increased load. Unbalanced voltages **(E)** uncompensated source current, **(F)** compensated source current.

control scheme, the cost functions are evaluated independently from the following equations:

$$\begin{aligned} g^a &= \| i_c^{a^*} - \hat{i}_c^a(k+1)\|^2 \\ g^b &= \| i_c^{b^*} - \hat{i}_c^b(k+1)\|^2 \\ g^c &= \| i_c^{c^*} - \hat{i}_c^c(k+1)\|^2. \end{aligned} \tag{7}$$

Next, the optimization algorithm selects the optimal vector $S_{\eta,opt}^{\phi}$ which corresponds to the voltage that minimizes the cost function, to then be sent to the modulator stage.

Space Vector Phase-Shift PWM Technique

As mentioned in the previous section, the optimization algorithm evaluates all feasible switching states. SAPF based on 7-level CHB converters, consists of $2^{\psi S_6}$ which is equivalent to 264 144 voltage vectors, where $S_{xy} = 6$ corresponds to the six control signals and $\psi = 3$ represents the three CHBs per phase. This latter leads to a high computational burden that makes it impossible to be implemented in digital signal processors available today. Therefore, in this paper, a modulation structure that consists of a combination of the vector space with phase shift modulation is proposed. The aim of this approach is to reduce the computational cost by reducing the number of vectors using as a base of 3-level CHB topology corresponding to one CHB per phase, where the vectors are represented as the first and second hexagons delineated as shown in **Figure 1B**, the third and fourth hexagon represent the second level by adding a CHB, the fifth and sixth hexagon define the third level by adding a third CHB (He et al., 2020). To

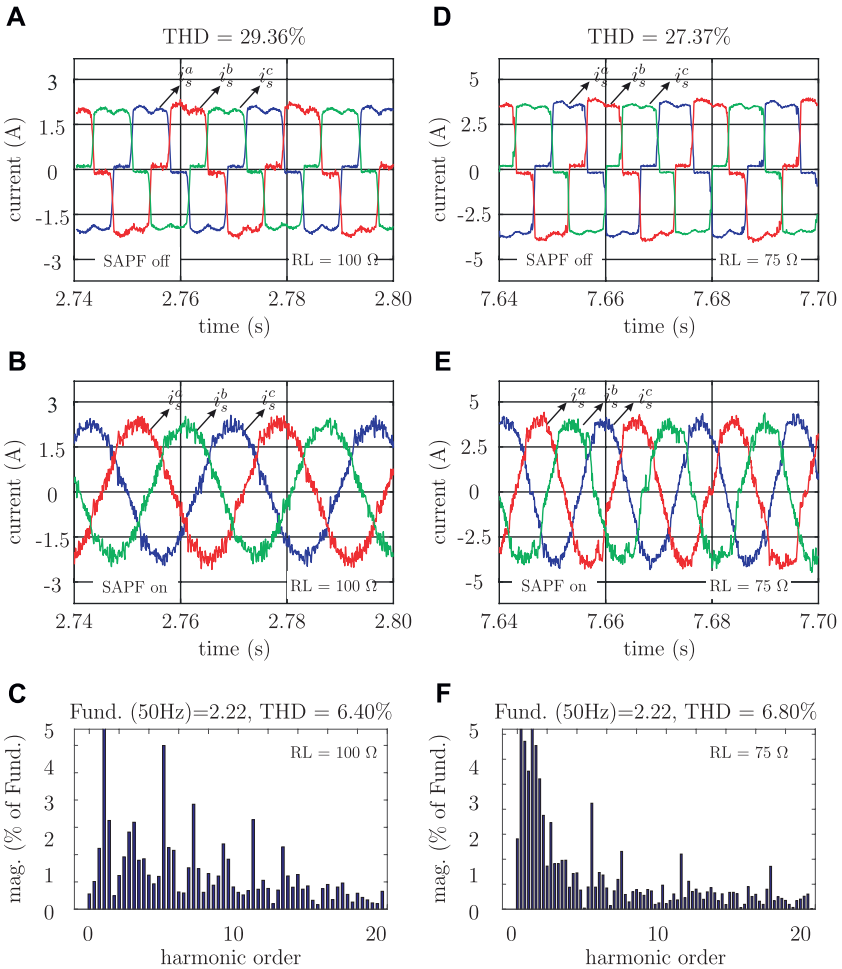

FIGURE 4 | Experimental results of source current harmonics compensation at the grid side considering a non-linear load and three operation points. **(A)** Uncompensated grid current for R_L = 100 Ω, **(B)** Compensated grid current for R_L = 100 Ω, **(C)** THD level of compensated grid current for R_L = 100 Ω. **(D)** Uncompensated grid current for R_L = 75 Ω, **(E)** Compensated grid current for R_L = 75 Ω, **(F)** THD level of compensated grid current for R_L = 75 Ω.

reduce the number of vectors, the first-level vectors extrapolate to the second and third levels. For instance, if the optimal switching states correspond to the first level are (1 0 1) to select the optimal voltage vectors corresponding to the second level is (2 0 2), the same analysis is carried out for the voltage vectors corresponding to the third level. This proposal significantly reduces the interactions from 264 144 to 54 corresponding to the number of points in the diagram in vector space and thus reducing the computational cost and making possible the real-time implementation (Wang C. et al., 2020; Yuan et al., 2020).

Once the optimal voltage level has been selected, the PSPWM is carried out, which consists of three triangular carriers $\frac{180°}{3}$ out of phase with each other with the same appliance and the same frequency to obtain the activation times of the trigger signals (Gregor et al., 2021).

$$v_{ct}^{\phi} = \frac{v_{c,\eta,opt}^{\phi}}{3} \tag{8}$$

where v_{ct}^{ϕ} is a normalized modulator between − 1 and 1, and $v_{c,\eta,opt}^{\phi}$ are the optimal voltage levels selected in the vector space. To make the thing clearer, Algorithm 1 summarizes the optimization process.

Algorithm 1. Optimization algorithm of the proposed modulated MPC current controller.

1. Initialize $g_{opt}^{a} := \infty, g_{opt}^{b} := \infty, g_{opt}^{c} := \infty, \eta := 0$
2. Compute the current references
3. **while** $\eta \leq \varepsilon$ **do**
4. $S_{\eta}^{\phi} \leftarrow S_{xy}^{\phi} \; \forall \; x \; \& \; y = 1, 2, 3$
5. Calculate the prediction currents
6. Compute the cost function
7. **if** $g^{a} < g_{opt}^{a}$ **then**
8. $g_{opt}^{a} \leftarrow g^{a}, \;\; S_{opt}^{a} \leftarrow S_{\eta}^{a}$
9. **end if**
10. **if** $g^{b} < g_{opt}^{b}$ **then**
11. $g_{opt}^{b} \leftarrow g^{b}, \;\; S_{opt}^{b} \leftarrow S_{\eta}^{b}$
12. **end if**
13. **if** $g^{c} < g_{opt}^{c}$ **then**
14. $g_{opt}^{c} \leftarrow g^{c}, \;\; S_{opt}^{c} \leftarrow S_{\eta}^{c}$
15. **end if**
16. $\eta := \eta + 1$
17. **end while**
18. Compute the modulation signals
19. Get the turn-on times of the firing signals
20. Apply the firing signals.

EXPERIMENTAL ASSESSMENT

The DSPACE MicroLabBOX was used as controller in an experimental bench of SAPF based on 7-level CHB connected to a balanced power grid with a non-linear load. Each converter uses a SiC-MOSFET switching devices and a DC-link as shown in **Figure 2**. Then, to verify the performance of the proposed MPC technique, several experimental tests have been carried out using the following parameters: v_s^{ϕ} = 120 Vrms, v_{dc}^{ref} = 85 V, C_{dcx}^{ϕ} = 23 420 uF, L_f = 10 mH, carrier frequency f_c = 1 kHz for the PSPWM.

First, the DC-link voltage regulation is analyzed. The PI control parameters are kp = 0.587 and ki = 0.293 5. So, to verify the PI control that acts on the load and balance of the DC-link voltages, the dynamic response of the voltages v_{dc}^{ϕ} is shown in **Figure 2B**. Taking into account a reference voltage v_{dc}^{ref} = 85 V, a balance of the voltages can be observed with an error of ± 5 V which represents an error of approximately 5%.

Then, a dynamic analysis of the SAPF is performed. **Figures 3A,B** show the measured current i_c^a at the converter output before and after activating the SAPF. It can be notice, in **Figure 3A**, how the grid current i_c^a is compensated with a sinusoidal waveform. **Figure 3B** includes the voltage v_c^a of 7 levels at the converter output. In **Figure 3C** the dynamic response of the converter output voltage v_c^a and the electrical power grid current i_s^a are presented when a load change occurs R_L = 75 Ω to R_L = 50 Ω. A good dynamic response can be observed with a low current injection of about 2 A peak-to-peak to 6 A peak-to-peak. In **Figure 3D** the current injected by the filter i_c^a is shown against the variation of the load and the current of the electrical power grid i_s^a when the load varies. Next, in **Figure 3E** a test of the proposed control algorithm is shown against a variation of 10% of the voltages of the electrical power grid v_s^{ϕ} and the load current i_L^a when the SAPF is off, which leads to an distorted source current. However, when the SAPF is activated, under the 10% of variation of the voltages of the electrical grid, the current of the electrical power grid i_s^a compensated, as show in **Figure 3E**.

Last, the analysis of the Total Harmonic Distortion (THD) of the electrical grid current under two non-linear load conditions has been carried out. **Figure 4A** shows the uncompensated (SAPF off) electrical power grid currents i_s^{ϕ}. **Figure 4B** shows the i_s^{ϕ} when en SAPF is on, where it can be appreciated the sinusoidal waveform. The same analysis has been performed R_L = 75 Ω as depicted in **Figure 4D,E**. In both cases, a considerable reduction of the THD has been obtained, that corresponds to 29.9–6.4%, and 27.37 to 6.8%, for a R_L = 100 Ω and R_L = 75 Ω, respectively.

CONCLUSION

This paper presented the real-time implementation of a model predictive current controller equipped with a modulation stage of a SAPF based on 7-level CHB converters, using SiC-MOSFET switching devices. The novel control scheme combines the concepts of model predictive control with the SV-PSPWM technique with the aim to reduce the computational burden. In addition, PI control is added to balance the DC-link voltages of the capacitors. The proposed control scheme has been validated experimentally. It has been shown that the proposed control can reduce 80% of THD caused by non-linear loads. Moreover, the robustness and effectiveness have been demonstrated under different operating points in both, in steady and transient conditions. Future works may include a comparative study of the proposed control schemes against classic control methods.

DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/Supplementary Material, further inquiries can be directed to the corresponding author.

AUTHOR CONTRIBUTIONS

AR conceived the idea for this paper. AR, JP and JR were responsible for the primary writing of the manuscript, while LC, MA and RG were responsible for revising the manuscript. All authors contributed to the article and approved the submitted version.

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