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EDITED BY
Tahir Khurshaid,
Yeungnam University, South Korea

REVIEWED BY
Liansheng Huang,
Hefei Institutes of Physical Science (CAS), China
Tohid Rahimi,
Carleton University, Canada

*CORRESPONDENCE
Jin Zhu,
zhujin@mail.iee.ac.cn

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A low-cost current flow controlling interline hybrid circuit breaker combined with SCR and H-bridge sub-module

Qingpeng Zeng[1,2], Jin Zhu[1]*, Xinming Guo[1,2], Qunhai Huo[1,2], Jingyuan Yin[1] and Tongzhen Wei[1,2]

[1]Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China, [2]University of Chinese Academy of Sciences, Beijing, China

A massive number of DC circuit breaker is usually necessary to be installed to protect HVDC grids from DC faults, this will lead to high capital costs because large number of expensive IGBT-in-series are used. In this paper, an interline hybrid circuit breaker is proposed by the combination of SCR string and a small number of H-bridge modules (SCR-IHCB). The proposed SCR-IHCB has the capacity of blocking DC fault of two adjacent lines respectively by sharing only one main breaker branch (MB) mainly composed of low-cost SCR string and H-bridge module instead of IGBT-in-series string. The interline current flow control function is also integrated. Hence it has advantages of simple and compact topology, economical design compared with typical IGBT based HCB solutions. The operation process of the proposed SCR-IHCB is discussed in detail, and the performance is verified by MATLAB Simulink simulation and scale-down prototype experiment.

KEYWORDS

hybrid circuit breaker, interline, SCR string, current flow control, H-bridge submodule

1 Introduction

Nowadays, HVDC grids have attracted significant attention, due to its inherent advantages such as flexible control of active and reactive power, low loss, system redundancy, and power reliability (Flourentzou et al., 2009; Akhmatov et al., 2014). While the HVDC grid offers several advantages, its engineering application still faces several challenges, one of which is the DC fault handling. The DC circuit breakers (DCCBs) is considered as an essential technology to isolate the fault area and maintain normal operations of non-fault areas in HVDC grids. There are three main groups of DCCB: mechanical DCCBs (Shi et al., 2015; Lin et al., 2016), solid-state DCCBs (Corzine and Ashton, 2012; Sano and Takasaki, 2014; Chang et al., 2016; Keshavarzi et al., 2017; Li et al., 2019; Wang et al., 2019; Shu et al., 2020; Zhang et al., 2020; Xu et al., 2021), and hybrid DCCBs(HÄFNER and JACOBSON, 2011; Sander et al., 2018). The hybrid DCCBs combine the merits of mechanical DCCBs and solid-state DCCBs and therefore is considered as an acceptable solution in HVDC grids. The classic hybrid DCCB

(HCB) topology contains a main breaker branch (MB), an energy absorption branch and a transfer branch, the transfer branch consists of an ultra-fast mechanical disconnector (UFD) in series with load current switch (LCS). There are two main groups of HCBs based on the different MB technical routes.

One of the technical routes is IGBT based MB, the classic IGBT-in-series based HCB has been proposed by ABB and successfully tested (HÄFNER and JACOBSON, 2011; Sander et al., 2018). The State Grid Corporation of China (SGCC) proposed a full-bridge modular based MB to avoid the problem of IGBT-in-series synchronization control and has been used in Zhangbei four-terminal MMC-HVDC (Jia et al., 2020; Jinkun et al., 2020.). In order to further reduce the system cost, some integration solutions are proposed, multi-line DC circuit breakers are integrated into one equipment to reduce the number of unidirectional MBs (Liu et al., 2017; Majumder et al., 2017; Mokhberdoran et al., 2018a; Kontos et al., 2018; Li and Wang, 2018; Xiao et al., 2020; Guo et al., 2021; Wang et al., 2022), another solution integrated HCBs and current flow controllers (CFCs) into one equipment is proposed in (Cwikowski et al., 2018; Mokhberdoran et al., 2018b; Zhu et al., 2022.) to reduce the system loss. But there are still some drawbacks to the hybrid DCCB topology as follows:

(1) Large number of series connected full-controlled semiconductors, such as IGBTs or IGCTs, in the main breaker increase the investment severely (Chen et al., 2018).
(2) In future, large DC grids fault currents may exceed the interruption capacity of IGBT under serious fault conditions. The parallel connection of IGBTs is needed but also introduces challenges in terms of construction cost (Dong et al., 2021).

Another technical route is SCR based MB, The SCR based MB has advantages of larger capacity, and lower price. Since the current conducted through the SCR need to reach a value below its threshold current during the turn-off process of SCR, apply a reverse voltage is one of the possible solutions to ensure fast transition from conducting to blocking. The most important issue when designing an SCR-based HCB is reliably to generate a reverse voltage on SCR during the turn-off process so as to make the current conducted through the SCR reach a value below its threshold current(Jamshidi Far and Jovcic, 2018).

Coupled inductors or Z-source schemes are used to generate the required reverse voltage on SCR during the turn-off process in (Ray et al., 2019). In those schemes, the transient fault current through capacitors is used to generate a reverse voltage on SCRs, hence those schemes can only be passively turned-off in the condition of the high current rising rate.

A thyristor full-bridge based HCB topology is proposed in (Guo et al., 2020), which can pre-charge the capacitor with DC system voltage, and the reverse voltage is generated by discharge process of pre-charged capacitor. The full-bridge structure is used to pre-charge the capacitor with dc system voltage and switch the fault current path, the use of large number of thyristor strings also increases the system cost.

A SCR-HCB with multiple branches is proposed by Alstom in (Grieshaber et al., 2015), the capacitance voltage difference of different branches is used to generate the required reverse voltage. The inductor is no longer needed, but if n branches are required for each HCB, 2n number of thyristor strings are required for two adjacent lines, which also increases the number of components in the whole DC grid system.

A DCCB topology combing many SCRs with a few IGBTs-in-series is proposed in (Shu et al., 2020). The required reverse voltage can be generated by controlled IGBT. However, each DCCB requires two additional IGBT strings, the utilization of the device needs to be increased in multi-terminal system.

In this paper, an interlink hybrid DC circuit breaker (IHCB) based on the concept of sharing only one SCR string MB between two lines is proposed (SCR-IHCB) to increase the utilization of the device. Only a few H-bridge submodule is embedded in to generate the required reverse voltage of SCR turn-off process, and the current flow controlling function is also integrated into the IHCB. No additional capacitor pre-charge circuits and inductors are required, the proposed solution can interrupt the short circuit current of two lines independently and control the current flow if necessary. Therefore, compared to the traditional DCCB/CFC schemes, the proposed topology is simple and economical.

2 Proposed topology

2.1 Basic structure of proposed SCR-IHCB

A novel IHCB is proposed in this paper and its detailed structure is shown in Figure 1. MB is composed of an anti-parallel SCR string and a H-bridge sub module, connecting line 12 and line 13. MOV_2 is used to protect IGBTs in H-bridge sub module. The transfer branch consisting of LCS and UFD is installed on each line. C_1 can be charged through T_1 to the limiting voltage of MOV_1 to block the fault current and absorb the residual energy of the system.

There are three modes of operation: normal operation without current flow controlling (bypass mode), normal operation with current flow controlling (CFC mode), fault current blocking mode. Obviously, higher system integration, lower volume and cost are achieved because only 1 MB mainly based on low-cost SCR string is used, and CFC function are integrated together.

2.2 Operation principles in different mode

2.2.1 Bypass mode

When the multiterminal HVDC (MT-HVDC) system is running normally, LCS_1/LCS_2 and UFD_1/UFD_2 are all

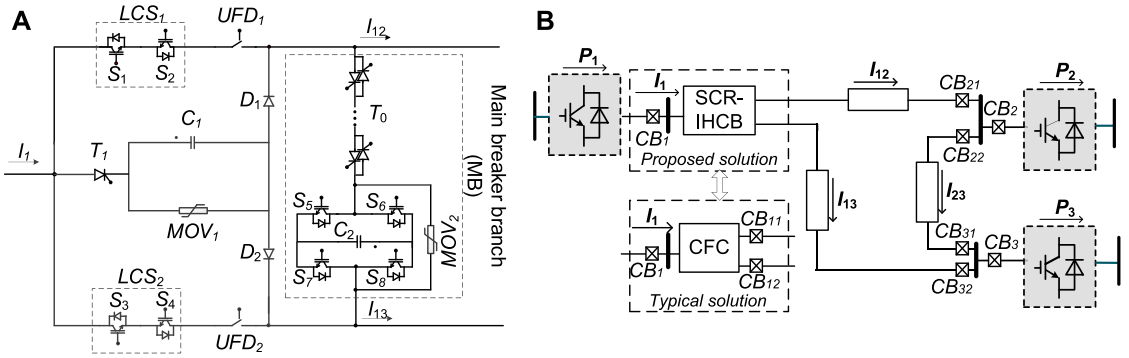

FIGURE 1
Proposed SCR-IHCB topology and installation position in system. **(A)** Proposed topology; **(B)** Three-terminal meshed HVDC system under study.

TABLE 1 Switching states for CFC mode.

State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_1	V_2	V_{C2}
Bypass Mode											
0	1	1	1	1	0	0	0	0	0	0	–
CFC Mode (I_{12} and I_{13} are going out the CFC and I_1 is entering)											
1	1	0	0	0	0	0	0	0	0	$-E$	↑
2	0	0	1	0	0	1	1	0	E	0	↓
3	1	0	0	0	1	0	0	1	0	E	↓
4	0	0	1	0	0	0	0	0	$-E$	0	↑
CFC Mode (I_{12} and I_{13} are entering the CFC and I_1 is going out)											
5	0	0	0	1	0	0	0	0	$-E$	0	↑
6	0	1	0	0	0	1	1	0	0	E	↓
7	0	0	0	1	1	0	0	1	E	0	↓
8	0	1	0	0	0	0	0	0	0	$-E$	↑

E is the reference value of voltage over C_2.

conducted, the SCR string (T_0) and H-bridge submodule are bypassed. There is no additional conduction loss and switching loss of semiconductor devices except LCS_1/LCS_2.

2.2.2 Current flow control mode

When the current flow needs to be adjusted, the proposed SCR-IHCB can work in CFC mode, the working principle is similar with other interline power flow controllers as shown in (Balasubramaniam et al., 2015; Sau-Bassols and Gomis-Bellmunt, 2017). The possible states concerning the available switches are summarized in Table 1.

Where "1" represents the switch is ON and "0" represents the switch is OFF. In Figure 2, one pair of states (state1 and state 2 in Table 1)f of current flow scenarios (I_{12} and I_{13} are going out the SCR-IHCB and I_1 is entering) are considered as an example. In order to transfer power from line13 to line 12, the CFC should switch continuously in state 1 and state 2 by alternating conduction of S_1 and S_3.

Below, the analytical analysis of the SCR-IHCB is performed for the pair of states (state 1 and state 2) presented before. Then, the analysis can be extended to the whole range of current configurations.

Taking state 1 as an example, capacitor C_2 is charged by I_{13}, which is equivalent to inserting a negative voltage in series with line 13. In state 2, capacitor C_2 is discharged by I_{12}, which is equivalent to inserting a positive voltage in series with line 12.

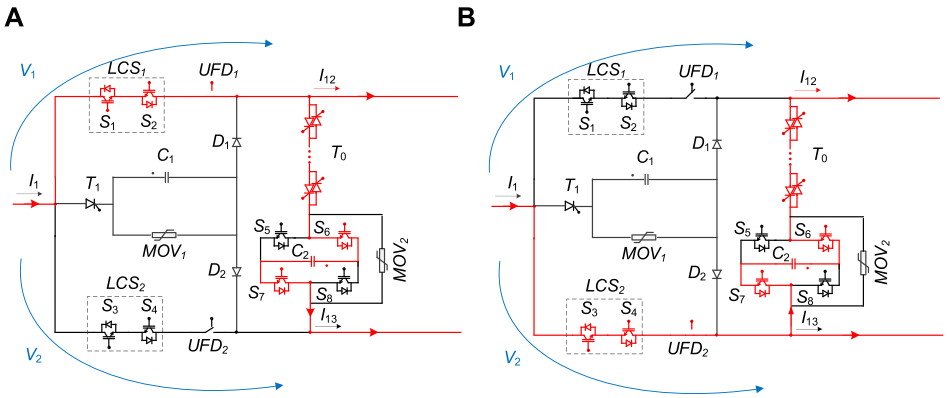

FIGURE 2
Operation stages of SCR-IHCB. **(A)** State 1; **(B)** State 2.

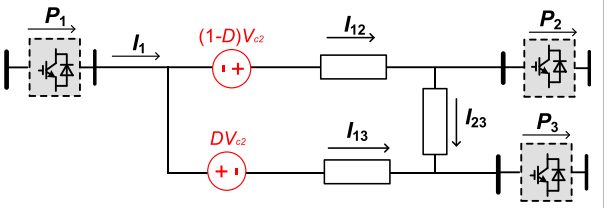

FIGURE 3
Average model of three-terminal DC grid with SCR-IHCB in current control mode.

Assuming D is the duty cycle of state 1. The average model of the three-terminal system with SCR-IHCB can be described as Figure 3.

2.2.3 Fault blocking mode

Take the DC short circuit fault of line12 when SCR-IHCB works in bypass mode as an example, the DC fault current blocking principle is given in Figure 4. Before the fault occurs, the load currents may flow through the low-loss transfer branches in bypass mode as shown in Figure 4A or in CFC mode such as shown in Figure 2.

Stage 1(t_1-t_3): If a fault occurs on line12 at t_1 and is detected at t_2, S_5, S_7 and T_0 will be switch on immediately, and then the IGBTs in LCS_1 will all be switched off at t_3, as shown in Figure 4B. The fault current is then commutated from transfer branch to the main breaker branches, and UFD_1 will open within 2 m.

Stage 2(t_3-t_5): With UFD_1 in open position at t_4 as shown in Figure 4C. Then S_7 switched off, and the S_8 will be switched on, thyristor T_1 will also be turned on immediately as shown in Figure 4D. Initially, T_0 still is on-state, capacitor voltage V_{c2} may suddenly increase in a short time, but its maximum value is strictly limited to the protection voltage V_{MOV2} by the parallel MOV_2, that will protect the IGBT S_5-S_8 from exceeding its maximum withstand voltage. Fault current will keep charging C_1 from zero-voltage state. The capacitor voltage V_{c1} gradually increases from zero but it is smaller than the capacitor voltage of V_{c2} which has been pre-charged in interline CFC mode, and a reverse voltage V_{T0} ($V_{T0} = V_{c1}(t) - V_{c2}$) will hereby be generated, the equivalent circuit is shown in Figure 5. The duration of reverse voltage should be larger than the requested recovery time, and the SCR string will be turn off reliably at t_5 as shown in Figure 4E.

Stage 3(t_5-t_7): The fault current continuously charges C_1. When V_{c1} reaches the protection voltage of MOV_1 at t_6, the current flowing through C_1 is transferred to MOV_1 as shown in Figure 4F. Until fault current decreases to value that no longer maintain D_1 conduction, the fault is cleared at t_7.

3 Parameters design and analysis

3.1 Analysis of current commutation

Based on the fault blocking mode described in Section 2, the process of current commutation starts when the IGBTs in LCS_1 are switched off at t_3. Prior to the capacitor C_1 is inserted at t_4, the fault current is fed into the fault node through healthy nodes, it means the current of other stations will inject into line12, the equivalent circuit is given in Figure 5A. Ignoring the resistance of the IGBTs and thyristor which are much less than line resistance, the fault current i_{fault} can be written as below:

$$i_{fault}(t) = i_{12}(t) + i_{13}(t) = \frac{V_1}{R_{12}}\left(1 - e^{\frac{-tR_{12}}{L_{12}}}\right) + \frac{V_3}{(R_{12}+R_{13})}\left[1 - e^{\frac{-t(R_{12}+R_{13})}{(L_{12}+L_{13})}}\right] \quad (t_1 \le t \le t_4) \tag{1}$$

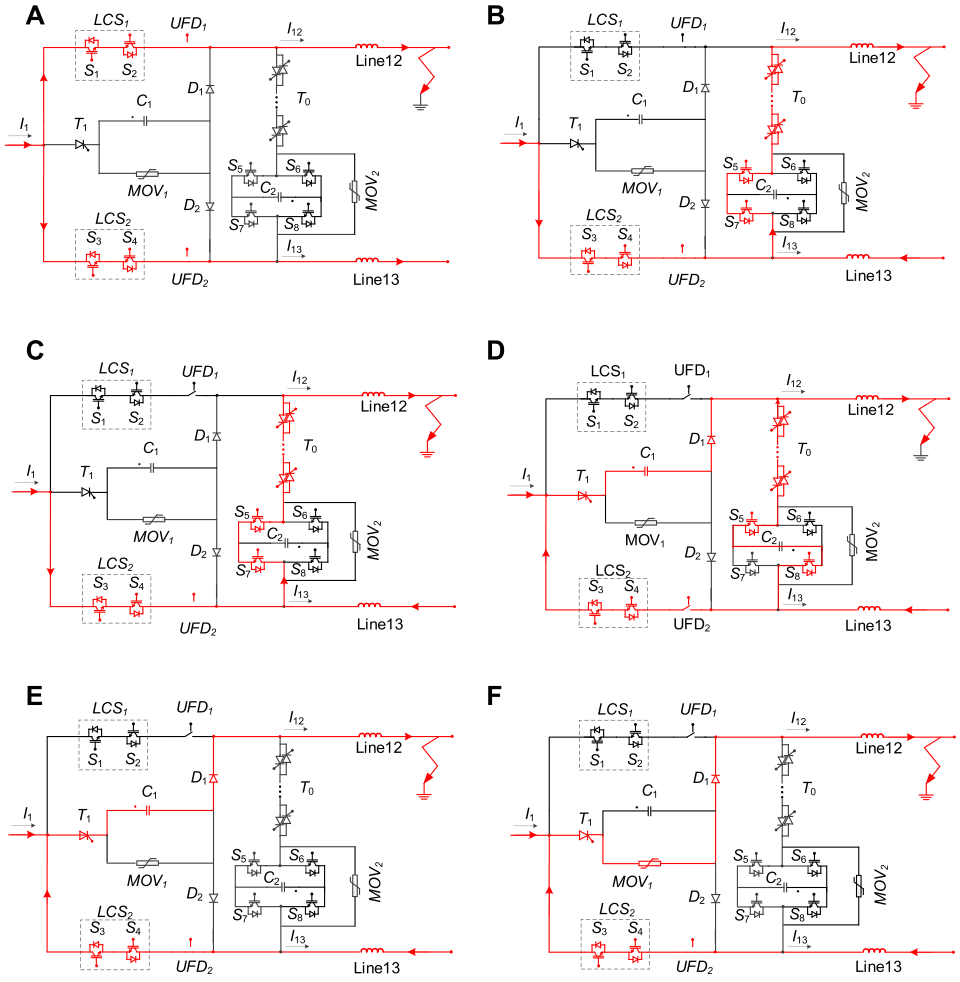

FIGURE 4
Operation of the SCR-IHCB for the transmission line fault. **(A)** Before t_2. **(B)** t_2-t_3. **(C)** t_3-t_4 **(D)** t_4-t_5 **(E)** t_5-t_6 **(F)** t_6-t_7.

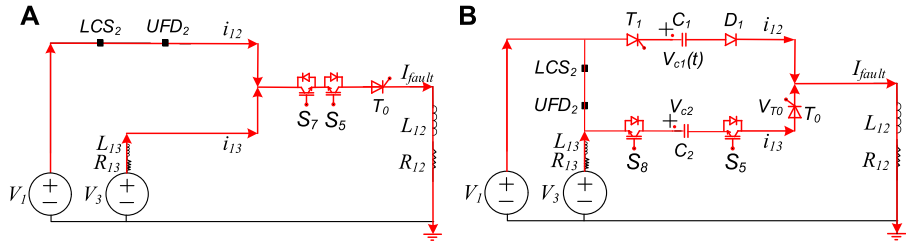

FIGURE 5
Implified equivalent circuit of current commutation process. **(A)** t_3-t_4 **(B)** t_4-t_5.

Where V_1 and V_3 are the voltage of station 1 and station 3 that assumed to remain constant value throughout the process, R_{12} and L_{12} is the resistance and inductance value of line12 to fault point, R_{13} and L_{13} is the resistance and inductance value of line13.

From t_4 to t_5, the capacitor C_1 and C_2 are inserted into the system, the simplified equivalent circuit can be seen in Figure 5B. For capacitor C_2, its voltage has a sudden increase in a short time and the maximum value is the clamping voltage of MOV_2. The

current i_{12} will charge the capacitor C_1 from zero until trigger the clamping voltage of MOV_1 at t_6. According to Figure 5B, the differential equations from t_4 to t_5 can be expressed as:

$$\begin{cases} L_{12}\dfrac{\mathrm{d}i_{12}}{\mathrm{d}t} + V_{\mathrm{c1}} = V_1 \\ i_{12} = \mathrm{C}_1\dfrac{\mathrm{d}u_{\mathrm{c_1}}}{\mathrm{d}t} \\ V_{\mathrm{c1}}(0) = 0 \\ V_{\mathrm{c2}} = V_{\mathrm{clamp2}} \\ i_{12}(0) = i_{12}(t_4) \end{cases} \tag{2}$$

where V_{clamp2} is the clamping voltage of MOV_2, the voltage of the capacitor C_1 from t_4 can be obtained:

$$V_{\mathrm{c1}}(t) = V_1 - V_1\cos\frac{1}{\sqrt{L_{12}C_1}}t + \sqrt{\frac{L_{12}}{C_1}}i_{12}(t_4)\sin\frac{1}{\sqrt{L_{12}C_1}}t \quad (t_4 \le t \le t_5) \tag{3}$$

Assuming T_{scr} is the minimum recovery time of SCR string, the SCR voltage V_{T0} can be expressed as:

$$V_{T0} = V_{\mathrm{c1}}(t) - V_{\mathrm{c2}} = V_1 - V_1\cos\frac{1}{\sqrt{L_{12}C_1}}t + \sqrt{\frac{L_{12}}{C_1}}i_{12}(t_4)\sin\frac{1}{\sqrt{L_{12}C_1}}t - V_{clamp2} \le 0\,(t_4 \le t \le t_4 + T_{scr}) \tag{4}$$

The most important issue of parameter design of the proposed topology is to make sure that the duration of reverse voltage on the SCR string T_0 must be larger than the minimum requested recovery time to make sure the current conducted thought the SCR reach a value below its threshold current and last long enough, thus the thyristor can be switched off reliably.

To meet the minimum recovery time of SCR under the worst situation, and the calculation process can be simplified:

$$T_{rv} = \frac{C_1 V_{C2}}{I_{\max}} \ge \alpha T_{scr} \tag{5}$$

The capacitor C_1 and voltage of C_2 can be chosen as:

$$\begin{cases} C_1 \ge \dfrac{\alpha T_{scr} I_{\max}}{V_{C2}} \\ V_{C2} \ge \dfrac{\alpha T_{scr} I_{\max}}{C_1} \end{cases} \tag{6}$$

Where T_{rv} is the required reverse voltage time, T_{scr} is the minimum recovery time of T_0. I_{max} is the maximum allowed breaking current of SCR-IHCB. α is a redundancy factor and must be larger than 1.

According to Eqs. 5, 6, a larger redundancy factor α increases the reliability of SCR-IHCB, but the capacitor value C_1 and V_{c2} becomes larger. A redundancy factor of 1.5~2 is generally preferred. When the value of α is determined, the value of C_1 and V_{C2} should be designed together, A smaller value of C_1 means a faster blocking speed (t_b in Figure 6) of the fault current because V_{c1} can rise to V_{DC} faster, but it also means that a higher V_{C2} value is required; a higher V_{c2} value also means higher withstand voltage of S_5-S_7, IGBT-in-series or cascaded multi submodule topology can be used, but the cost and loss of the system will also increase. There exists a trade-off between system economy and fault current blocking speed, as shown in Figure 6.

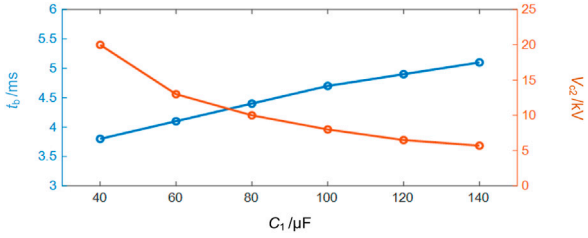

FIGURE 6
The relationship between C_1, t_b and V_{c2}.

3.2 Parameters calculation of MOV

The rated voltage for the MOVs of the typical HCB should be greater than 1.5 times the system voltage to quickly reduce the fault current to zero:

$$V_{MOV} \ge 1.5V_{DC} \tag{7}$$

The total absorbing energy E_{MOV} of MOV is associated with the energy storage components of system, which can be given by:

$$E_{MOV} = \frac{1}{2}L_{DC}I_{\max}^2 - \frac{1}{2}C_1\left(V_{mov}^2 - V_{DC}^2\right) \tag{8}$$

where L_{DC} is the value of system equivalent inductance, I_{max} is the maximum value of fault current.

3.3 Device cost and loss analysis

In order to compare the improvements of the proposed SCR-IHCB, it is compared with the typical HCB+CFC solution which is not integrated (three ABB's HCB solution (Häfner and Jacobson, 2011) in three lines with one CFC (Sau-Bassols and Gomis-Bellmunt, 2017)) in 10kV/1 kA three-port system, as shown in Figure 7. 4.5 kV IGBT(5SNA1200G452300) and 5.2 kV thyristor(T1451N) are selected in the comparison. The relative conduction loss and device cost of two solutions in the same voltage level are shown in Figure 8, where the ordinate is a relative value and "1" represents the maximum.

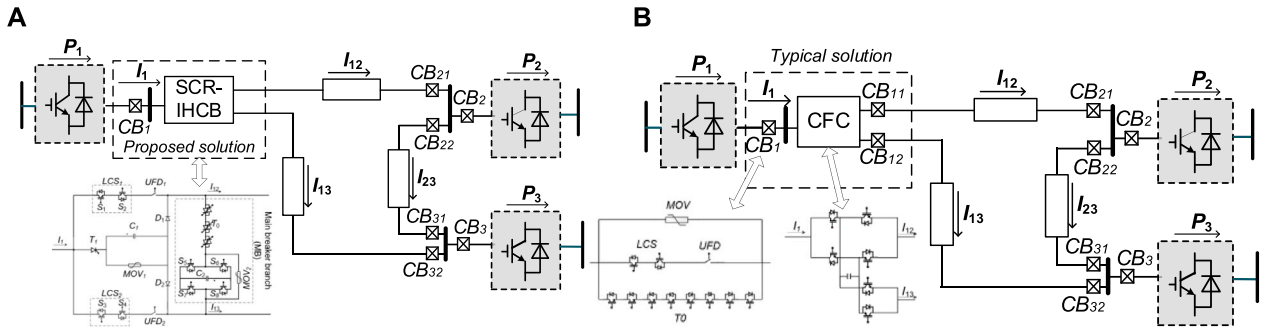

FIGURE 7
Detailed topologies of two solutions in 10kV/1 kA three-port system **(A)** Proposed SCR-IHCB; **(B)** Typical HCB+CFC solution.

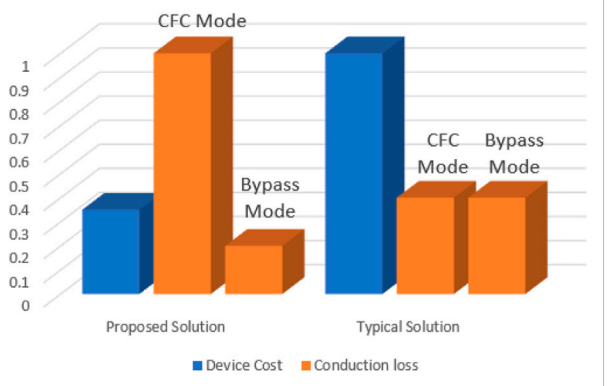

FIGURE 8
Economic comparison with two solutions in 10 kV three-port system.

As can be seen in Figure 8, the device cost of the proposed solution is much lower than that of typical HCB+CFC solution, because less HCBs are used and large number of fully-controlled semiconductor devices have been replaced by semi-controlled semiconductor devices.

The conduction loss in the proposed SCR-IHCB is much higher in CFC mode, but is lower in bypass mode compared with typical IGBT based HCB + CFC solution. Because in bypass mode, only the conduction loss of LCS is added with the proposed solution, but both conduction loss of IGBTs in LCS and CFC parts are added with the typical solution. Considering the investment and conduction loss in different mode together, the comprehensive cost during operation strongly depends on how often the SCR-IHCB need to operate in CFC mode to ensure stable grid conditions, therefore the comprehensive cost could be much lower than the typical solution in the application scenario where inter line power flow control is only needed occasionally.

4 Modeling and control methodology of CFC

In this section, the dynamic model of the proposed CFC is presented, using averaging technique where the terminals voltages are taken into consideration as setting values. Taking the first scenario for example, and the analysis can be extended to the rest of possible current configurations. We can see the current flow of the first scenario in the Figure 2.

The following set of equations describes the circuit of Figure 2A. This equivalent circuit was developed based on a reduction of the physical circuit layout, where: r_{xx} and L_{xx} are the resistance and the inductance of the line xx originated from the CFC bus and carrying an instantaneous current i_x, V_{c1} is the capacitor voltage, V_1 is the voltage at the bus where the CFC is connected to, V_2 and V_3 are the voltages at the end terminals of the lines, respectively.

$$\begin{bmatrix} L_{12} & 0 & 0 \\ 0 & L_{13} & 0 \\ 0 & 0 & C_1 \end{bmatrix} \dot{X} = \begin{bmatrix} -r_{12} & 0 & 0 \\ 0 & -r_{13} & -1 \\ 0 & 1 & 0 \end{bmatrix} X + \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix} U \quad (9)$$

$$X = \begin{bmatrix} i_{12} \\ i_{13} \\ V_{c1} \end{bmatrix}, \; U = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \quad (10)$$

Similarly, the state equations of Figure 2B, where the capacitor is discharging into line12, are as follows:

$$\begin{bmatrix} L_{12} & 0 & 0 \\ 0 & L_{13} & 0 \\ 0 & 0 & C \end{bmatrix} \dot{X} = \begin{bmatrix} -r_{12} & 0 & -1 \\ 0 & -r_{13} & 0 \\ -1 & 0 & 0 \end{bmatrix} X + \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix} U \quad (11)$$

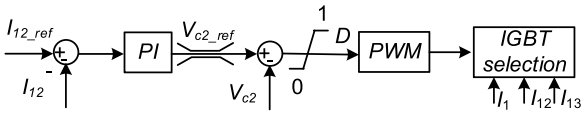

FIGURE 9
PI controller for CFC mode of SCR-IHCB.

Assume the duty ratio of the charging mode1 is D. Multiplying Eqs. 8, 10 by D and $(1–D)$, respectively, and adding the results to obtain the average model for the CFC for the scenario as follows:

$$\begin{bmatrix} L_{12} & 0 & 0 \\ 0 & L_{13} & 0 \\ 0 & 0 & C_1 \end{bmatrix} \dot{X} = \begin{bmatrix} -r_{12} & 0 & -1+D \\ 0 & -r_{13} & -D \\ -1+D & D & 0 \end{bmatrix} X + \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix} U \tag{12}$$

At steady state, Eq. 11 can be written as Eq. 12:

$$\begin{bmatrix} -r_{12} & 0 & -1+D \\ 0 & -r_{13} & -D \\ -1+D & D & 0 \end{bmatrix} X + \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix} U = 0 \tag{13}$$

Solving Eq. 12, the steady-state value of capacitor voltage is obtained as:

$$V_c = \frac{(V_1 - V_2) - r_{12} i_{12}}{1 - D} = \frac{(V_1 - V_3) - r_{12} i_{12}}{D} \tag{14}$$

Eq. 13 gives an expression for the capacitor voltage as a function of the network parameters and the voltage drops across the cables connected to the CFC which represents the loading condition of the grid.

Given that the power taken from one line is equal to the power added to the other line, the power balancing between state 1 and state 2 as shown in Figure 2 is given by:

$$V_{c2\_ref}(1 - D) I_{12} - V_{c2\_ref} D I_{13} = 0 \tag{15}$$

The relationship between I_{12} and I_{13} can be obtained from the above formula:

$$\frac{I_{12}}{I_{13}} = \frac{D}{1 - D} \tag{16}$$

From the previous analysis the voltage ripple can be deduced and it is given by Eq. 16.

$$\Delta U = \frac{D I_{13}}{C_2 f} = \frac{(1 - D) I_{12}}{C_2 f} \tag{17}$$

where f is the switching frequency of the CFC.

A block diagram for the control scheme is shown in Figure 9. The control system has two nested PI controllers: an inner capacitor voltage controller and outer DC current controller. The outer controller regulates the DC line current by feeding a reference voltage to the inner voltage controller. The inner controller achieves the required capacitor voltage level by controlling the duty cycle.

TABLE 2 Parameter of three-terminal HVDC system.

Line parameter	R (Ω Ω/km)	0.01105
	L(MH/km)	3.245
	C(μF/km)	0.382
Station	Length/km	
A1 to A2	200	
A1 to A3	300	
A2 to A3	200	
Converter Parameter	AC voltage	110 kV
	DC voltage	200 kV
	Limiting current inductor	100 mH
SCR-IHCB Parameter	Capacitor C_1	120 μF
	Capacitor C_2	1mF/6 kV
	Arrester protective voltage	250 kV

5 MTDC network Simulation Studies

In this section, a simplified three-terminal HVDC system is simulated. As shown in Figure 1, the proposed SCR-IHCB topology is equipped at station 1 to adjust the power of line 12 and line 13. The practical parameter of the three-terminal HVDC system is shown in Table 2.

The currents flowing from the DC bus of station 1 and the transmission lines in presence of the SCR-IHCB are depicted in Figure 10. The SCR-IHCB operates in the bypass mode for $0 < t <$ 2s. Thereafter, the CFC changes its operation mode to CFC mode at 2s. Figures 10A, B implies that the SCR-IHCB can adjust the current bidirectionally in CFC mode. The short-circuit fault in line12 happens at time $t = 4$s. It can be seen in Figures 10A, B that the SCR-IHCB can quickly isolate the fault on line 12, and the transmission between station 1 and station 3 returned to normal ($I_1 = I_{13}$).

As shown in Figure 10C, before the fault is detected in $t = 4.001$s, the SCR-IHCB is still working in CFC mode. when the system detects the fault, IHCB mode is activated, S_5 and S_7 conducts as mentioned above, the fault current goes through T_0, and I_{T0} started to rise rapidly. After 2 m (waiting for the UFD_1 completely open), the fault current was successfully transferred to charging path of the capacitor C_1, V_{c1} starts to rise (as shown in Figure 10E), in less than

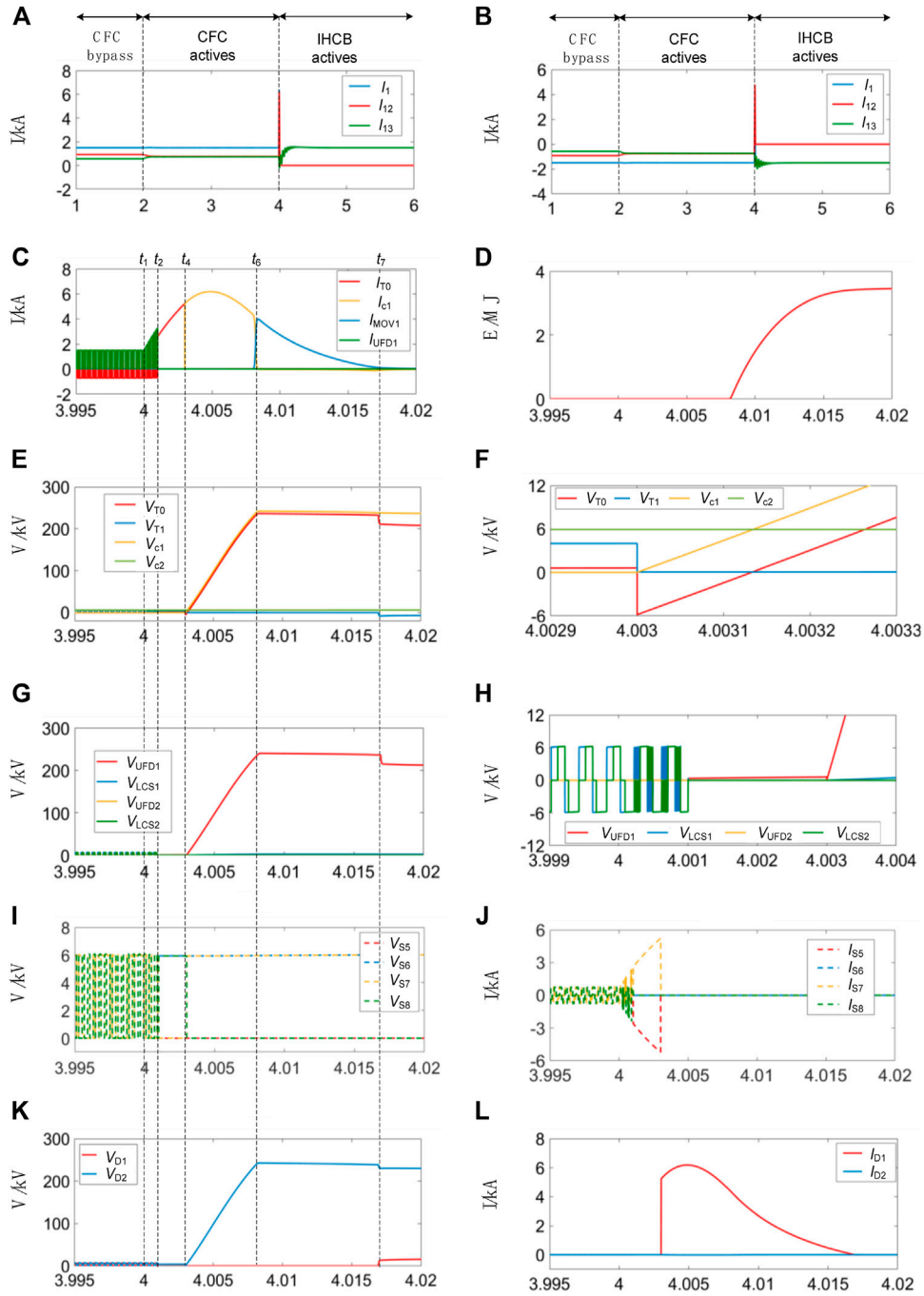

FIGURE 10
Performance of SCR-IHCB. **(A)** Current waveforms with forward power flow. **(B)** Reverse power flow. **(C)** Fault current transfer process. **(D)** Energy absorb by MOV_1. **(E)** V_{T0}, V_{T1}, V_{c1} and V_{c2}. **(F)** Details of V_{T0}, V_{T1}, V_{c1} and V_{c2}. **(G)** Voltage of transfer branches. **(H)** Details of voltage of transfer branches. **(I)** V_{S5}-V_{S8}. **(J)** I_{S5}-I_{S8}. **(K)** V_{D1} and V_{D2}. **(L)** I_{D1} and I_{D2}.

5 m, the fault current (I_{c1}, I_{D1}) reaches the peak value 6.1 kA. When V_{c1} reaches the protection voltage of MOV_1(250 kV as shown in Figure 10E), the fault current is transferred to MOV path (I_{mov1} in Figure 10C) and decreases to zero. The amount of absorbed energy of MOV_1 reaches almost 3.6 MJ as shown in Figure 10D. When the fault current drops to zero, the value of V_{T0} return to V_{DC}-V_{c2}, and the thyristor T_1 needs to withstand a reverse voltage of V_{c1}-V_{DC}, about 50 kV as shown in Figure 10E.

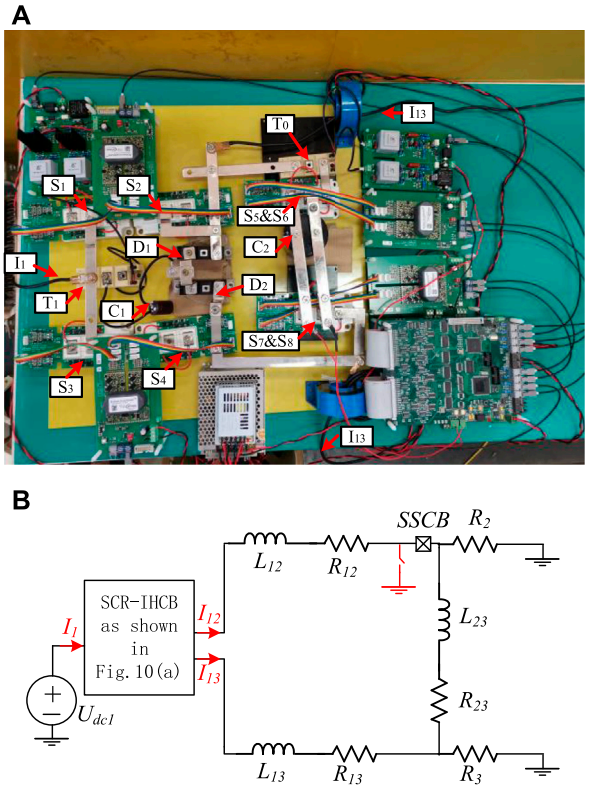

FIGURE 11
Experimental system. **(A)** Photograph of the scale down SCR-IHCB prototype. **(B)** Circuit diagram of three-terminal test platform.

TABLE 3 Parameters of the experimental system.

Parameter	Value
U_{dc1}	200V
$L_{12}/L_{13}/L_{23}$	6mH/6mH/6 mH
R_{12}	6Ω
R_{13}	1.2Ω
R_{23}	4.8Ω
R_2	18.6Ω
R_3	18.6Ω
V_{c2_ref}	30V

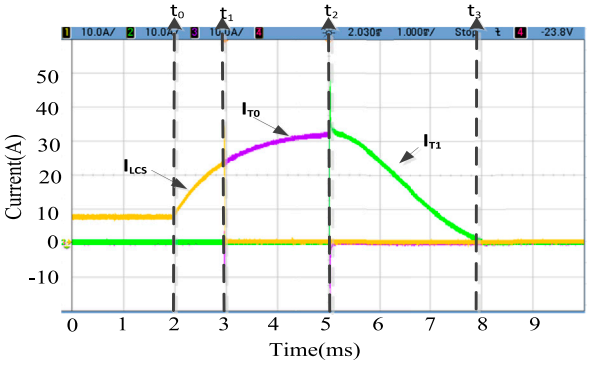

FIGURE 12
Measured fault-interrupting waveforms of the DC Fault Mode.

Figure 10F shows that the reverse voltage V_{T0} ($V_{T0} = V_{c1} - V_{c2}$) is generated at 4.003s, and the duration time is about 140us, much larger than the minimum requested recovery time of SCR string in (Jamshidi Far and Jovcic, 2018).

Figures 10G, H show the voltage waveform of two transfer branch, LCS_1 and LCS_2 works in CFC mode before fault is detected. UFD_2 and LCS_2 remain on-state to keep transmission of station1 and station 3 after fault blocking, LCS_1 switch off at 4.001s, and the UFD_1 takes 2 m to completely open, then the voltage on UFD_1 increases with V_{c1}.

Figures 10I, J show the voltage and current of the S_5-S_7. Obviously, the operation sequence of S_5-S_8 is consistent with the theoretical analysis, and the maximum withstand voltage of S_5-S_8 is limited to the given voltage of V_{c2}, the maximum current is equal to the value when the fault current transferred from T_0 branch to C_1 branch.

Figures 10K, L show that the maximum withstand voltage and current of diode strings (D_1 and D_2) are consistent with the maximum voltage of V_{c1} and maximum fault current.

6 Experimental Studies

Considering that the proposed SCR-IHCB topology is a symmetrical structure for fault blocking of two adjacent lines; therefore, the verification for the current opening process of one line is enough. A scale-down prototype is built for verifying the concept of the feasibility of the SCR-IHCB, as shown in Figure 11A, the component marks in Figure 11A are consistent with those in Figure 1A. The diagram of the experimental system is depicted in Figure 11B and the system parameters are listed in Table 3.

6.1 Fault current blocking

The fault blocking waveforms of the SCR-IHCB are shown in Figure 12. It can be seen that after the fault occurs at t_0, after a detection time of 1 m, the IGBT in LCS is turned OFF, fault current is transferred to main breaker branch at t_1. A 2 m delay is

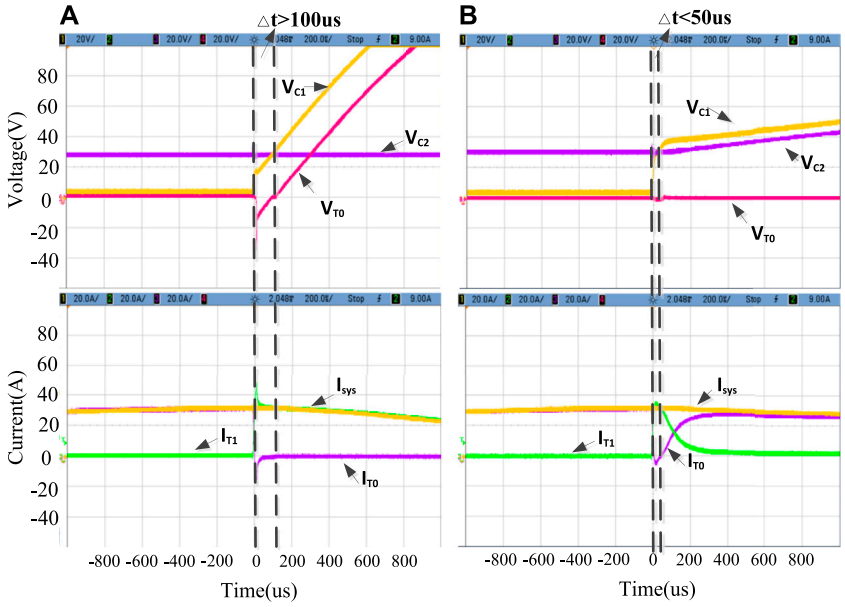

FIGURE 13
Measured waveforms during the thyristor recovery stage at **(A)** C_2 = 220μF; **(B)** C_2 = 100 μF.

set between t_1 and t_2 to simulate the opening time of mechanical switch. The IGBTs in main breaker branch is turned off at t_2, while C_1 is charged and the fault current is successfully interrupted eventually at t_3.

The detailed waveforms of the thyristor T_0 recovery stage is shown in Figure 13. When the value of 220 μF is chosen for C_2, the SCR-IHCB has Δt > 100us as shown in Figure 13A, and the thyristor is turned off successfully, the fault current of the system (I_{sys}) is quickly transferred from T_0 to T_1 (I_{T0} and I_{T1} in Figure 13A), the voltage of T_0 (V_{T0}) rises as C_1 is charged by the system fault current.

When the value of C_2 is reduced to 100 μF, the SCR-IHCB has Δt < 50us, smaller than t_q in datasheet of thyristor SKKT62 which is used in our experiment. It is obvious that the thyristor has failed to turn off, the fault current of the system (I_{sys}) continues to flow through T_0, Capacitor C_1 and capacitor C_2 are connected in parallel, and the voltage rises synchronously.

6.2 Current control

The CFC function is also verified by experiments, as shown in Figure 14. At the beginning, the current at line 12 (I_{12}) is 12A and at line 13 (I_{13}) is 6A at first. At t = 10 m, the CFC begins to work and the current at line 13 (I_{13}) begins to increase and the current at line 12 (I_{12}) decreases meanwhile. After 5 m, the line current forms a new steady state. It can be found that the controller can keep capacitor voltage constant at 30V (V_{c2}) during current regulation.

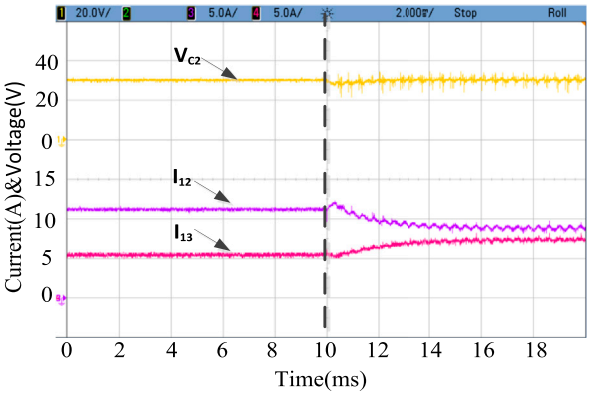

FIGURE 14
Measured fault-interrupting waveforms of the current control mode.

7 Conclusion

In this paper, a SCR string and H-bridge module based interline hybrid circuit breaker topology with current flow control function is proposed. The operation principles in normal operation mode and DC fault mode are analyzed, the parameters design principle is also presented in detail. The simulation and experiment results from a meshed HVDC grid model confirm the operational performance of the proposed topology. Compared with other solutions, the topology design is more economical and simpler because only one bidirectional

SCR string and only one H-bridge module is needed for two adjacent lines, no additional capacitor pre-charge circuits and inductors are required, the current flow control function is also integrated without additional components.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material; further inquiries can be directed to the corresponding author.

Author contributions

QZ: Writing—Original Draft, Experimental Studies and Visualization. JZ: Conceptualization, Methodology and Supervision. XG: Writing—Original Draft and Simulation Studies. QH: Editing, Parameters Design. JY: Process Analysis, Supervision. TW: Supervision.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

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