



Investigating Variable Speed Wind Turbine Transient Performance Considering Different Inverter Schemes and SDBR

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In wind energy applications, voltage source converters are employed to achieve energy conservation. Recently, multilevel converters have been showing promising advantages compared to the traditional 2-level converter scheme, due to the fact that they can overcome certain limitations during transient conditions. This paper investigates the transient performance of variable DFIG-based speed wind turbines taking into account different scheme configurations of the power converter system. The schemes investigated are a 2-level six step IGBT inverter, a parallel interleaved 2-level six step IGBT inverter, and a 3-level IGBT inverter. All schemes were compared during severe three-phase to ground fault at the terminal of the DFIG wind turbine using the conventional Phase Lock Loop (PLL) and a DC-chopper protection. A coordinated approach of improving the performance of all the converter schemes with series dynamic braking resistor (SDBR) was analyzed. Investigation of the best location for the SDBR in the DFIG architecture considering the best switching signal was also carried out. Furthermore, a new control strategy of PLL for the DFIG system was proposed in conjunction with the SDBR scheme for the converter systems. Simulations were carried out in Power System Computer Aided Design and Electromagnetic Transient Including DC (PSCAD/EMTDC). The results show that the proposed PLL and SDBR hybrid scheme in the various inverter topologies considered in the study can enhance the performance of the wind generator variables during severe three-phase to ground fault. This is because the proposed hybrid scheme could help to boost the capability of the current and recovery of the wind generator after post-fault scenarios. Also, the voltage source converter leg switched output voltage would be enhanced to maximum change in common mode voltage by the inverter schemes' modulation of the space vector using the proposed strategy.

Keywords: index terms-doubly fed induction generator, series dynamic braking resistor, wind energy, power converters, stability, protection schemes

INTRODUCTION

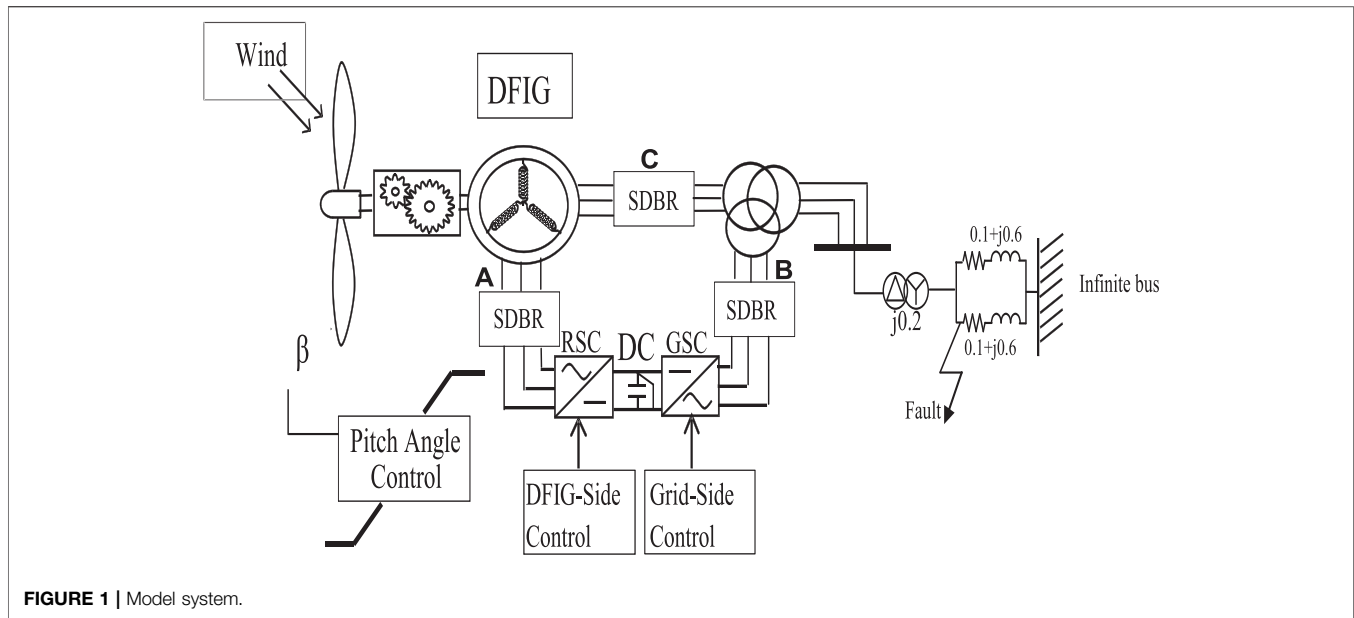
The use of Insulated Gate Bipolar Transistors (IGBTs) has been increasing lately for high power applications among semiconductor devices. This is because the current capability of the IGBT switches can be increased by configuring them in a parallel connection (Gohil et al., 2015). Because the IGBT switches are high power and are subjected to high voltage and current, their transient operations during periods of several microseconds are vital (Okedu, 2013; Wang et al., 2013). Therefore, the ability for variable speed IGBT-based wind turbines to withstand abnormal conditions is necessary to achieve the lifetime specifications (Ohi et al., 2002; Volke and Hornkamp, 2012) of the wind turbine and at the same time fulfill the requirement of grid codes.

In wind energy applications, the Doubly Fed Induction Generator (DFIG) has one main merit of utilizing only 20–30% of the wind generator rating for the power converters linking the rotor side and the grid side (Xu and Cartwright, 2006; Okedu, 2020). In addition, this wind turbine technology has low power loss, cost effective power converters, four quadrants of power regulation for active and reactive power, and an improved mechanism for wind energy capture in comparison with the earlier technology of fixed speed induction generators (Djeriri et al., 2013). All these features mean this type of wind turbine is widely employed in wind energy conversion systems. However, this wind turbine technology has two fragile back-to-back power converters that are vulnerable to damage when operating under a severe three line to ground fault. Consequently, these power converters need to be protected to avoid damage and also to fulfil the grid requirements, by controlling frequency and voltage via its rotor circuit. Basically, this AC three phase voltage can be controlled using various switching techniques ranging from six step switching (Murphy and Turnbull, 1988), Pulse Width Modulation (PWM) (Muller et al., 2002), and space PWM (Mohan, 2005). In traditional wind generators based on DFIG, the power converters are connected back-to-back and this topology is limited in its applications regarding high power. Therefore, if converters based on multilevel topology are employed, this drawback could be overcome. Consequently, in wind energy generation applications, the multilevel converters are gaining popularity (Nabae et al., 1981; Stemmler and Geggenbach, 1993). This is because this type of converter topology for wind turbines has higher power ratings than the power converter structure, leading to less impact on the switches of the IGBTs. Hence the low harmonic contents with improved voltage waveforms would be achieved considering this type of converter strategy.

The Neutral Point Clamped (NPC) converter (Bansal et al., 2003) is one of the most popular structures in the multilevel voltage source inverter proposed in the literature. However, a lot of reports on the control of converter currents have been proposed in recent years. In (Brod and Novotny, 1985; Nagy, 1994; Kazmierkoski and Malesani, 1998), various current controller classifications of the power converter system were reported, of which some have been developed, ranging from hysteresis and linear proportional integral to predictive dead-beat

(Buso et al., 1998; Ghennam et al., 2013). The hysteresis current controller is mainly used because it is simple and does not require any knowledge of the load with an advantage of a fast dynamic response (Salama and Lennon, 1991; Nagay et al., 1996; Kwon et al., 1998). The major disadvantages of this conventional controller are the limit cycle oscillations, switching at a random rate, and interaction of phase currents (Ueda et al., 1995; Baiju et al., 2002; Tekwani et al., 2005). The application of a three level NPC voltage source converter for DFIG and a vector hysteresis current control were reported in (Djeriri et al., 2013; Ghennam et al., 2013) respectively for effective power control of the variable speed wind turbines. References (Ueda et al., 1995; Asiminoaci et al., 2008; Zhang et al., 2010; Gohil et al., 2015) reported that when the carrier signals of a voltage source converter connected in a parallel configuration was interleaved, enhanced waveforms of the effective voltage in high power applications could be achieved, despite the harmonic quality present. An evaluation of the reliability and effectiveness of the IGBT switches considering short circuit faults was analyzed in (Ma et al., 2015; Reigosa et al., 2015), respectively. A comparative study of power quality improvement for the DFIG system by subjecting the wind generator to various types of rotor converters was presented in (Nashed and Eskander, 2012). It was reported that in the two-level six-step IGBT inverter schemes, the harmonic contents are very high because frequency of switching the switches is low. Consequently, the inverter performance is reduced. The production of high harmonic contents in the conventional two-level DFIG system because of low switching frequency reduces the performance of the variable speed wind turbine system. Therefore, interleaving the converters in a parallel configuration could help improve the wind generator performance.

As the use of multilevel converters is becoming popular in wind energy conversion systems, because of their robustness during transient conditions, this paper aims to improve the performance of the six-step 2-level IGBT inverter by proposing a coordinated control of the inverter system with a new Phase Lock Loop (PLL) configuration together with a Series Dynamic Braking Resistor (SDBR). The high voltage usually experienced during grid disturbances is shared by the small, inserted resistance because of the series connection strategy of employing the braking resistor. Thus, the loss of the converter control system is not experienced in this topology due to induced overvoltage. In addition, the series connected braking resistor strategy significantly reduces the very high current in the rotor circuitry of the wind generator to lower values. Consequently, the overvoltage of the DC-link that was supposed to be dangerous to the power converters of the wind generator are avoided because of the low DC-link capacitor charging current (Okedu and Muyeen, 2011; Okedu et al., 2012; Okedu, 2019). Although many studies in the literature considered the use of fault current limiters for enhancing power quality and limiting fault currents of DFIG wind turbines in wind farms (Chen et al., 2015; Rashid and Ali, 2016; Firouzi and Gharehpetian, 2018), in this paper, the preferred position of the braking resistor in the wind generator system was analyzed considering different switching signals. The optimal braking resistor position and switching



strategy were used for further analysis of the proposed wind generator schemes used in this study. In addition, a comparative study using the proposed scheme for the 2-level IGBT inverter was carried out with the schemes having a parallel interleaved IGBT inverter and 3-level IGBT inverter. Simulations were run in PSCAD/EMTDC (PSCAD/EMTDC Manual, 1994). The proposed hybrid scheme could help to increase the current capability and post-fault recovery of the wind turbine. In addition, the space vector modulation of the inverter schemes resulted in maximum value change in common mode voltage, using the proposed hybrid control strategy of the PLL and SDBR scheme. Consequently, there is improved switched output voltage of the converter leg of the voltage source converter. The results show that the hybrid scheme in the various inverter topologies considered in the study can enhance the performance of the wind generator variables during severe three-phase to ground fault.

MODEL SYSTEM OF STUDY

The model system of the study is shown in **Figure 1**. The wind turbine is modeled using **Eqs 1–6**. The wind generator consists of a rotor, also known as the prime mover, a gearbox system, and a shaft. The wind generator's torque, which is aerodynamic in nature, and the mechanical power are expressed by (Okedu et al., 2012; Justo et al., 2015):

$$T_M = 0.5\rho C_t(\lambda)\pi R^3 V_w^2 [\text{NM}] \quad (1)$$

$$P_{wt} = 0.5\rho C_p(\lambda, \beta)\pi R^2 V_w^3 [\text{W}] \quad (2)$$

Where ρ is the air density, R is the radius of the turbine, V_w is the wind speed, and $C_p(\lambda, \beta)$ is the power coefficient given by

$$C_p(\lambda, \beta) = 0.5(\Gamma - 0.02\beta^2 - 5.6)e^{-0.17\Gamma} \quad (3)$$

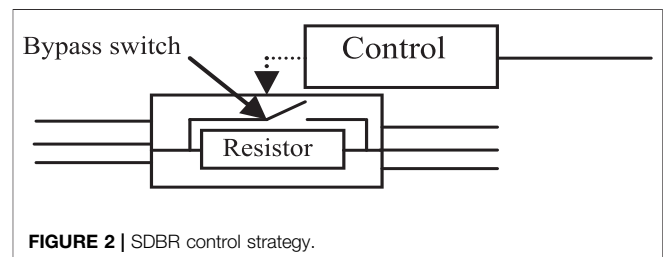
C_t and C_p are related by

$$C_t(\lambda) = \frac{C_p(\lambda)}{\lambda} \quad (4)$$

$$\lambda = \frac{\omega_{wt} R}{V_w} \quad (5)$$

$$\Gamma = \frac{R(3600)}{\lambda(1609)} \quad (6)$$

The rotational speed [rad/s] of the wind turbine is ω_{wt} , the tip speed ratio is λ , and C_p is the power coefficient. In **Figure 1**, the rotor side (A), the grid side (B), and the stator side (C) of the wind generator show the insertion of the proposed braking resistor scheme in series connection, respectively. A three-phase to ground fault was used to investigate the optimal position of the braking resistor considering the model system of study in **Figure 1** that is connected to an infinite bus. **Figure 2** shows the various control signals: DC-link voltage, current of the rotor for the wind generator, and terminal voltage of the grid, along with the conditions of operation of the braking resistor. The optimal position and switching strategy of the braking resistor in the wind generator was used for further analysis of the inverter schemes proposed in this paper.



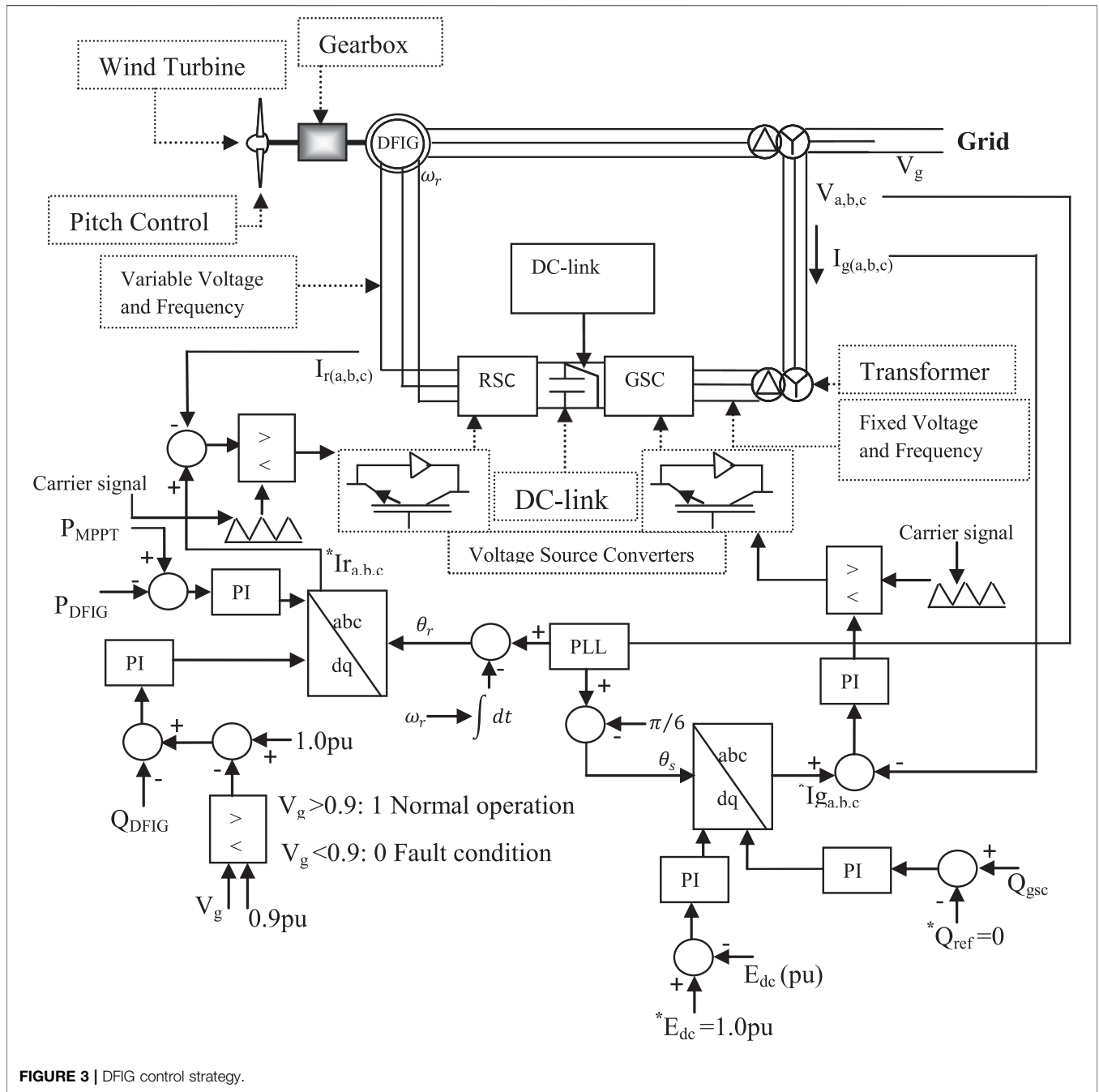


FIGURE 3 | DFIG control strategy.

VARIABLE SPEED DRIVE CONTROL

Figure 3 shows the control strategy of the DFIG-based variable speed wind turbine. The cost of the crowbar protection scheme used in a conventional DFIG system is more than the other schemes, such as the braking resistor or DC chopper. During grid fault, the crowbar makes the DFIG-based variable speed wind generator act like a fixed speed wind generator. This is done by disconnecting the wind generator’s rotor side converter. In this paper, the DC-link (chopper) scheme is the alternative employed in place of the traditional crowbar switch, as shown in

Figure 3. The coordinated controls of the active and reactive power of the DFIG system via abc to dq and dq to abc conversion to generate pulses for the switching of the PWM are shown in Figure 3.

The new PLL control strategy used in this study has a delay element incorporated to improve the performance of the DFIG system. The PLL scheme is designed based on a frequency of 50 Hz and rated a line-to-line voltage of 0.69 kV. Unlike the conventional PLL scheme, the proposed PLL scheme in this work links the Sine and Cosine function angles for the three phases via a multiplier before the insertion of a delay element in order to

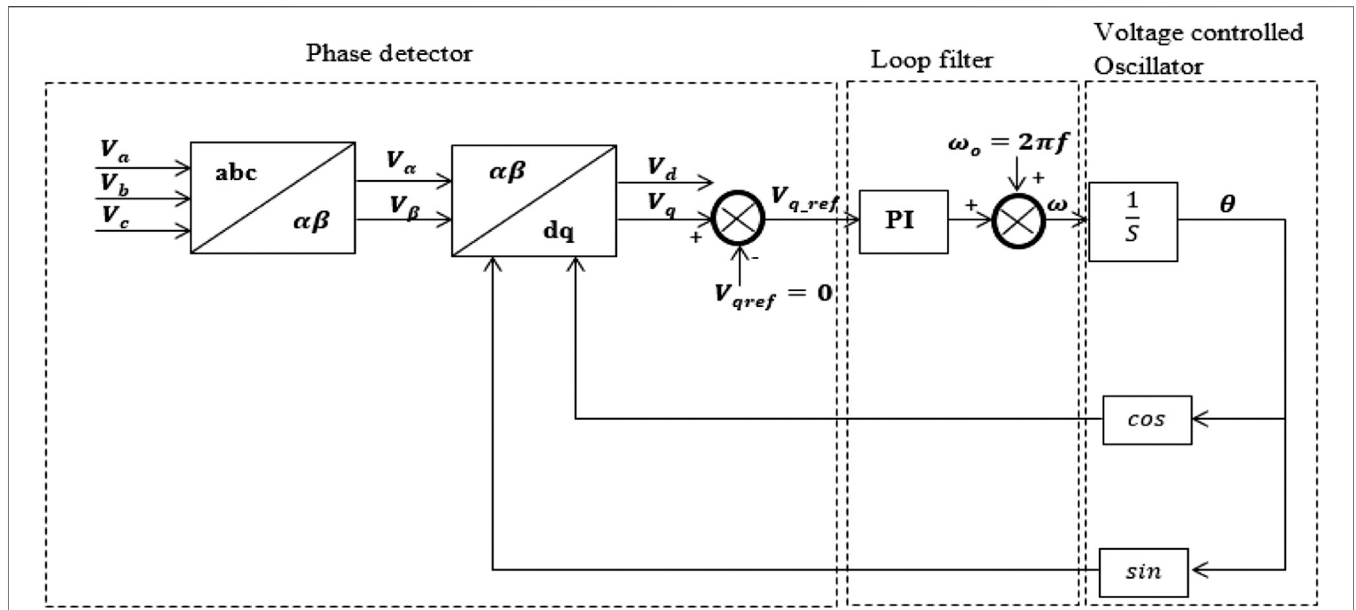


FIGURE 4 | Conventional PLL scheme.

boost its synchronizing strength with the grid for better performance during transient conditions.

Figure 4 shows the conventional three-phase PLL scheme, which is basically an error signal feedback system based on the principle of a synchronous rotating frame, with low pass filters and a voltage-controlled oscillator (Justo et al., 2015). The working principle is based on the conversion of measured voltage of a three-phase system to d-q component via conversion coordinates and set DC voltage reference of q-axis v_{ref} . Figure 5 shows the vector partition diagram for the PLL. From Figure 5, the d-axis component is fully co-phased with the vector voltage when the q-axis component is zero, despite the values of the voltages on the various q-axes. The PI controller in Figure 4 helps in obtaining the frequency of the system. With the grid voltage having only positive sequence fundamental

components, the d-q steady value coordinate is the DC current, and its phase and frequency can be locked by controlling the q-axis component to zero. Frequency detection when the grid voltage is balanced is achieved for the conventional three-phase PLL based on tracking the grid voltage positive sequence fundamental components, as the inner of the PLL is a closed loop controller. However, during transient conditions, there will be a sudden change giving rise to an instantaneous negative sequence and zero sequence fundamental components which leads to the oscillation of the PLL output angle.

If the grid voltage becomes unbalanced, there exists positive, negative, and zero sequence fundamental components. For a typical three-phase system without a neutral point, the zero sequence is not usually considered. Thus, the grid voltage can be expressed as (You-wei et al., 2012).

$$\begin{aligned}
 v_{abc} &= v_{abc}^+ + v_{abc}^- \\
 &= V^+ \begin{bmatrix} \cos \omega t \\ \cos\left(\omega t - \frac{2}{3}\pi\right) \\ \cos\left(\omega t + \frac{2}{3}\pi\right) \end{bmatrix} + V^+ \begin{bmatrix} \cos(\omega t + \theta_0^-) \\ \cos\left(\omega t - \frac{2}{3}\pi + \theta_0^-\right) \\ \cos\left(\omega t + \frac{2}{3}\pi + \theta_0^-\right) \end{bmatrix} \quad (7)
 \end{aligned}$$

From Eq.7, V^+ , V^- gives the voltage amplitude separately for the positive and negative sequences, respectively. θ_0^- gives the relative phase angle of the initial voltage negative sequence. The voltage of the output is achieved after a 3/2 conversion, in $\alpha\beta$ static coordinates and expressed as (Jung-Woo et al., 2007; Da Silva et al., 2008):

$$v_{\alpha\beta} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = T_{\alpha\beta} v_{abc} \quad (8)$$

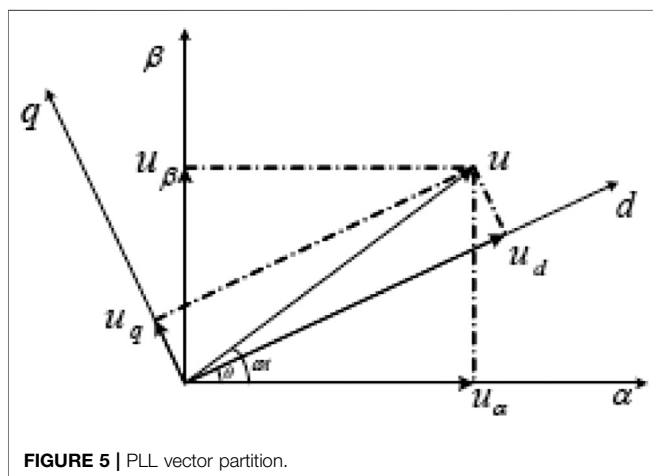


FIGURE 5 | PLL vector partition.

$$T_{\alpha\beta} = \frac{2}{3} \begin{bmatrix} 1 & \frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \quad (9)$$

In the static $\alpha\beta$ coordinates of the grid voltage, the fundamental positive and negative sequence component is given as:

$$v_{\alpha\beta} = v_{\alpha\beta}^+ + v_{\alpha\beta}^- = V^+ \begin{bmatrix} \cos \omega t \\ \sin \omega t \end{bmatrix} + V^- \begin{bmatrix} \cos(\omega t + \theta_0^-) \\ -\sin(\omega t + \theta_0^-) \end{bmatrix} \quad (10)$$

After d-q transformation to the synchronous coordinate system, the following equation is obtained:

$$v_{dq}^+ = T_{dq}^+ v_{\alpha\beta} = T_{dq}^+ v_{\alpha\beta}^+ + T_{dq}^+ v_{\alpha\beta}^- \quad (11)$$

$$T_{dq}^+ = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \quad (12)$$

Considering Eqs 11, 12 leads to

$$v_{dq}^+ = V^+ \begin{bmatrix} \cos \omega t - \theta \\ \sin \omega t - \theta \end{bmatrix} + V^- \begin{bmatrix} \cos(\omega t + \theta_0^- + \theta) \\ -\sin(\omega t + \theta_0^- + \theta) \end{bmatrix} \quad (13)$$

The effective working of the PLL requires that $\omega t \approx \theta$, so Eq.13 can be expressed as

$$\begin{cases} v_{dq}^+ = V^+ + V^- \cos(2\omega t + \theta_0^-) \\ v_{dq}^- = V^- \sin(2\omega t + \theta_0^-) \end{cases} \quad (14)$$

From Eq.14, it could be observed that a synchronous sequence due to the positive system coordinates enables the conversion to DC components from the positive sequence, and for the components of the negative sequence, a value that is twice the frequency component is obtainable. This is because the traditional PI controller can only be used to remove the steady state error, thus the negative voltage will have influence on the output of the PLL.

The traditional PLL strategy has a negative sequence component during transient conditions in the grid. Therefore, a low loop filter cutoff frequency is required to help achieve an improved performance of the system during steady state. Based on this, since the transient performance of the system would also be affected, this study aims to propose a new configuration and control topology of PLL with a delay element as shown in Figure 6, in order to overcome this drawback. The negative effects due to the component of the voltage sequence would be greatly mitigated during transient conditions in the grid with the help of the delay element e^{-sT} .

The principle of the delay element is based on phase shifting after abc/dq transformation in the controller, as shown in Figure 6, compared to the traditional strategy employed for

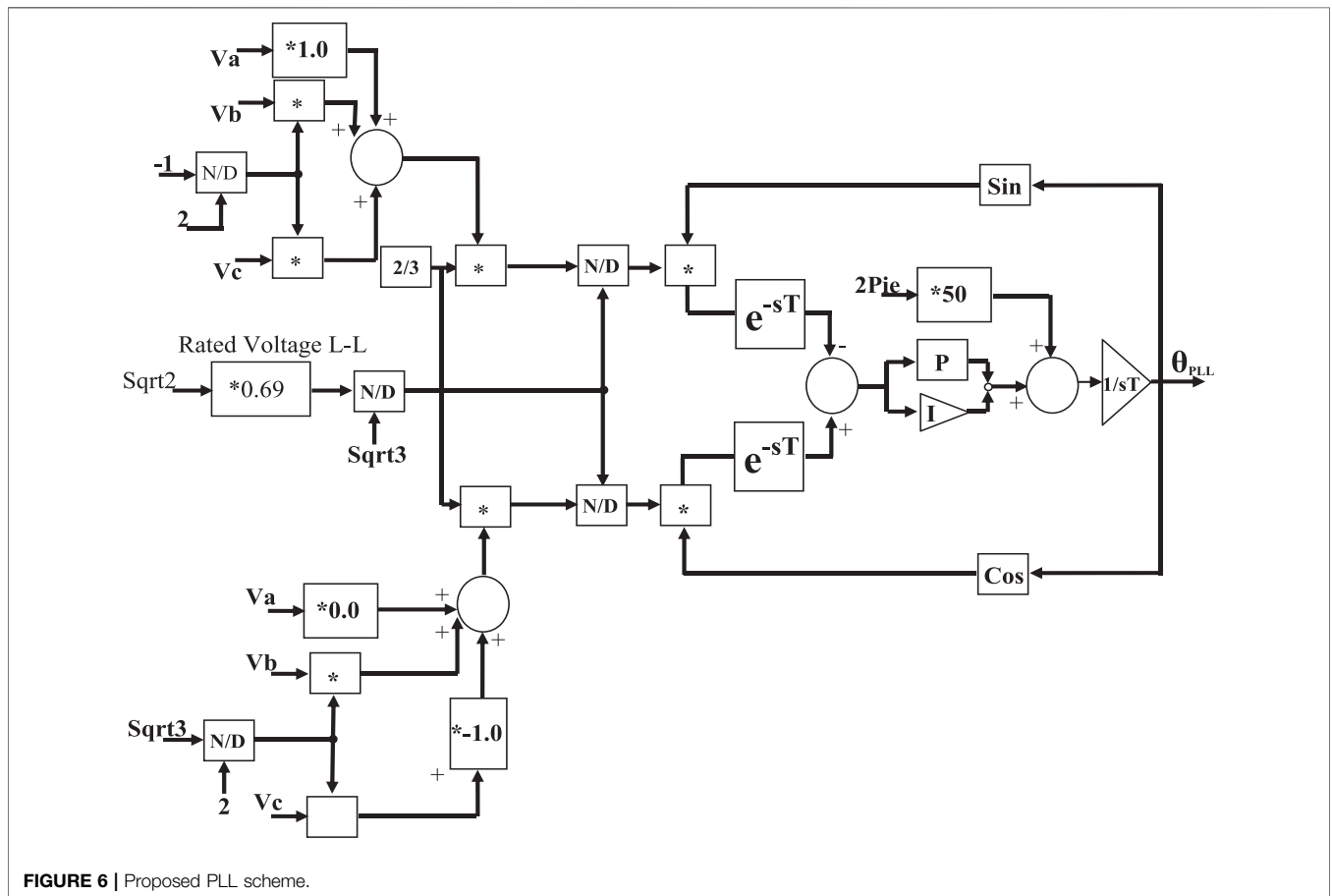


FIGURE 6 | Proposed PLL scheme.

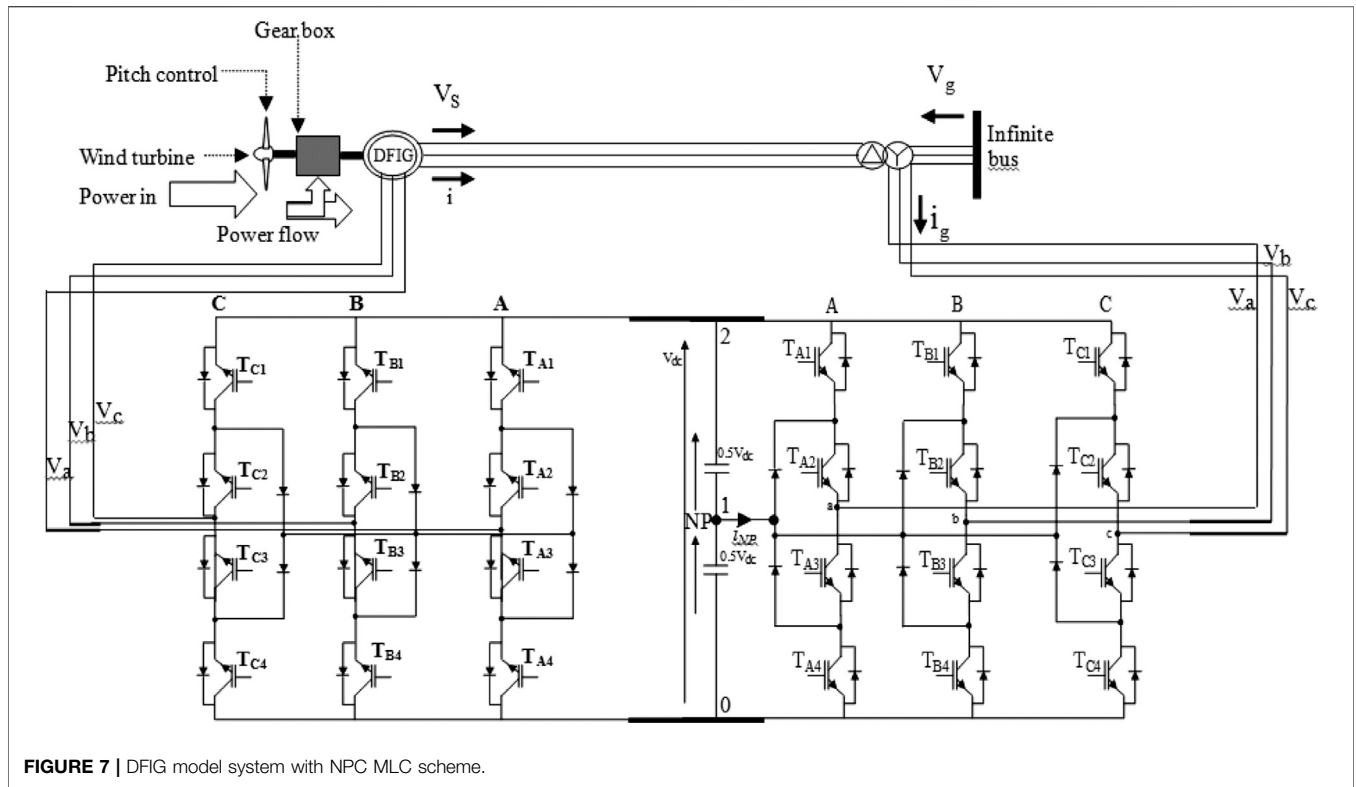


FIGURE 7 | DFIG model system with NPC MLC scheme.

TABLE 1 | DFIG NPC MLC bridge leg voltages for different combinations of switches .

State of leg	V_{a0}	T_{A1}	T_{A2}	T_{A3}	T_{A4}
2	V_{dc}	On	On	Off	Off
1	$0.5 V_{dc}$	Off	On	On	Off
0	0	Off	Off	On	On

the PLL in Figure 4. The proposed control PLL scheme would counteract twice the amount of grid frequency disturbances based on Eq.15.

$$\begin{cases} v_d^+ = \cos 2\omega t + \cos 2\omega\left(t - \frac{\pi}{4}\right) \\ v_q^+ = \sin 2\omega t + \sin 2\omega\left(t - \frac{\pi}{4}\right) \end{cases} \quad (15)$$

DFIG NEUTRAL POINT CLAMPED MULTILEVEL CONVERTER TOPOLOGY

Figure 7 shows the model system for the DFIG wind generator NPC MLC topology. The NPC has three legs, A, B, and C, with three different voltage states. Switch 1 and 3 are complementary on each leg, therefore, when switch 1 is on, switch 3 is off, and vice versa. Similarly, switch 2 and 4 are complementary. From Figure 7, each of the capacitors has a constant voltage of

$0.5 V_{dc}$, therefore having the two upper switches on will lead to an output voltage of V_{dc} compared to 0 level. Also, switch 2 and 3 being on will lead to $0.5 V_{dc}$ and having the two lower switches on leads to an output voltage level of 0. There exists a forbidden state whose scenario is when the first switch is on and the second is off, in addition to the three states. Table 1 shows the bridge leg voltages at different combinations of the switch states. The excitation parameters of the DC circuitry and the DFIG wind generator parameters are given in (Takahashi et al., 2006).

DFIG PARALLEL INTERLEAVED MULTILEVEL CONVERTER TOPOLOGY

Figure 8 shows the model system for the DFIG wind generator Parallel Interleaved MLC topology (Okeku, 2016). Figure 9 shows the table of switching, with the switching sequence of the pulse width modulation represented by the numbers. The space vector reference V_{ref} is formulated based on the nearest three voltage vector summation geometries in region 1, as shown in Figure 10. The connections of the passive filters of the grid side to the parallel interleaved MLC are shown in the model system. The reduction of the harmonics is achieved by the grid filters with a value of 9.6 mH and also with the help of the common mode inductor. The IGBTs are numbered for both RSC and GSC power converters.

For the operation of the two-level conventional SV modulation, the converters cycle through switching cycles with four switch states. However, for the 180° parallel interleaved MLC

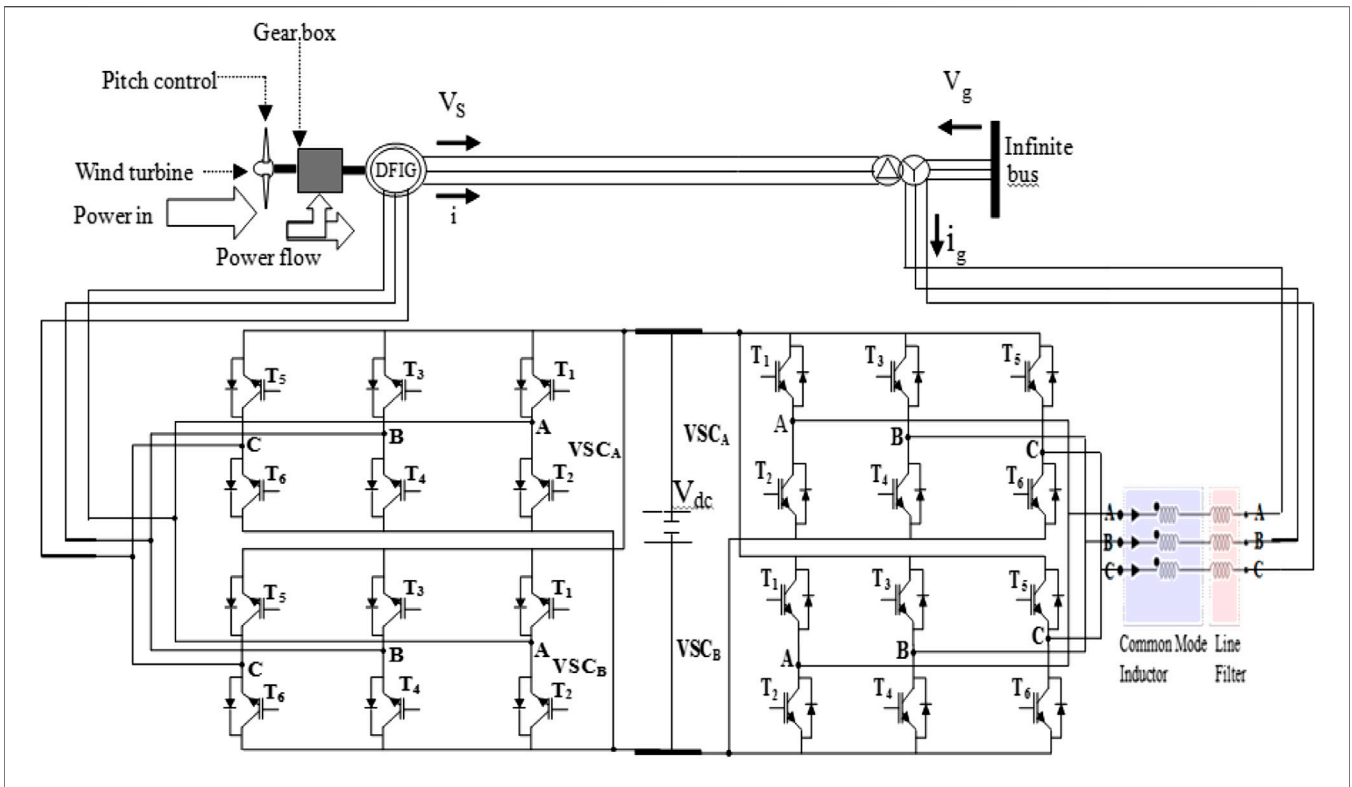


FIGURE 8 | DFIG model system with parallel interleaved MLC scheme.

scheme, its SV modulation gives voltage and the common mode changes with a peak value to $\pm V_{dc}$, whereas for the clamped Discontinuous Pulse width Modulation (DPWM) schemes, this value is $\pm (2V_{dc}/3)$. The common leg flux can be mitigated by the time integral reduction of the common mode voltage change. Avoiding the zero vectors voltage would help achieve this purpose. In this paper, the Near State PWM scheme with

three nearest active voltage vectors to synthesize the reference voltage vector \vec{V}_{ref} is used. The table of switching sequence in Figure 11, for the parallel interleaved MLC, is formulated by the vector space diagram in Figure 12, with six regions, like the NPC MLC scheme earlier discussed. The formulation considers the voltage vectors corresponding to the sequence numbers. However, in the parallel interleaved MLC scheme, the 612

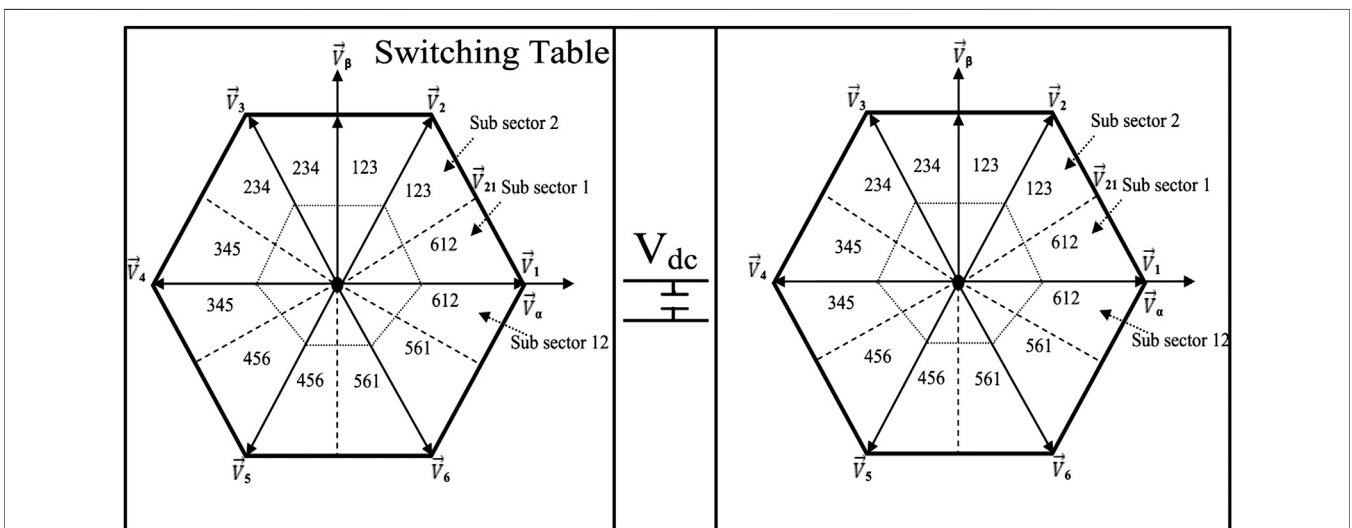


FIGURE 9 | Switching table for the parallel interleaved MLC scheme.

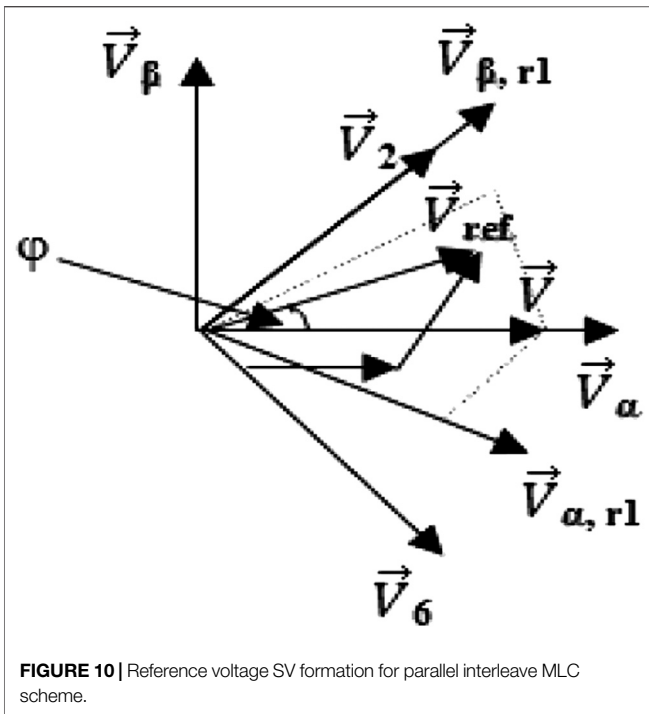


FIGURE 10 | Reference voltage SV formation for parallel interleave MLC scheme.

sequence of switching is employed in sub-sector 1, for $0^\circ \leq \varphi \leq 30^\circ$, and sub-sector 12, for $330^\circ \leq \varphi \leq 360^\circ$. Region 1 is formulated by the geometry for the voltage of reference \vec{V}_{ref} as shown in Figure 12. The two sub-sections and the reference voltage make up region 1. The table of switching and their corresponding dwell times, based on \vec{V}_1 , \vec{V}_2 and \vec{V}_6 active voltages, are (Gohil et al., 2015; Okeku, 2016):

$$T_1 = \left(\sqrt{3} \frac{V_{\alpha,r}}{V_{dc}} + \frac{V_{\beta,r}}{V_{dc}} - 1 \right) T_s \tag{16}$$

$$T_2 = \left(1 - \frac{2}{\sqrt{3}} \frac{V_{\alpha,r}}{V_{dc}} \right) T_s \tag{17}$$

$$T_6 = \left(1 - \frac{1}{\sqrt{3}} \frac{V_{\alpha,r}}{V_{dc}} - \frac{V_{\beta,r}}{V_{dc}} \right) T_s \tag{18}$$

T_1 , T_2 , and T_3 , in Eqs 16–18 are the active vector voltages dwell times, while the time of switching is T_s . The α , β components in Figure 10 are given by V_α , V_β , while the α and β components for region 1, at the beginning of the region, are $V_{\alpha,r}$ and $V_{\beta,r}$. These are expressed mathematically as:

$$V_{\alpha,r1} = \frac{\sqrt{3}}{2} V_\alpha - \frac{1}{2} V_\beta \tag{19}$$

$$V_{\beta,r1} = \frac{1}{2} V_\alpha - \frac{\sqrt{3}}{2} V_\beta \tag{20}$$

$$T_1 = \frac{2}{\sqrt{3}} \left| \frac{\vec{V}_{ref}}{V_{dc}} \right| T_s \sin(60^\circ - \varphi) \tag{21}$$

$$T_2 = \frac{2}{\sqrt{3}} \left| \frac{\vec{V}_{ref}}{V_{dc}} \right| T_s \sin \varphi \tag{22}$$

$$T_3 = T_6 = (T_s - T_1 - T_2)/2 \tag{23}$$

The active vectors (T_1 , T_2) adjacent dwell time for the PWM zero state and for the traditional space vector modulation in Eqs 21–23 are the same. Though in this case, the (\vec{V}_3 , \vec{V}_6) voltage vectors, which are actively opposing two near vectors, are used instead of the zero vectors. Consequently, the operation range of modulation ($0 \leq M \leq 2/\sqrt{3}$) is obtained.

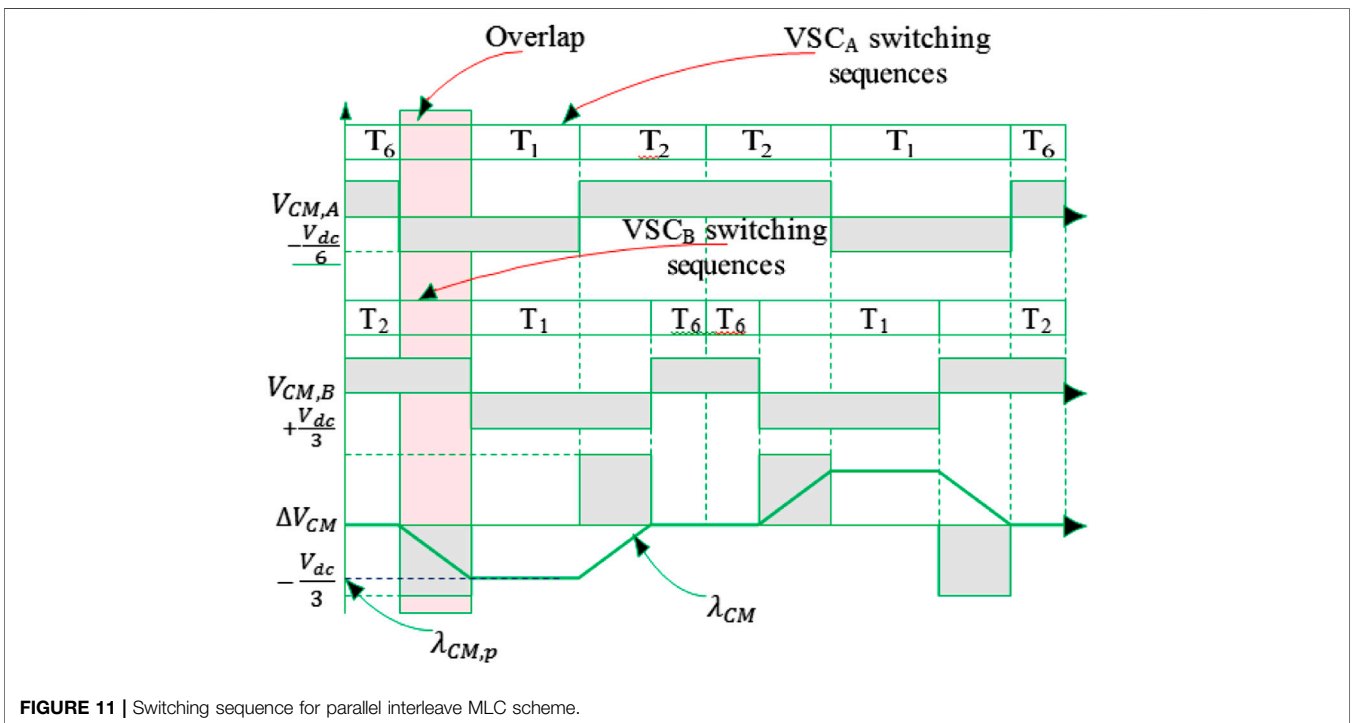
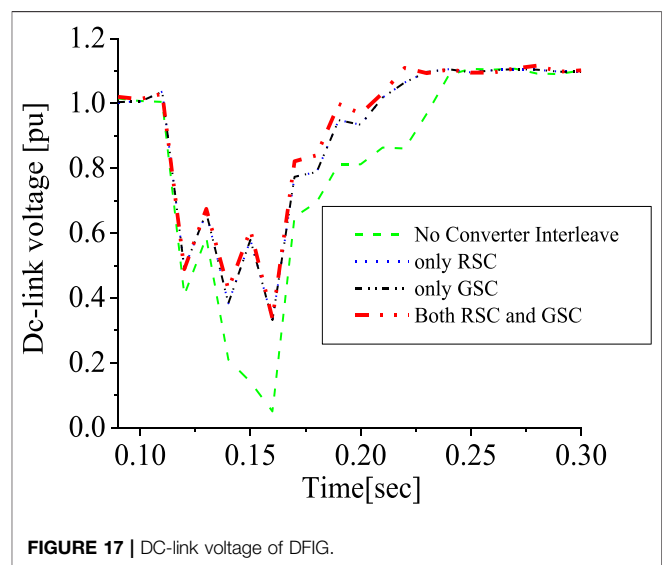
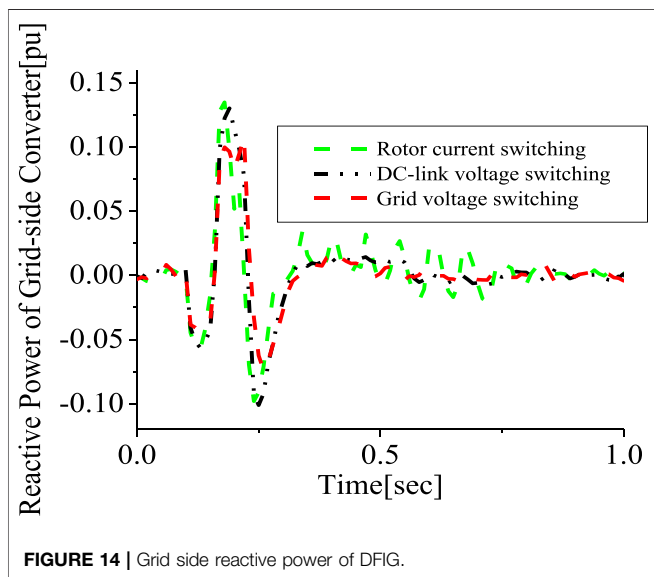
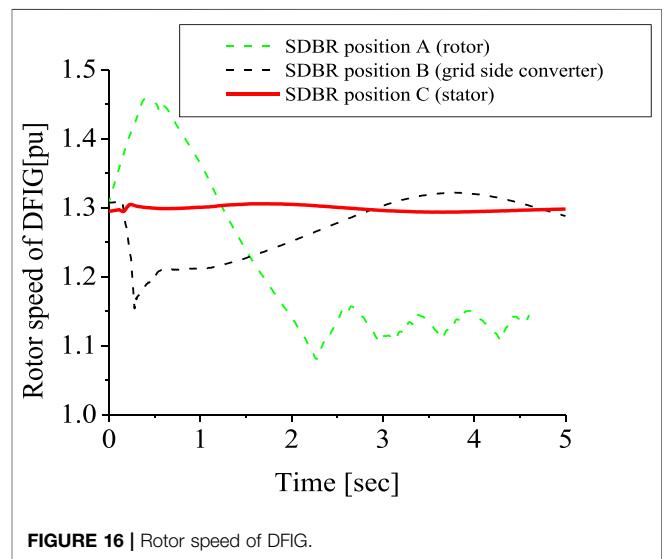
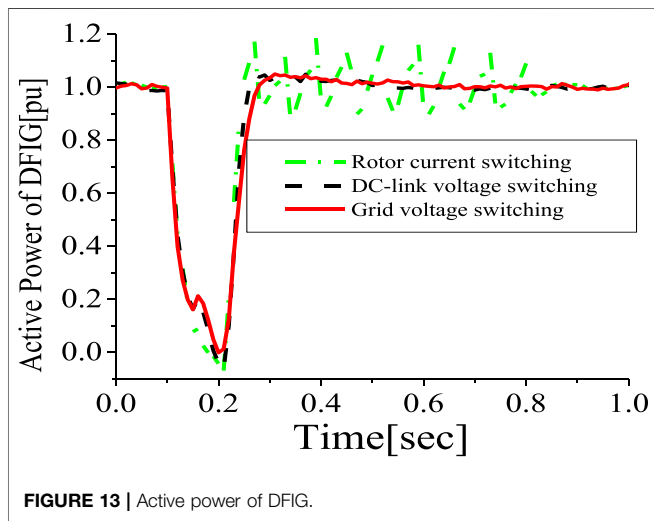
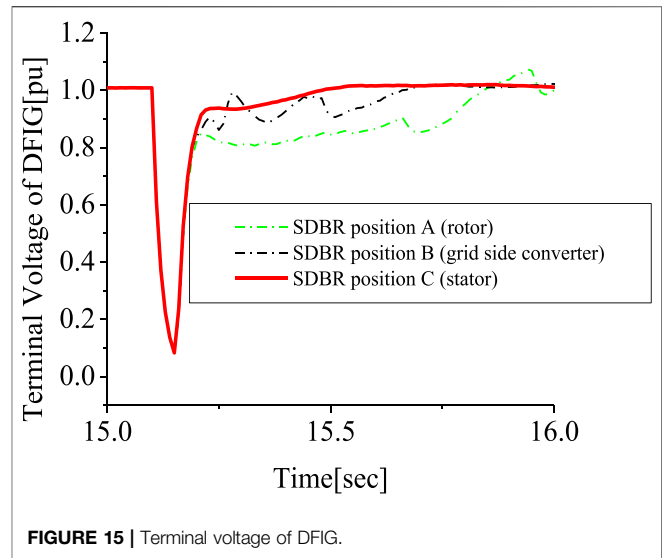
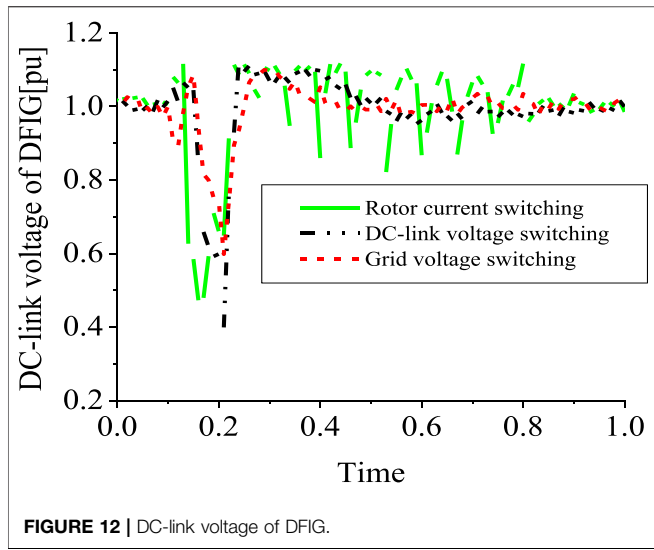
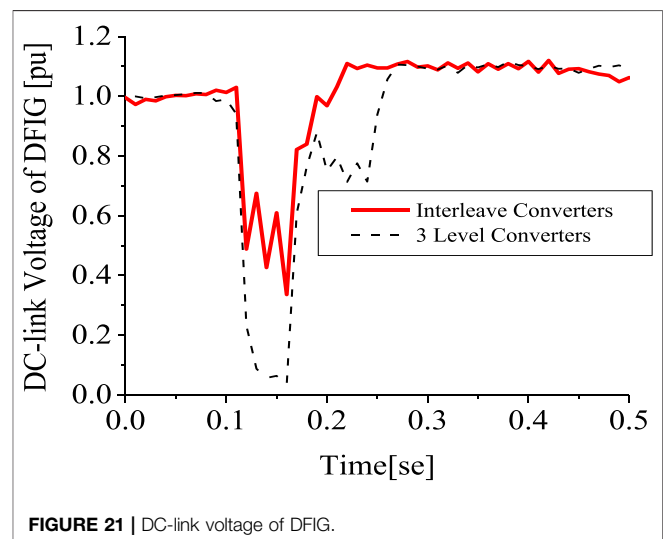
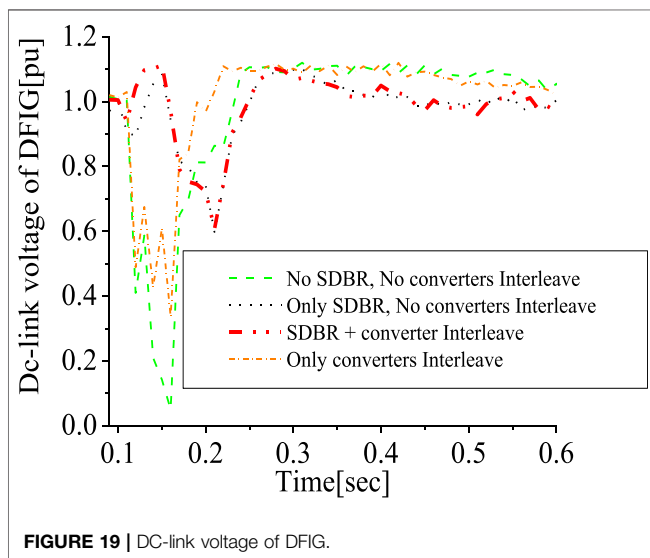
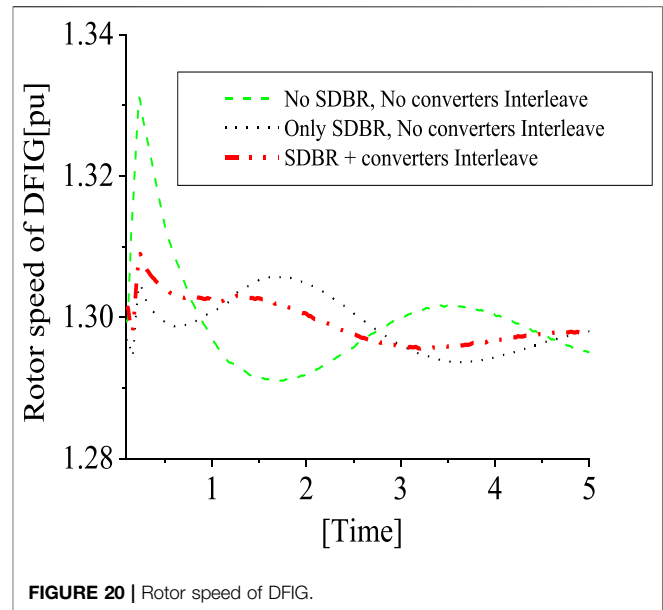
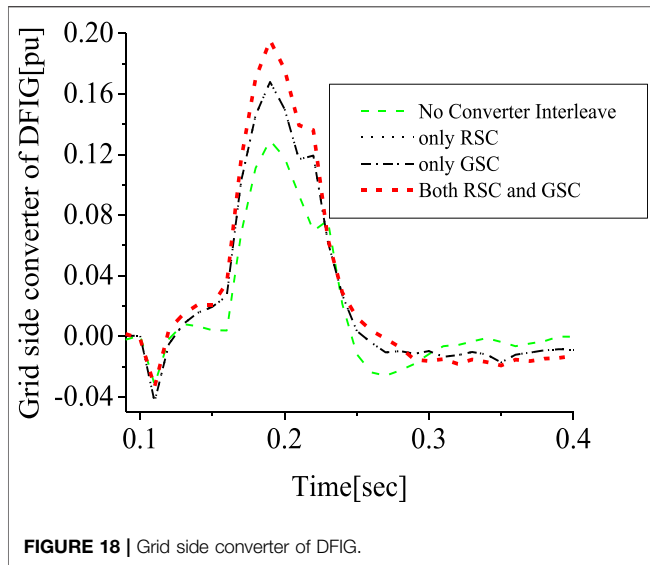


FIGURE 11 | Switching sequence for parallel interleave MLC scheme.





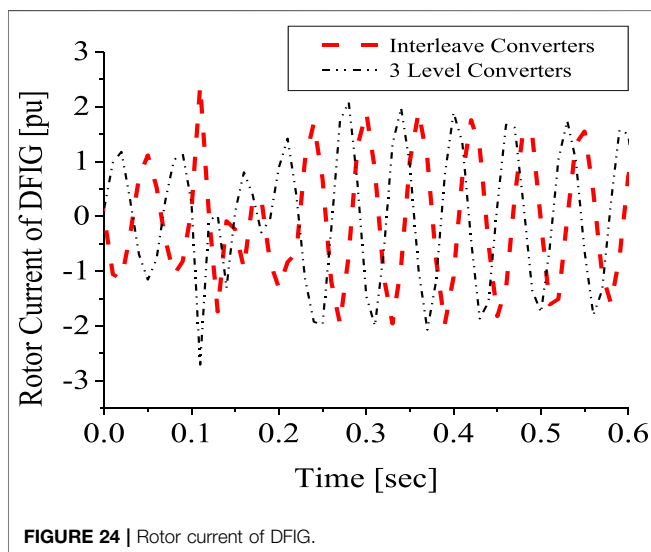
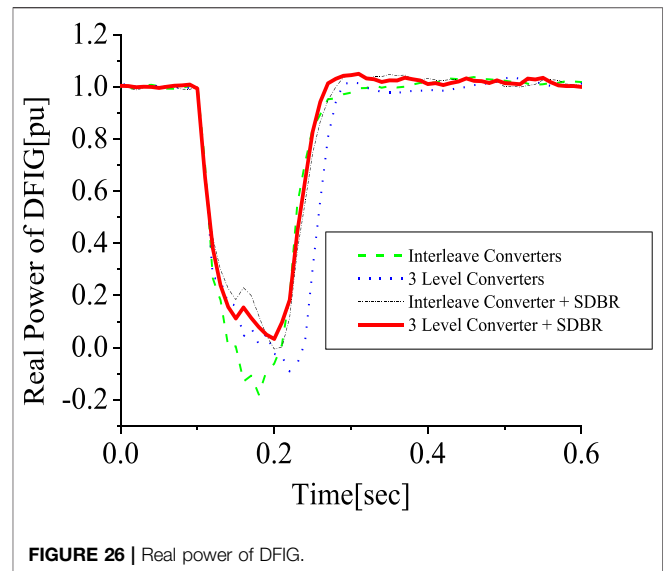
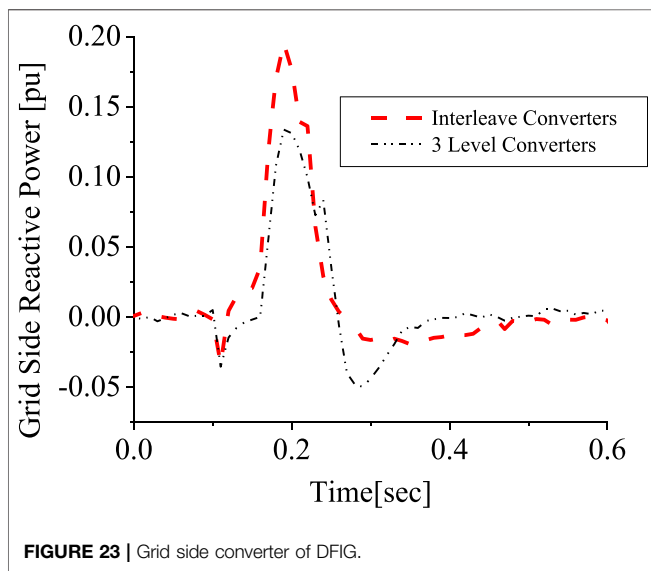
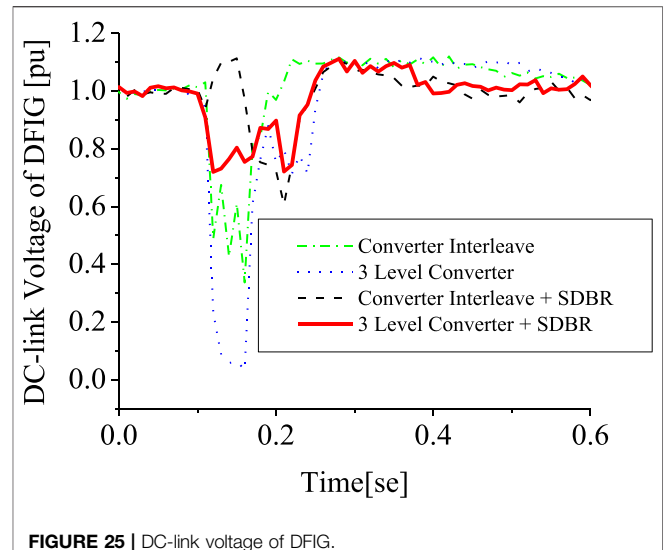
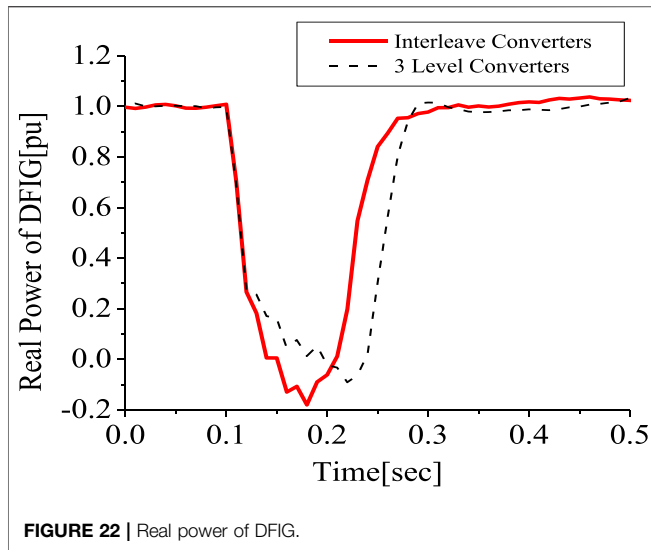
The DFIG parallel interleaved MLC switching sequence and common mode (CM) voltages are shown in **Figure 13** for both converter sides. The two converter halves are tagged A and B, respectively. With a voltage common to each voltage source converter, the maximum individual VSCs' common mode voltage is constrained to $\pm (V_{dc}/6)$. VCM, A and VCM, B and their difference ΔVCM is shown in **Figure 13**. Since only active vectors are used in this topology, the peak CM voltage of the individual VSCs is constrained to $\pm (V_{dc}/6)$. The CM voltages' polarity are equal but opposite for the power converters scheme. Due to the individual CM voltages' opposite polarity, the combined use of \vec{V}_1 and \vec{V}_2 in VSC_A and VSC_B , respectively, and the other configuration in sub sector 1, makes the change in the common mode ΔVCM to confine its value to $\pm (V_{dc}/3)$. Consequently, the flux linkage for a switching $\lambda_{CM,p}$ depends on the voltage vectors' time of overlap, as shown in **Figure 11**, for the voltage of a particular DC-link. These voltage vectors \vec{V}_1 and \vec{V}_6 overlap

time in \vec{V}_{ref} sub sector 12, as shown in the table of switching controls the $\lambda_{CM,p}$ value, which varies with the voltage vector \vec{V}_{ref} reference. Because the changes in the reference voltage is with respect to the space vector angle φ , different values of the switching cycle for the power converter are obtained.

SIMULATION RESULTS AND DISCUSSIONS

SDBR Switching and Position

Simulations were done based on the optimal switching signal (**Figure 2**) and placement (**Figure 1**) of SDBR with a value 0.01 pu for a severe 3LG fault, which occurs at 0.1 s. The two-level inverter



scheme with a DC chopper was used in this investigation. As seen from **Figures 12–14**, the following wind generator variables—DC-link voltage, active power, and reactive power—show improved performances with low distortions, with the use of the braking resistor, when subjected to transient conditions. This was mainly due to the fact that most of the harmonics and vibrations experienced during the transient period were transferred by the rotor current and DC-link voltage signals to the braking resistor circuitry, compared to when the grid voltage signal was employed. The scenario where the braking resistor was inserted at the stator side of the wind generator, considering the grid voltage switching signal, led to an enhanced performance of the terminal voltage and rotor speed variables of the wind generator (**Figures 15, 16**). The reason for this is because the wind generator active power was enhanced, and consequently, its stability was improved. The braking resistor also limits the rotor speed at times of transient changes, thus improving the power output

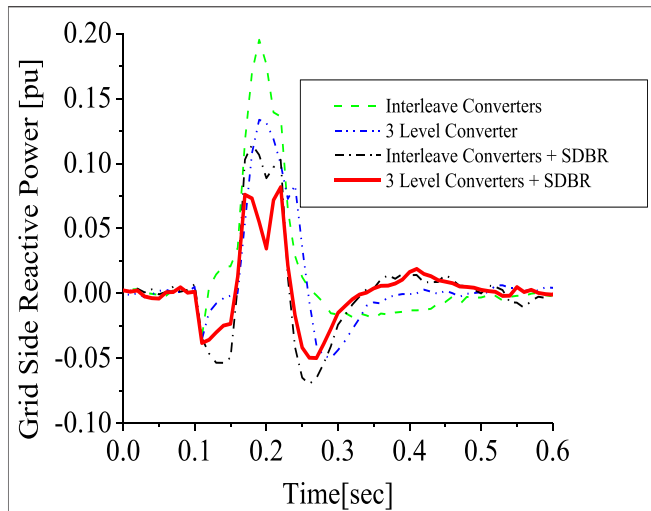


FIGURE 27 | Grid side converter of DFIG.

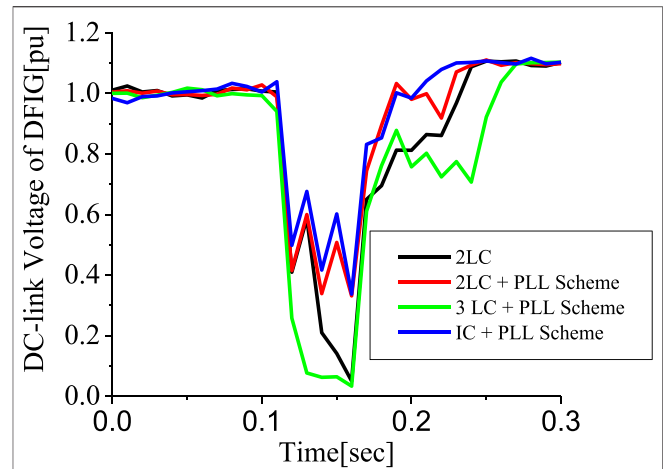


FIGURE 29 | DC-link voltage of DFIG.

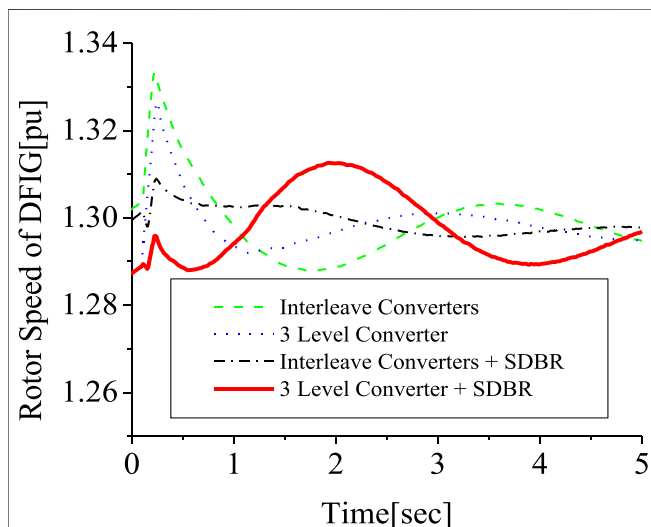


FIGURE 28 | Rotor speed of DFIG.

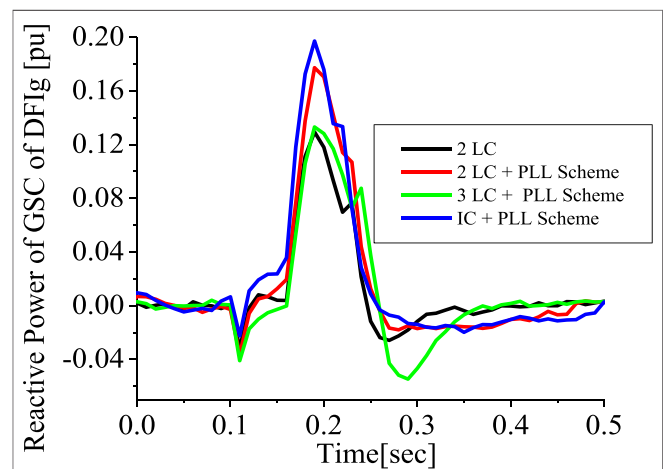


FIGURE 30 | Reactive power of DFIG.

of the wind turbine. Consequently, the recovery of the variables of the wind generator after fault is better because of the control capability of the braking resistor in the acceleration of the rotor speed.

2-Level Interleave Inverter and SDBR

A comparison was made between the single 2-level converter system and when it is interleaved for the wind turbine system. As seen from **Figures 17, 18** for the DC-link voltage and reactive power of the wind generator, interleaving the two side converters using the 2-level converters enhances the stability of the wind turbine during transient changes by providing more reactive power within the DFIG power converters (**Figure 18**). Based on the best SDBR performance for the stator side, as given in section *SDBR Switching and Position* of the simulation results, a further investigation was carried out for the 2-level interleave inverter system to improve the

stability of the wind turbine for the DC-link voltage and the rotor speed variables, shown in **Figures 19, 20**, respectively. The DC-link charging current of the capacitor is mitigated during fault scenario in order to avoid the under- or over-voltage experienced, as shown in **Figure 19**. In addition, this topology effectively controls the voltage and current in the rotor circuitry. This would definitely improve the rotor speed of the DFIG as shown in **Figure 20**.

3-Level Inverter, 2-Level Interleave Inverter, and SDBR

Investigation was further carried out comparing the responses of the 3-level inverter and the 2 level interleave inverter. The responses of the DFIG DC-link voltage and active power in **Figures 21, 22**, respectively, is better for the 2-level interleave inverter than the 3-level inverter due to more reactive power being supplied, as shown in **Figure 23**. However, the response of

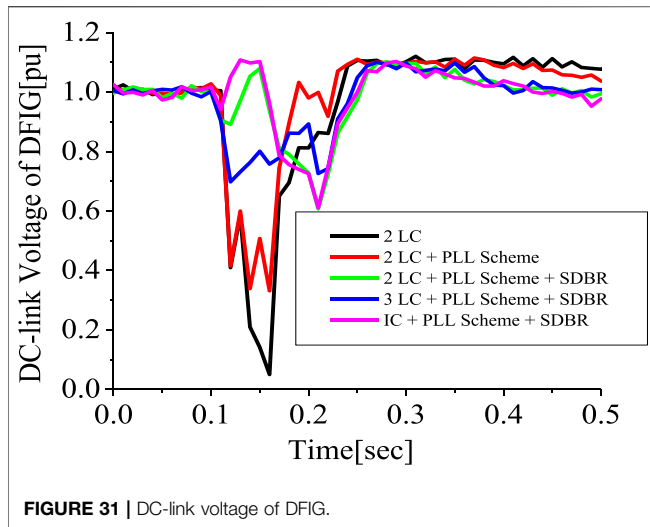


FIGURE 31 | DC-link voltage of DFIG.

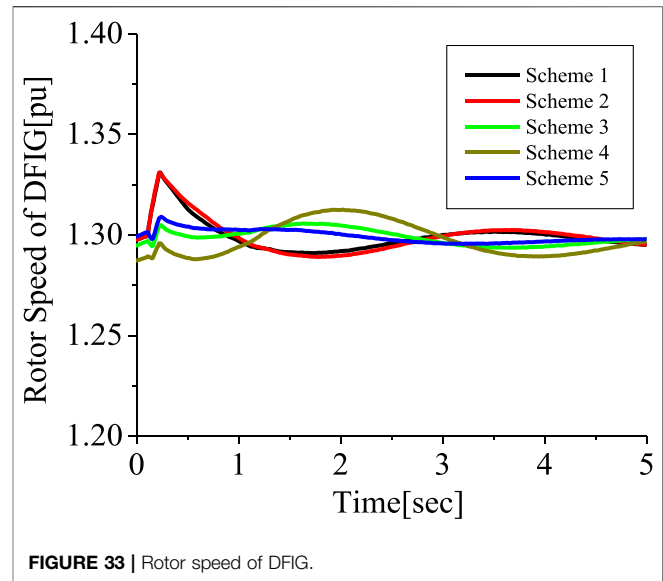


FIGURE 33 | Rotor speed of DFIG.

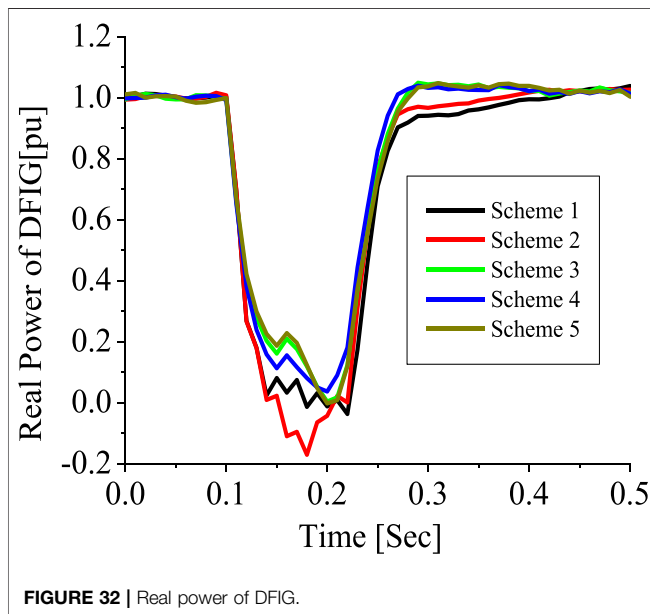


FIGURE 32 | Real power of DFIG.

the rotor current is almost the same, but in different directions, as shown in **Figure 24**, for both converter systems. An addition of SDBR to both systems, as shown in **Figures 25–28**, shows that the SDBR can further enhance the performance of both inverter schemes for the DC-link voltage, real power, reactive power of the grid side converter, and rotor speed of the wind generator. The response of the 2-level interleaved inverter is slightly better because the SDBR more greatly limits the reactive power (**Figure 27**) for the 3-level inverter.

Proposed PLL Control Strategy and the Various Schemes

The conventional PLL has been used in the earlier analysis. This section investigates five schemes. Scheme 1 is the 2-level converter (2LC) using the conventional PLL, scheme 2 is the

2LC with the proposed PLL scheme in **Figure 6**, scheme 3 is the 2LC with a proposed PLL scheme and SDBR. Schemes 4, 5 uses the 3-level converter (3LC), and parallel Interleave converter (IC), having the proposed PLL scheme and SDBR, respectively. **Figure 29** shows the response of the DFIG wind turbine DC-link voltage considering the various converter schemes without SDBR. The response of the DC-link voltage using the proposed PLL scheme for the 2-level converter system is better than when the conventional PLL scheme was used. This is because the proposed PLL scheme helps in enhancing the reactive power of the DFIG grid side converter (**Figure 30**). The coordinated control of SDBR with the proposed scheme shows that a better performance of the wind turbine variables could be achieved during transient changes for the DC-link, real power, and rotor speed of the wind generator as shown in **Figures 31–33**. In **Figure 31**, the SDBR and the proposed PLL scheme enhances the single step 2-level inverter, thus giving a better response than the interleaved and 3-level inverter schemes. This is also the same for the wind turbine real power in **Figure 32** and rotor speed in **Figure 33**, respectively.

CONCLUSION

In this paper, the DFIG variable speed wind turbine performance operating with three types of inverter system has been investigated. The 2 level single step inverters, 2 level parallel interleaved inverters, and 3 level inverter systems for a DFIG wind turbine during transient changes were presented. An SDBR was used to enhance the performances of all the inverter systems.

Furthermore, a Phase Lock Loop (PLL) was proposed in conjunction with the SDBR system to improve the performance of the wind turbine using a 2-level single step inverter system. It was observed that the proposed PLL SDBR strategy can further improve the performance of the 2-level single

step inverter system during transient changes, thus enhancing the transient responses of the wind turbine.

DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/Supplementary Material, further inquiries can be directed to the corresponding author.

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AUTHOR CONTRIBUTIONS

KO did the conception, simulations and design of the controllers in the work. HB did the literature review and sponsorship of the work.

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Conflict of Interest: The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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