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RECEIVED 24 September 2024

ACCEPTED 15 January 2025

PUBLISHED 14 February 2025

CITATION

Li W, Huang Y, Liu C, Valencia A and Daoud WA
(2025) Low-loss power management strategy
for weak and low-frequency biomechanical
energy harvesting for new generation
wearable electronics.
Front. Electron. 6:1501178.
doi: 10.3389/felec.2025.1501178

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Low-loss power management strategy for weak and low-frequency biomechanical energy harvesting for new generation wearable electronics

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Introduction: Amidst the rapidly growing development of wearable electronics, their dependence on external power sources increases the power expense while leading to interruptions of their operation during charging. Biomechanical energy harvesters offer a promising solution for self-powered wearable electronics by converting waste kinetic energy to electricity. Despite successful efforts in advancing their power outputs from μW to mW , several challenges persist, including low output current at the μA -level, high internal impedance in the $\text{G}\Omega$ -level, and AC outputs, restricting their practical applications. Conventional power management circuits are commonly utilized in high-frequency harvesters without adequate consideration of the energy loss that incurs, potentially leading to circuit failure when used in low-frequency harvesters with a lower power output.

Methods: Here, we introduce a low-loss power management circuit (L-PMC) that functions under low-frequency conditions to facilitate biomechanical energy harvesting.

Results: Our innovative two-stage energy transfer strategy boosts the energy extraction efficiency to 42.24%, breaking previous records. With an energy transfer efficiency of 30.59%, L-PMC can charge a battery from 1.9 V to 2.4 V in just 10 min.

Discussion: Moreover, the integration of passive current amplification tripled charge accumulation and energy storage, representing 207% enhancement in energy transfer efficiency, presenting a versatile and universal approach to low-frequency biomechanical energy harvesting for new generation wearable electronics.

KEYWORDS

biomechanical energy harvester, power management, circuit optimization, impedance matching, low-frequency energy storage, energy transfer

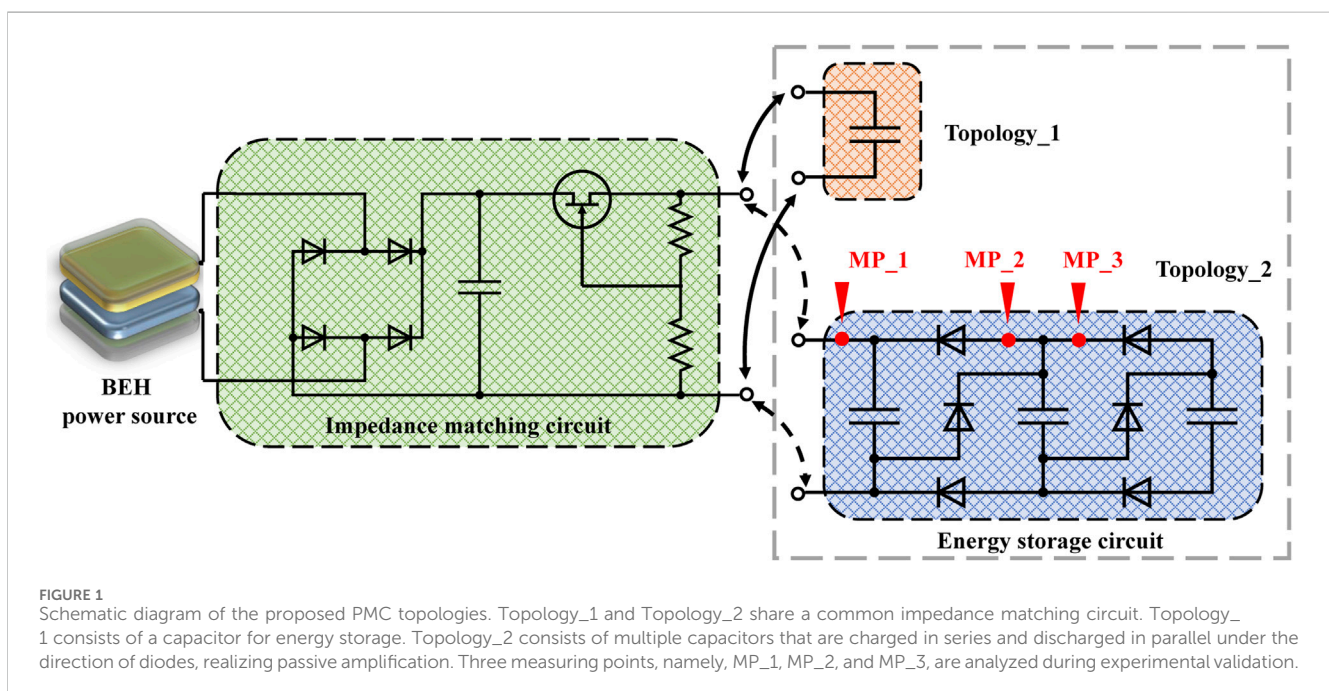
1 Introduction

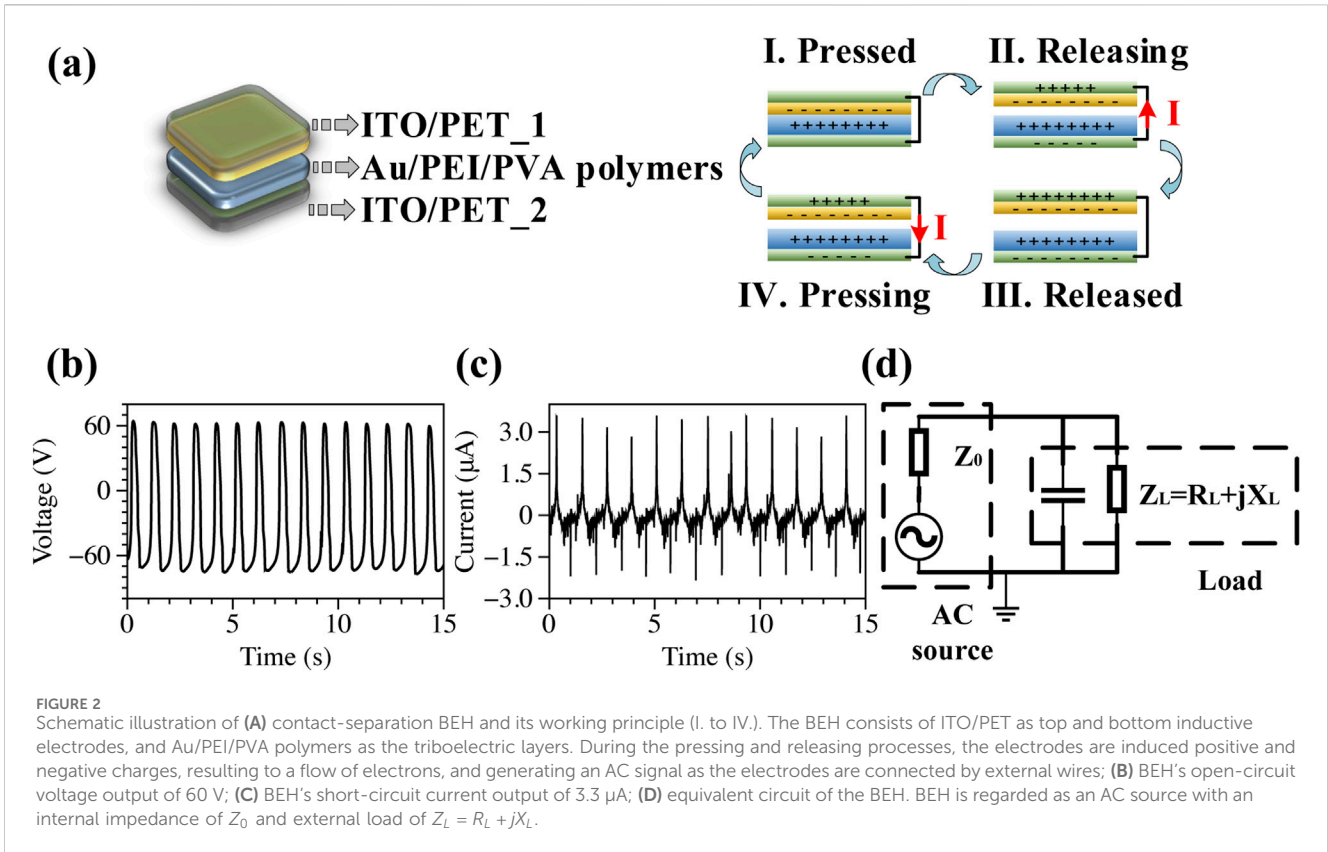
The power management circuit (PMC) plays a vital role in realizing the integration of renewable energy sources with energy storage systems, enabling efficient energy transfer to address the rising energy demand for new generation wearable electronics (Faisal et al., 2018; Xu et al., 2014; Abhinav and Pindoriya, 2016; Kaper and Choudhary, 2016; Nouri et al., 2024; Abdelsattar et al., 2024). Biomechanical energy harvesters (BEH), first reported in 2012 (Fan et al., 2012), convert ambient mechanical energy into electricity using electrification and electrostatic induction effects, offering a promising weather-independent and compact energy alternative compared to other renewable energy sources (Jiang et al., 2015; Wang, 2019; Zi and Wang, 2017; Zhang H. et al., 2024). However, as the device responds to external stimuli, the varying frequency and magnitude of mechanical energy inputs result in fluctuations in electricity generation, causing difficulties in energy integration and storage. Moreover, the typically high output voltage (up to kV-level), weak output current (μA -level), and AC outputs of BEH restricts their use as direct power sources or for battery charging, where a relatively low-voltage (V-level), high-current (mA to A-level), and DC electricity source is required. The mismatch between BEH sources and terminal appliances reduces the energy extraction and transfer efficiency, resulting in considerable energy loss. To address this problem, the integration of PMC is essential.

To date, PMCs have been studied for AC/DC conversion and capacitor charging when operating with a relatively greater current output from high-frequency BEH sources (Niu and Wang, 2015; Shankaregowda et al., 2016; Lee et al., 2014; Zhang Z. et al., 2024; Zhou et al., 2023; Wang et al., 2023). However, commercial full-wave bridge rectifier and capacitors often experience leakage currents, which can result in circuit failure when the current output from low-frequency BEH sources is much lower. This simple topology works

well to temporarily store energy in capacitors for powering portable electronics, such as smartwatches and humidity meters (for seconds). However, its energy extraction and transfer efficiencies are very limited due to the mismatch between the internal impedance of BEH sources and external circuit load. Resistor-inductor-capacitor (RLC) impedance matching circuits with buck conversion functionality have been researched to improve energy extraction (Zhang Z. et al., 2024; Fang et al., 2020; Zhao et al., 2017; Kong et al., 2010; Wang et al., 2015). Inductors function in discontinuous mode, when their current direction changes within a single switch on-and-off cycle (Supplementary Figure S1), leading to an RLC series resonance phenomenon under light-loading ($\leq 30\%$) or no-loading. Its pulse current and voltage electromagnetically interact with the BEH source, resulting in greater ripple, which requires additional filtration, resulting in energy loss and reduced energy transfer efficiency. In summary, BEH for battery charging has been minimally studied. Less efficient RLC impedance matching and high energy loss due to inappropriate component sizing reduce energy extraction and transfer efficiencies, respectively (Kong et al., 2010; Shi et al., 2022).

A low-loss PMC (L-PMC) technique is explored in this study for the purpose of weak biomechanical energy harvesting at low-frequency. Since the current and intermittence of BEH affect circuit efficiency and are determined by the operating frequency, we studied the PMC under extreme conditions at 1 Hz. The objective is to realize battery charging by reducing current ripple and energy loss, while attaining efficient energy extraction and transfer efficiency to fulfil the requirements of a reliable and readily available DC power source. This work incorporates two PMC topologies, as seen on Figure 1. Topology_1 is a 2-stage RC impedance matching circuit with buck conversion functionality. The analyzed Topology_1 achieves an energy extraction efficiency of 42.24% and can charge a battery to 20% in 10 min at a low operating frequency of 1 Hz. Topology_2 is a multi-capacitor unit for current





amplification, further enhancing the energy transfer efficiency from 30.59% to 63.55%, representing 207% enhancement. The study is conducted in three phases: 1) mathematical derivation for impedance matching, 2) circuit topology design and simulation, and 3) experimental validation.

2 Materials and methods

2.1 Biomechanical energy harvester

A 3 cm \times 3 cm contact-separation BEH device was fabricated as the power input of the PMC, with working principle as shown in Figure 2A (Wang et al., 2020). The device features Au/PEI/PVA as the tribo-positive layer, PET as the tribo-negative layer, and PET-ITO as the top and bottom electrodes. The device was packaged using Kapton tape, with a 2 mm air gap between the triboelectric layers. Upon pressing and releasing the device, the PET and Au/PEI/PVA layers became negatively and positively charged, respectively, due to their differing electronegativity. Externally, electrons flowed between the top to bottom electrodes, and the cyclic operating mode of the device resulted in an AC power output.

2.2 Measurements

The output performance of the BEH was measured using source meters (Keithley 2400 and 6514) and a low-noise current

preamplifier (SR570). A linear motor (LinMot) supplied biomechanical energy. The device output was measured at 1 Hz, with a positioning movement of 0.015 m per cycle, an acceleration of 1 m/s², and a maximum speed of 1 m/s. PMC performance was simulated using NI Multisim, LTspice, and MATLAB simulink. The BEH output remained steady after 1,250 cycles, with an open-circuit voltage of 65 V, a short-circuit current of 3.3 μ A, and a power density of 108.33 mW/m², as shown in Figures 2B, C. Operating frequency greatly affected device output. Supplementary Figures S2, S3 show device's output under different operating frequencies ranging from 0.5 to 5 Hz. This study only considers low-frequency conditions and thus operates at a frequency of 1 Hz unless stated otherwise.

2.3 Mathematical derivation for impedance matching

Due to the capacitive property of BEH, its huge internal impedance makes it difficult to output power on the external load without a well-considered impedance matching. To study this process, consider an equivalent circuit as shown in Figure 2D. The AC power source is ideal with an internal impedance of Z_0 and an external load impedance of Z_L . To be universally applicable, both Z_0 and Z_L consist of two components: resistance (R) and reactance (X) in Equations 1, 2.

$$\text{Internal impedance: } Z_0 = R_0 + jX_0 \quad (1)$$

$$\text{External impedance: } Z_L = R_L + jX_L \quad (2)$$

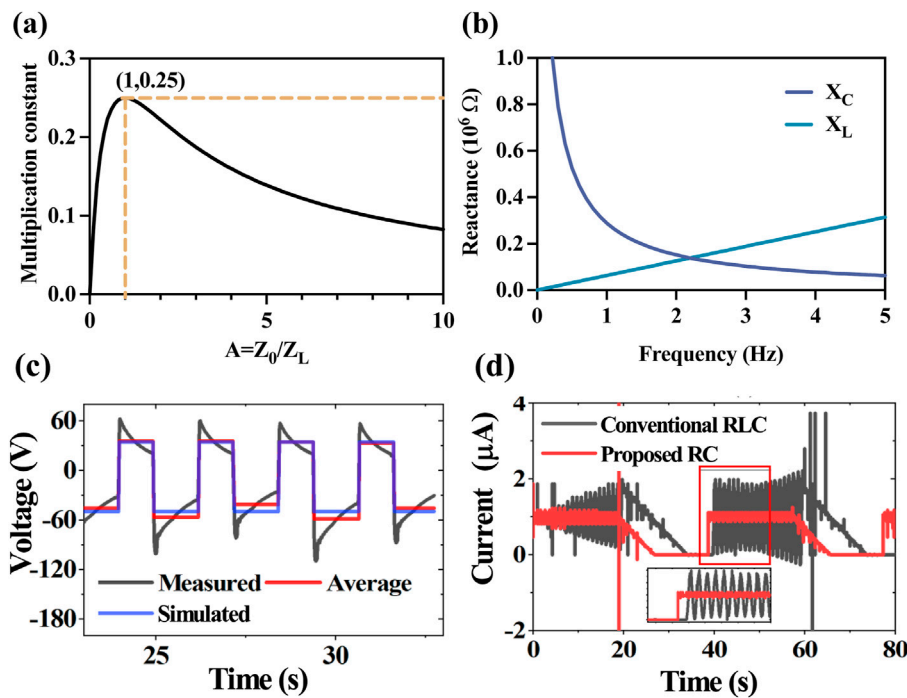


FIGURE 3 (A) Multiplication constant of K depends on ratio between Z_0 and Z_L . The curve is generated by MATLAB based on Equation 7. A peak of 0.25 is calculated when Z_0 equals to Z_L , where the theoretical maximum power on external load is achieved; (B) reactance of X_C and X_L depends on operating frequency. When the operating frequency is lower than 1 Hz, X_C dominates and X_L can be disregarded. K is calculated to be approximately 0.25, indicating that with low operating frequency, impedance matching by the capacitor results in a maximum power output on external load; (C) simulation process of the open-circuit voltage of BEH. To replicate the recorded voltage of 60 V (shown by the black line), the average value is calculated as depicted by the red line. Fluctuations are found in the negative phase of the voltage curve. Thus, to standardize the signals, a pulse value of 48 V and a duty ratio of 43% is used for further simulation (blue line); (D) comparison on current ripple on the external load with an RLC circuit (black line) and an RC circuit (red line). The introduction of an RC circuit has effectively reduced the current ripple caused by the discontinuous conductive mode of the RLC.

According to Ohm’s Law and voltage division principle, load voltage and load current can be derived in Equations 3, 4. The output power on load can be calculated using Equation 5.

$$V_L = \frac{Z_L}{Z_0 + Z_L} V_0 \tag{3}$$

$$I_L = \frac{V_L}{Z_L} = \frac{Z_L V_0}{(Z_0 + Z_L) Z_L} \tag{4}$$

$$P_L = V_L I_L = \frac{Z_L V_0}{(Z_0 + Z_L)} \times \frac{Z_L V_0}{(Z_0 + Z_L) Z_L} = \frac{Z_L V_0^2}{(Z_0 + Z_L)^2} \tag{5}$$

$$A = \frac{Z_0}{Z_L} \tag{6}$$

$$K = \frac{A}{(A + 1)^2} \tag{7}$$

$$P_L = \frac{V_0^2}{Z_0} \times \frac{A}{(A + 1)^2} = \frac{V_0^2}{Z_0} \times K \tag{8}$$

The varied A is used to denote the ratio between Z_0 and Z_L in Equation 6. As V_0 and Z_0 are determined by the device itself and can be regarded as constants, the multiplication constant of K in Equation 7 is introduced to facilitate comparison among various impedance matching strategies. The power input on external load in Equation 5 can be further expressed by Equation 8.

2.3.1 RLC complex conjugate matching

The maximum power on loads of an RLC matching circuit occurs when the load impedance is the complex conjugate of the source impedance for a fixed AC source (Kong et al., 2010; Niu et al., 2014), which is an ideal result. The external impedance under complex conjugate matching process can be further described as:

$$\text{External load impedance: } Z_L = R_0 - jX_0 \tag{9}$$

According to Equations 8, 9, the theoretical maximum power on external load can be derived in Equation 10:

$$P_{L,conjugate} = \frac{V_0^2}{Z_0} \times K = \frac{V_0^2}{4Z_0} \tag{10}$$

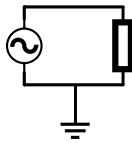
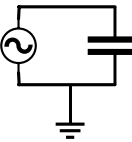
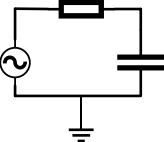
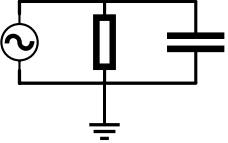
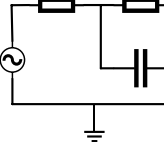
According to Equation 7, K for RLC complex conjugate matching is 0.25 with A equals to 1, as shown in Figure 3A.

2.3.2 Resonance RLC matching

Resonance RLC matching is studied to achieve theoretical maximum power on external load, where the reactance of inductor and capacitor is equal. The relationship of L and C in this case is described by Equation 15

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C} \tag{11}$$

TABLE 1 Mathematical description of load impedance Z_L with different circuit topologies.

Topology structure	Description of Z_L	Description of Z_L under low-frequency
	$Z_L = R_L$	$Z_L = R_L$
	$Z_L = \frac{1}{j\omega C_L}$	$Z_L = \frac{1}{j\omega C_L}$
	$Z_L = R_L + \frac{1}{j\omega C_L}$	$Z_L = \frac{1}{j\omega C_L}$
	$Z_L = \frac{R_L}{1 + j\omega R_L C_L}$	$Z_L = R_L$
	$Z_L = R_1 + \frac{R_2}{1 + j\omega R_2 C_L}$	$Z_L = R_1 + R_2 = R_L$

$$\frac{1}{X_C} \propto f \tag{12}$$

$$X_L = \omega L = 2\pi f L \tag{13}$$

$$X_L \propto f \tag{14}$$

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{15}$$

$$I_{Leakage} = k \times C \times U \tag{16}$$

With a fixed operating frequency of 1 Hz, the empirical formula for capacitor leakage current in Equation 16 states that the constant of current leakage (k) is equal to 0.003 for electrolytic capacitors in industries (Shi et al., 2022). Here, C represents the capacitance of the capacitor and U is the rated voltage of the capacitor. With U in the hundreds of volts, to ensure that the capacitor leakage current does not result in circuit failure, only capacitors with C no larger than μF and a $I_{Leakage}$ no larger than μA can be used for BEH applications. In this case, RLC resonance can only be achieved when the inductance (L) is more than 20 kH while using a μF -capacitor; however, this configuration would occupy too much space for wearable and portable electronics.

2.3.3 Proposed RC matching

To simulate the output of the BEH, its average voltages were calculated and used to generate a pulse signal, shown by the red line

in Figure 3C. To enhance the uniformity of the simulated pulse signal, a pulse voltage source with a pulse value of 48 V and a duty ratio of 43% was used for simulation, as shown by the blue line. Figure 3D shows the current ripple elimination through the proposed RC impedance matching. By taking out the inductor from the RLC (which operates in a discontinuous mode) and adding a capacitor for energy storage and filtering, the proposed RC impedance matching enhances the stability of the output. This modification helps prevent capacitor failure and improves the efficiencies of energy transfer and extraction. According to Equations 11–15, the reactance depends on operating frequency, as shown in Figure 3B, with a capacitance of 1 μF and an inductance of 20 kH. When operating under a very low frequency, the X_C is significantly greater than X_L . The RC strategy's K is very close to 0.25. This proposed RC strategy can achieve a power output that is closer to the theoretical maximum while also being suitable for practical applications.

3 Results

3.1 Circuit topology design and simulation

The RC circuit topology design is examined from two specific perspectives, namely, the resistive load (R) and the capacitive load

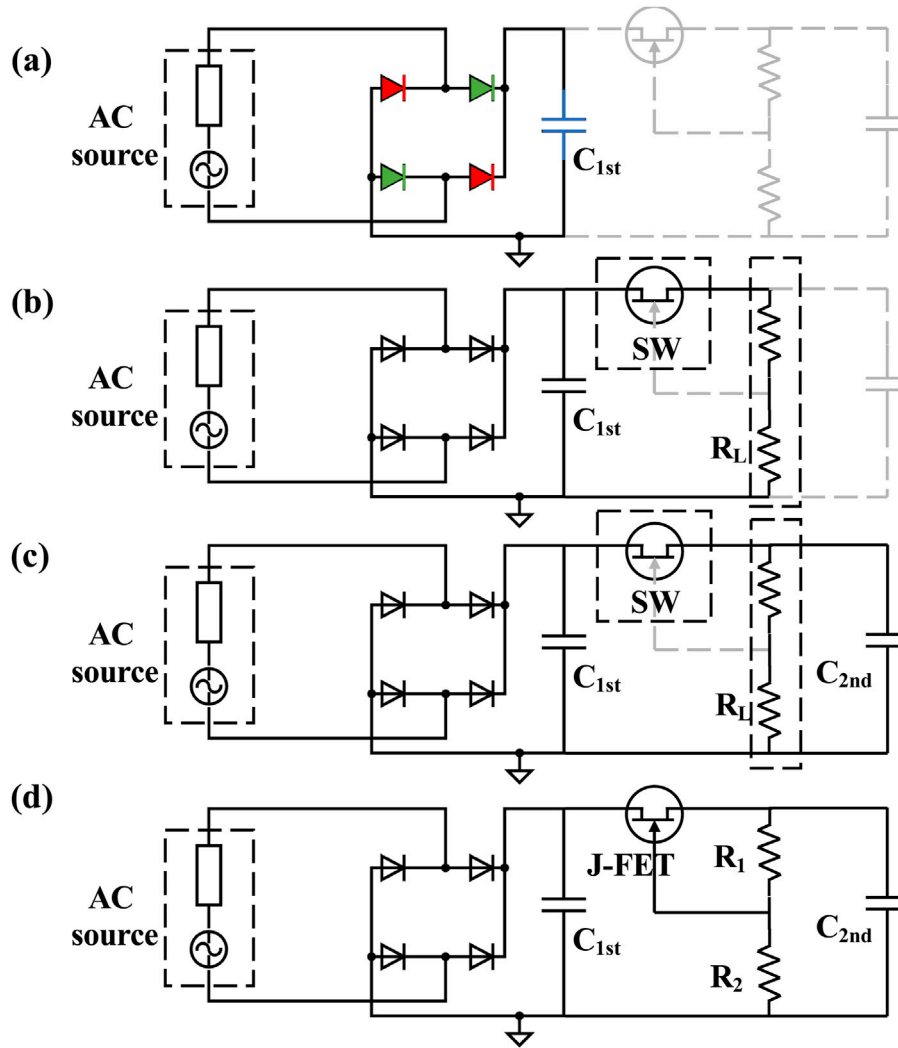


FIGURE 4 Circuit topologies with (A) AC/DC conversion; (B) RC impedance matching; (C) Second-level capacitor; (D) Switch control.

(C), to minimize energy loss and maximize power production. Various permutations and combinations of R and C result in distinct circuit topologies and varying load impedances (Z_L), as summarized in Table 1. The characterization of Z_L can be further refined based on the RC load behavior during low-frequency operation. Equation 11 states that $X_{L,C}$ approaches infinity at low frequencies, providing a significant advantage over R_L and exerting a major impact on the Z_L of the second and third topologies in Table 1. In contrast, when components are connected in parallel, the impedance of a circuit is mostly determined by the smaller impedance component. Therefore, R_L have a significant impact on the first, fourth, and fifth topologies. Thus, to simplify the modelling process, the circuit topologies are categorized into two groups based on their impedance characteristics.

3.1.1 Powering a resistive load

Using BEH to power a pure resistive external load, the power output on load can be described as:

$$P_L = V_L I_L = \frac{V_0}{\left(\frac{Z_0}{R_L} + 1\right)} \times \frac{V_0}{(Z_0 + R_L)} = \frac{V_0^2}{\left(\frac{Z_0^2}{R_L} + 2Z_0 + R_L\right)} \quad (17)$$

Deriving Equation 17 with respect to R_L ,

$$P'_L (R_L) = \frac{V_0^2 \left(\frac{Z_0^2}{R_L^2} - 1\right)}{\left(2Z_0 + R_L + \frac{Z_0^2}{R_L}\right)^2} \quad (18)$$

The optimum power on external load can be obtained when Equation 18 equals to '0', which occurs at an external load in Equation 19:

$$R_L = R_0 + \frac{1}{j\omega C_0} \quad (19)$$

Therefore, the R_L is determined by the operating frequency of the BEH for an optimum matching, lacking universality for circuit applications.

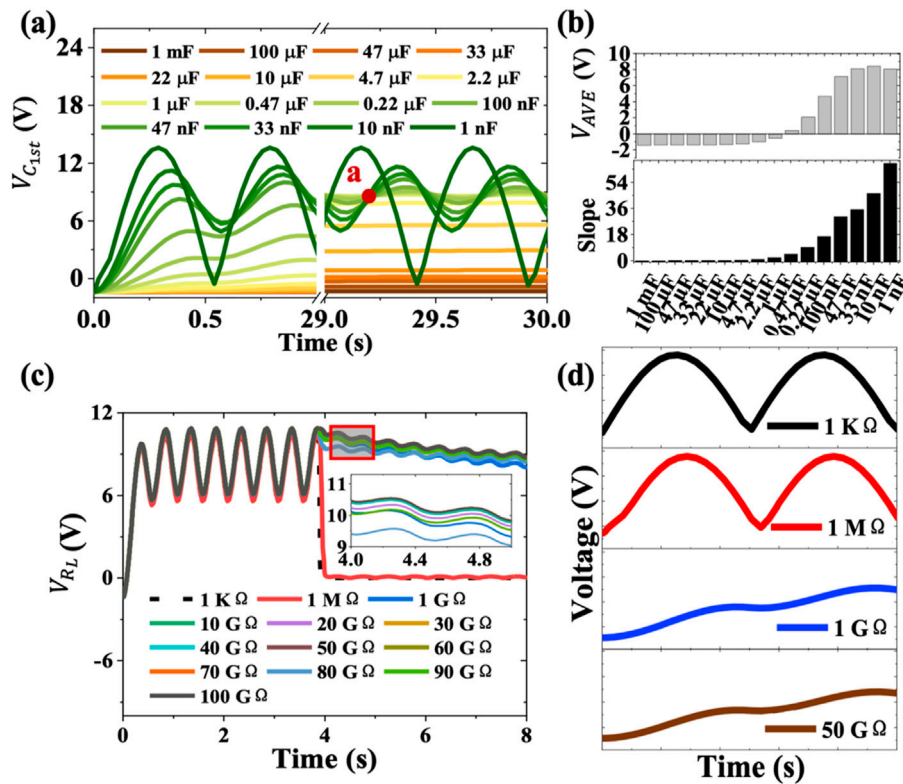


FIGURE 5 (A) Dependence of voltage accumulation on varying C_{1st} ranging from 1 nF to 1 mF within 30s operation period; (B) Average voltage of C_{1st} within one operation cycle, and voltage accumulation curve slopes of varying C_{1st} . C_{1st} of 1 nF–33 nF demonstrates similar V_{AVE} . 33 nF shows the highest energy extraction efficiency where it depends on capacitance only. For longer operation period, C_{1st} of 1 nF cannot achieve filtration, 10 nF to 1 μ F exhibit identical voltage, while 1 μ F shows highest energy transfer efficiency where it depends on capacitance only; Dependence of voltage accumulation of varied R_L range from 1 K Ω to 100 G Ω on the (C) 8s operation period (inset displays output at 4s–5s). An R_L at the G Ω -level demonstrates effective filtration; (D) charging-discharging waveform of varied R_L .

3.1.2 Charging a pure capacitive load

The voltage $V(t)$ and the current $I(t)$ are cyclic functions of time for an AC power source.

$$V(t) = V_{peak} \sin(\omega t) \tag{20}$$

$$I(t) = \frac{dq}{dt} = \frac{Cdv}{dt} = C\cos(\omega t) \tag{21}$$

Given Equations 20, 21, the voltage and current consistently exhibit a 90° phase delay, resulting in a total energy buildup of zero on the external load during a single operation cycle. This ineffective charging of the external load highlights the need for an AC/DC conversion circuit. Here, we investigated four specific elements of topology modification to improve the PMC based on the pure capacitive load approach.

3.1.3 Modification with AC/DC conversion

A full-wave bridge rectifier consisting of four diodes is introduced to convert AC electricity into pulsed DC electricity to avoid energy elimination within one operation cycle. The circuit topology is shown in Figure 4A. Instead of using a commercially assembled rectifier designed for power levels ranging from mW to W, we selected four low-loss diodes to match the BEH's power level of μ W. The energy storage on the capacitive load can be described as:

$$E = \frac{1}{2} CV^2 \tag{22}$$

$$\eta = \frac{E_L}{E_0} = \frac{V_L^2 C_L}{V_0^2 C_0} = B \frac{C_L}{C_0} \tag{23}$$

C_L is the capacitance of external load, while C_0 is the internal capacitance of BEH. Charging a capacitor is a dynamic process as charge accumulates over time. With continuous device operation, V_L theoretically equals to V_0 given adequate charging time. Equation 23 can be simplified by introducing B as a constant factor, defined as $\frac{V_L^2}{V_0^2}$. Thus, the energy extraction efficiency largely depends on C_L . However, C_L of capacitor cannot be increased infinitely since this can cause excessive current leakage, reducing circuit efficiency and resulting to circuit failure. To assess the circuit performance over a short operation period, the mathematical model must be revised.

$$C = \frac{Q}{V} \tag{24}$$

Deriving from Equations 23, 24, the energy extraction efficiency can be expressed as:

$$\eta = \frac{Q_L V_L}{Q_0 V_0} \tag{25}$$

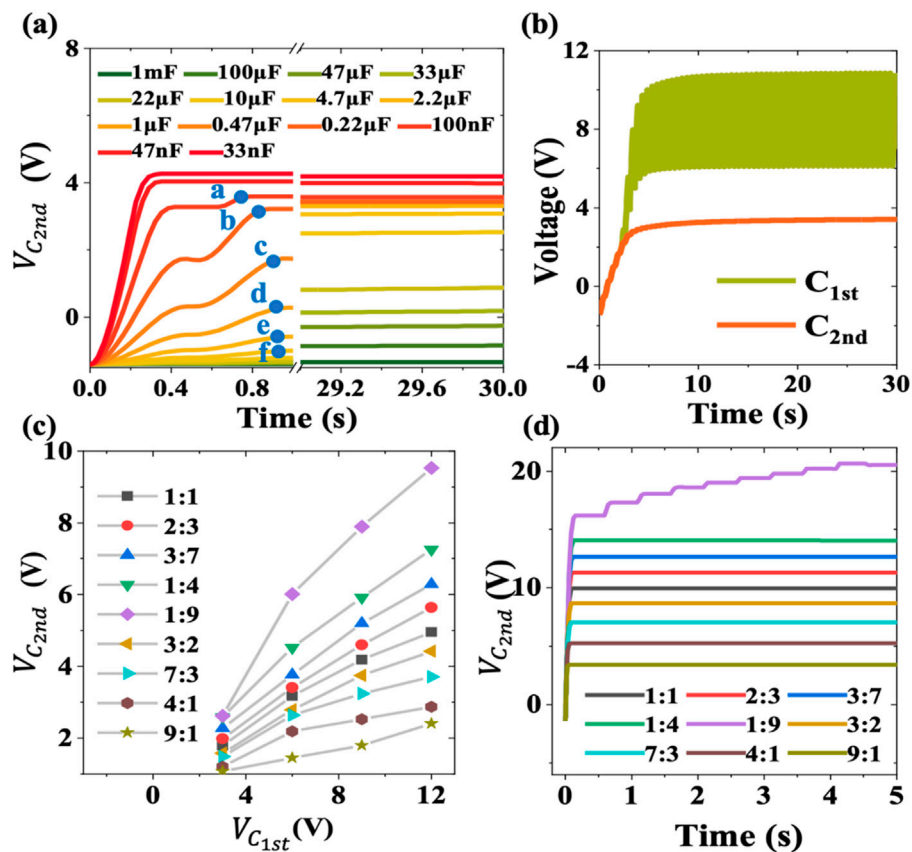


FIGURE 6

(A) Dependence of voltage accumulation on C_{2nd} ranging from 33 nF to 1 mF within 30s operation period; (B) Dependence of voltage accumulation on a C_{1st} of 33 nF and a C_{2nd} of 1 μ F within 30s operation period, and under varying ratios of $R_1:R_2$; (C) Dependence of $V_{C_{2nd}}$ on $V_{C_{1st}}$; (D) Dependence of $V_{C_{2nd}}$ on operation period with an input voltage of 35 V.

Assuming there is no additional energy loss between the device and the capacitor load. Based on Equation 25, the charge transfer amount is fixed within one operation cycle of the power source, and the efficiency depends on V_L .

According to the simulation results with an AC power source of 3 μ A and 35 V in Figure 5, an nF-level capacitor demonstrated higher energy extraction efficiency within one operation cycle, particularly with a larger V_L , as shown in Figure 5A. The average voltages (V_{AVE}) of various C_{1st} are summarized in Figure 5B. C_{1st} of 1 nF, 10 nF and 33 nF exhibited nearly identical V_{AVE} , indicating that the energy extraction efficiency depends primarily on capacitance, with the 33 nF showing the highest efficiency. For a longer operation period of 30s, C_{1st} ranging from 10 nF to 1 μ F achieved equivalent voltage as indicated by their intersection point 'a' in Figure 5A, with the 1 μ F capacitor demonstrating optimum performance due to its larger capacitance. Experimental validation was conducted for C_{1st} values ranging from 10 nF to 1 μ F.

3.1.4 Modification with RC filtration

A switch is used to control the circuit connection between C_{1st} and R_L as shown in Figure 4B. C_{1st} is charged by the BEH when the switch was turned off, and discharge to R_L when the switch was turned on. The discharging process is affected by the different values of R_L , as the power delivered to R_L is inversely proportional to its

resistance. This resulted in a smoother voltage waveform due to the faster-charging and slower-discharging processes, achieving filtration as shown in Figures 5C, D. Moreover, with a 1 K Ω and 1 M Ω R_L , the discharge voltage approaches zero in Figure 5C, indicating that R_L was too small compared to the BEH's internal resistance, and was being short-circuited. From the enlarged voltage waveform in Figure 5C, with a G Ω -level R_L , C_{1st} discharged effectively, providing a stable voltage to the circuit. The filtration effects remained consistent across various G Ω -level R_L , with nearly identical discharge slopes and output voltages.

As demonstrated by the mathematical model, larger capacitance leads to higher energy transfer efficiency over an extended operation period. A C_{1st} of 33 nF is optimized for the highest energy extraction efficiency within a short operation period (one cycle). Figure 4C introduces a second-level capacitor, designated as C_{2nd} , aimed at enhancing energy transfer efficiency increased capacitance.

The simulation results of C_{2nd} ranging from 33 nF to 1 mF are shown in Figure 6. C_{2nd} demonstrated lower voltage accumulation rate and values with an increase in capacitance (Figure 6A). C_{2nd} with a capacitance of 33 nF demonstrate the fastest and highest voltage accumulation. C_{2nd} values ranging from 2.2 μ F to 33 μ F exhibit a slower voltage accumulation with increasing capacitance. C_{2nd} values ranging from 47 μ F to 1 mF show an invalid energy storage without voltage accumulations, indicating a significant

amount of energy loss in terms of current leakage. Moreover, C_{2nd} of 0.22 μF , 0.47 μF , and 1 μF reached the same voltage level (around 4 V) in 30s, indicating that the energy transfer efficiency depends on capacitance only in this case, and that C_{2nd} of 1 μF has the highest energy transfer efficiency. When comparing the short-time charging performances of 33 nF (maximum voltage accumulation) and 1 μF (highest energy transfer efficiency), there is a 1.2-fold difference in voltage. However, the capacitances differ by a factor of 30.3-fold, indicating that the difference in capacitances have a major effect on the energy transfer efficiency. Thus, 1 μF is identified as the optimum C_{2nd} value, providing a balance between charging time and energy transfer efficiency.

3.1.5 Addition of a J-FET transistor switch

The purpose of buck conversion during battery charging in this work is to achieve a safe charging voltage of 3 V. To regulate the voltage, we introduce a J-FET transistor switch, where the voltage division between the gate and drain (V_{GS}) terminals defines its actuated state. L-PMC uses an n-type J-FET in its linear mode as a variable resistor to regulate its voltage. The regulated voltage of C_{2nd} load is $V_{C_{2nd}}$. Since the feedback current to JFET is very low ($\sim\text{nA}$), R_1 and R_2 can be up to $G\Omega$, leading to less power consumption. During operating cycles, the energy is stored in C_{1st} first, leading to increased $V_{C_{2nd}}$. V_{GS} is reduced as a result of increased $V_{C_{2nd}}$. Thus, drain current decreased, leading to reduced $V_{C_{2nd}}$. Therefore, the circuit can be used to regulate voltage. An R_L of 50 $G\Omega$ is divided into R_1 and R_2 for voltage division controlling, and the circuit topology is shown in Figure 4D.

According to the simulation results in Figures 6C, D, the switch can effectively regulate $V_{C_{2nd}}$ lower than $V_{C_{1st}}$ with an $R_1:R_2$ ratio of more than 3:2, and larger ratio leads to a better buck conversion performance. On the contrary, the switch has no obvious regulation effect on $V_{C_{2nd}}$ with a ratio of $R_1:R_2 = 1:9$ since the voltage before and after the RC units remains within the same range. With a voltage input of 35 V, the circuit output voltage is controlled to approximately 3 V with a ratio of $R_1:R_2 = 9:1$, perfectly aligning with the battery charging requirement. With the circuit topology illustrated in Figure 4D, a noisy $V_{C_{1st}}$ of 10 V is transformed to a stable $V_{C_{2nd}}$ of 3 V as shown in Figure 6B.

3.1.6 Passive amplification unit

Recently, a charge excitation circuit (CEC) has been proposed to enhance the device's surface charge density (Wang et al., 2020; Liu et al., 2019; Liu et al., 2020). However, this topology faces challenges related to potential air breakdown. Unlike CEC, the proposed passive amplification strategy using multiple capacitors enhance charge accumulation and amplifies current without introducing any active components which can cause additional energy consumption. The capacitors are charged in series to fully utilize the output from the BEH, and discharged in parallel to achieve a current amplification with a constant discharging voltage. According to the voltage accumulation results of C_{1st} in Figure 6B, the $V_{C_{1st}}$ is approximately 9V, which is 3-fold higher than the $V_{C_{2nd}}$ of approximately 3 V, underscoring the feasibility of this approach. The simulation and experimental results for Topology-2 are shown in Figure 8. Voltages from three measuring points (MP1, MP2, and MP3) in Figure 2 were collected to validate the concept. Moreover, voltage, charge,

and energy accumulation of Topology_1 and 2 are compared to evaluate the circuit performance.

$$I = \frac{\Delta Q}{\Delta t} = \frac{\Delta VCN}{\Delta t} \quad (26)$$

In Equations 22, 26, N represents the number of the multiple capacitors, and t is the operation period. A 3-fold increment in Q leads to 3-fold increments in I and E with Topology_2, indicating an improved circuit performance.

3.2 Experimental validation of L-PMC

3.2.1 RC filtration circuit

Experimental validation of C_{1st} ranging from 10 nF to 1 μF is shown in Figures 7A–D. C_{1st} of 10 nF demonstrated a highest voltage accumulation within one operation cycle; however, the voltage dropped to around 3 V after 30s, likely due to limited filtration. C_{1st} of 33 nF exhibited the highest voltage accumulation which is stable after long-time charging of 30s. Based on Equation 22, the energy accumulation ($E_{C_{1st}}$) is summarized in Figure 7C. C_{1st} of 33 nF showed maximized energy storage, approximately 3.75 times higher compared with other capacitors, confirming the simulation results and validating it as the optimized capacitance value in this L-PMC. As for the experimental verification of C_{2nd} , the nF-level capacitors showed higher $V_{C_{2nd}}$ but lower $E_{C_{2nd}}$ in Figures 7E–H. The 0.47 μF capacitor exhibited higher $E_{C_{2nd}}$ within 30s but was eventually matched by the 1 μF capacitor after an extended charging period of 160s with a more stable voltage. Thus, 1 μF is identified as the optimum sizing of C_{2nd} in this L-PMC, confirming the simulation conclusions.

3.2.2 J-FET switch

$V_{C_{2nd}}$ can be effectively controlled with resistor ratios of $R_1:R_2 = 3:2$, 7:3, 4:1, and 9:1 according to the simulations. A DC power source is used for experimental verification in Figures 7I–L. An R_L of $R_1:R_2 = 3:2$, 7:3, and 4:1 showed effective voltage regulation only when the input voltage was no less than 6 V, indicating an invalid switch and buck conversion for input voltage ranging from 3 V to 6 V. On the contrary, a ratio of $R_1:R_2 = 9:1$ exhibited effective voltage control with an input voltage larger than 3 V. Thus, $R_1:R_2 = 9:1$ is identified as the optimal component sizing for R_L , confirming conclusions drawn from the simulations.

3.2.3 Passive amplification unit

Three measuring points (MP_1, MP_2, and MP_3) in Figure 2 were selected. MP_3 measures the voltage on a single capacitor, MP_2 measures the voltage on the two series-connected capacitors, and MP_1 measures the voltage on three series-connected capacitors during the charging of the capacitors. Simulation and experimental results of the three MPs are displayed in Figure 8A, where a stable 3 V is observed across each capacitor. Additionally, processed outputs of Topology_1 and 2 are shown in Figures 8B–D. C_{2nd} is measured in Topology_1 and MP_1 is measured in Topology_2. The results indicate that the charge and energy accumulation achieved a 3-fold enhancement within 600s of charging. The experimental and simulation results are in high agreement. However, all the experimental results showed a relatively longer time to reach a stable state compared to the simulation results, which may be due to the nonnegligible energy dissipation in the practical charging experiment.

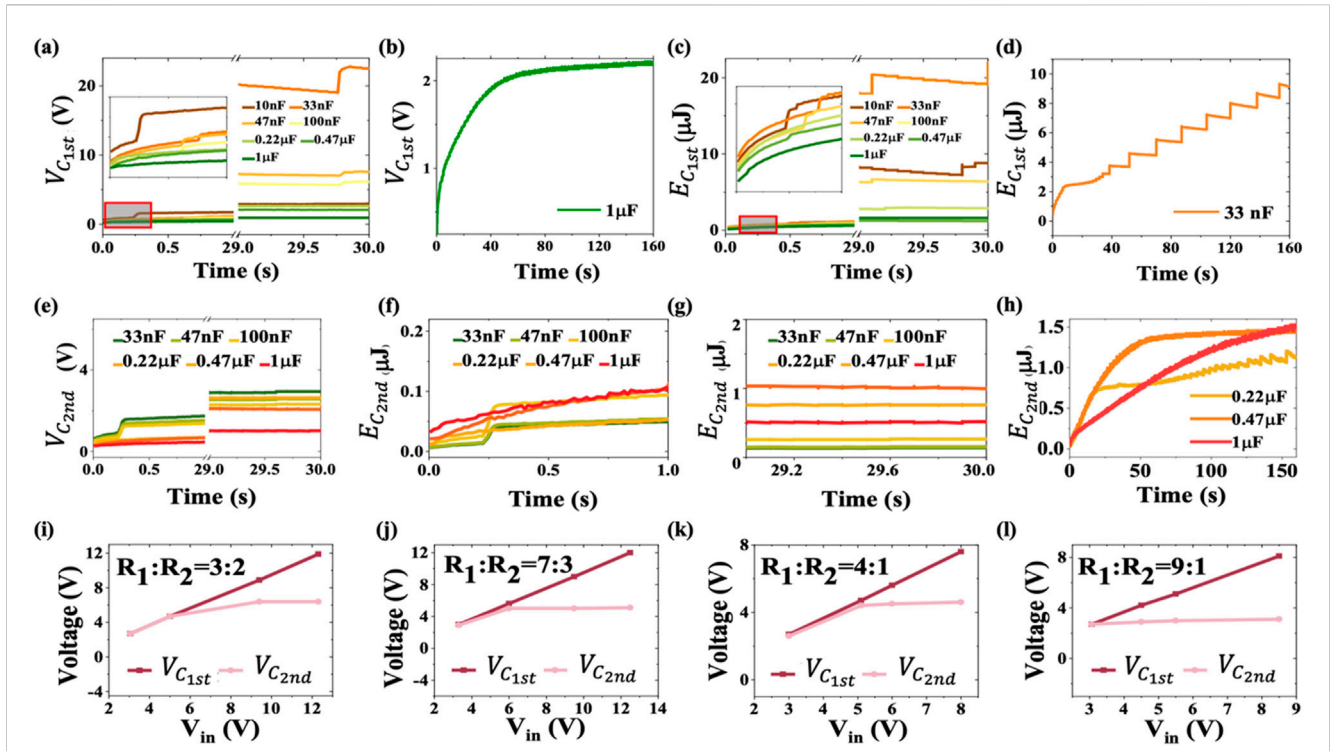


FIGURE 7 Dependence of voltage accumulation ($V_{C_{1st}}$) on time with (A) C_{1st} ranging from 10 nF to 1 μ F, and (B) C_{1st} of 1 μ F; Dependence of energy storage ($E_{C_{1st}}$) on time with (C) C_{1st} ranging from 10 nF to 1 μ F, and (D) C_{1st} of 33 nF; Dependence of voltage accumulation ($V_{C_{2nd}}$) on time with (E) C_{2nd} ranging from 33 nF to 1 μ F; Dependence of energy storage ($E_{C_{2nd}}$) with C_{2nd} ranging from 33 nF to 1 μ F on charging time of (F) 1s, and (G) 30s; (H) Dependence of $E_{C_{2nd}}$ with C_{2nd} ranging from 0.22 μ F to 1 μ F within 160s operation period; (I–L) Dependence of $V_{C_{1st}}$ and $V_{C_{2nd}}$ on V_{input} with different resistive loads.

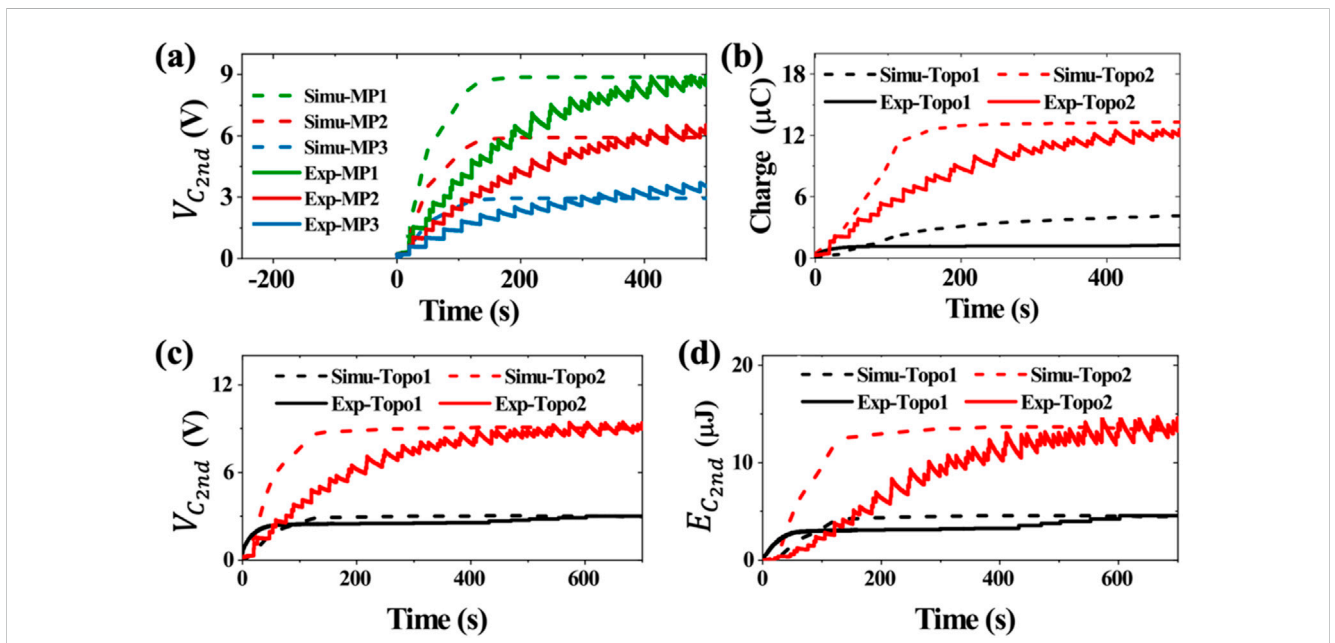


FIGURE 8 Simulation and experimental results of (A) $V_{C_{2nd}}$ on MP1, 2, and 3. The multiple capacitors are charged to 3 V in series; (B) charge accumulation in Topology_1 and Topology_2. Topology_1 shows a considerable energy loss as compared to the simulation result due to the excessive current leakage. The implementation of multiple capacitors in Topology_2 resulted in an enhanced circuit current, leading to a more efficient charge accumulation; (C) $V_{C_{2nd}}$ for Topology_1 and Topology_2; (D) $E_{C_{2nd}}$ for Topology_1 and Topology_2.

3.3 Circuit efficiency calculation

In summary, the optimal parameters of the L-PMC Topology_1 are $C_{1st} = 33 \text{ nF}$, $C_{2nd} = 1 \text{ }\mu\text{F}$, $R_L = 50 \text{ G}\Omega$ with a resistive ratio of 9:1 between R_1 and R_2 . Factors including energy extraction efficiency, energy transfer efficiency, and battery charging efficiency are used to evaluate the L-PMC.

3.3.1 Energy extraction efficiency

The energy extraction efficiency refers to the proportion of energy input on loads from the device, which is determined by the PMC matching. The energy extraction efficiency of Topology_1 is compared with other works in Table 2. With a C_{1st} of 33 nF, a stable $V_{C_{1st}}$ of 60.8 V was obtained after 34 cycles. The $E_{C_{1st}}$ is

TABLE 2 Comparison of energy extraction efficiency with published works.

Published year	Device mode	PMC module	Frequency	Calculation methods	Energy extraction efficiency (%)
2017 (Zi et al., 2017)	SFT-TENG	Motion-triggered switch and capacitors	1 Hz	$\eta = \frac{E_{out}}{E_{in}}$ $E_{out} = \frac{C_E Q_{SC,max}^2}{\left(\frac{Q_{SC,max}}{V_{OC,max}} + C_E\right)^2}$ $E_{in} = \frac{Q_{SC,max}^2}{\frac{Q_{SC,max}}{V_{OC,max}} + C_E}$	23%
2017 (Cheng et al., 2017)	LS-TENG CS-TENG	AC/DC conversion, transmission and LC oscillating units	<2 Hz	$\eta = \frac{E_C}{E_m}$ $E_m = \frac{1}{2} Q_{SC,max} (V_{OC,max} + V'_{max})$	29.6%
2020 (Wu et al., 2020)	CS-TENG	AC/DC conversion, mechanical transmission and control units (LC oscillating circuit)	1 Hz	$\eta = \frac{E_C}{E_m}$ $E_m = \frac{1}{2} Q_{SC,max} (V_{OC,max} + V'_{max})$	37.8%
2021 (Lin et al., 2021)	ES-TENG	AC/DC conversion with RLC	5 Hz	$\eta = \frac{E_{out}}{E_{in}} = \frac{\int I(t)^2 R dt}{mg \Delta h}$	29.7%
2023 (Shan et al., 2023)	CS-TENG S-TENG	Charge excitation with diode and capacitor, and LC oscillating circuit	1 Hz	$E = \int_0^T V I dt = \int_{t=0}^{t=T} V dQ = \oint V dQ$	NA
2024 (Abid et al., 2024)	3-layered CS-TENG	AC/DC conversion, DC/DC buck conversion with passive switching	2–4 Hz	<p>Reduce voltage to increase current, $Q_{SC} = A\sigma x(t) / (d_o + x(t))$, no efficiency calculation involved</p>	NA
This work	CS-TENG	AC/DC conversion, inductor-free buck conversion and two-level capacitor storage units	1 Hz	$\eta = \frac{E_C}{E_m} = \frac{E_C}{E_{TENG}}$ $E_{C_{1st}} = \frac{1}{2} C_{1st} V_{1st}^2$ $E_m = E_{TENG} = \frac{1}{2} Q_{SC,max} (V_{OC,max} + V'_{max})$	42.2%

calculated to be 60.995 mJ using Equation 22. The E_m shows the inherent characteristic of the device, which depends on the maximum surface charge density, open-circuit voltage, and absolute voltage (Wu et al., 2019). The measured $Q_{sc,max}$, $V_{oc,max}$ and V'_{max} are 60.48 nC, 58.85 V and 81.6 V, respectively. Based on the same method, E_m was calculated to be 4.25 mJ per cycle. The much higher energy extraction efficiency of 42.24% was calculated using the same method as prior works in the table (Zi et al., 2017; Cheng et al., 2017). The calculation details are provided in the supporting information (Supplementary Figure S4).

3.3.2 Energy transfer efficiency

Energy transfer efficiency refers to the proportion of energy stored in the second-level capacitor from the energy input on loads (first-level capacitor), which is calculated as 44.05% based on $E_{C_{1st}}$ and $E_{C_{2nd}}$ of Topology_1 using Equation 23. Furthermore, a battery is charged from 1.9 V to 2.4 V within 10 min with the L-PMC Topology_1 (Supplementary Figure S6). With Topology_2, the energy transfer efficiency shows 207% enhancement (from 30.59% to 63.55%), with calculation details presented in the supporting information (Supplementary Figure S5).

4 Conclusion

While the milliwatt output level of low-frequency biomechanical energy harvesters makes them appropriate for sensing application, their high voltage, weak current, and AC output restrict their effectiveness as a direct power source. Conventional RLC circuit limits the energy transfer efficiency in biomechanical energy harvesters due to the extremely low circuit current. In this study, a low-loss power management circuit is studied with a well-matched 2-stage energy transfer strategy to minimize energy losses, leading to a much higher energy extraction efficiency of 42.24% compared with previous studies. Furthermore, using Topology_1, a battery was charged from 1.9 V to 2.4 V in 10 min with an energy transfer efficiency of 30.59%. The integration of passive current amplification using Topology_2, a 3-fold enhancement in charge accumulation and energy storage is achieved and the energy transfer efficiency achieves an enhancement of 207%. This enables the effective use of the device as DC power source through integration with a battery, demonstrating potential for application in new generation self-powered wearable electronics.

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Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material, further inquiries can be directed to the corresponding author.

Author contributions

WL: Conceptualization, Investigation, Methodology, Writing—original draft. YH: Methodology, Writing—original draft. CL: Methodology, Writing—original draft, Formal Analysis. AV: Writing—original draft. WD: Conceptualization, Formal Analysis, Funding acquisition, Project administration, Supervision, Writing—review and editing.

Funding

The author(s) declare that financial support was received for the research, authorship, and/or publication of this article. This study was supported by the National Natural Science Foundation of China (Grant no. 22072125).

Conflict of interest

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Supplementary material

The Supplementary Material for this article can be found online at: <https://www.frontiersin.org/articles/10.3389/felec.2025.1501178/full#supplementary-material>

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