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Compact grounded memristor model with resistorless and tunability features

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This research article provides a circuit illustration of a grounded memristor emulator. An operational transconductance amplifier (OTA) is one of its active components, along with two transistors and one capacitor. With a simple flip of the input ports, the incremental and decremental settings for the proposed memristor may be preserved. With the capacity to function in the megahertz band, the circuit offers a resistorless and controllable feature. Using the Cadence Virtuoso EDA tool in an analog design environment (ADE), PSPICE simulation with 0.18 μm TSMC technology parameter has been used to illustrate the viability of the suggested memristor. It has been confirmed in the simulation section that the operating frequency and tunability responses in the current-voltage (I-V) plane are in reasonable agreement with the theory. The suggested memristor model's resilience has also been tested using process corner, Monte Carlo analysis, and temperature analyses, as well as single and parallel connected structures. The suggested memristor model is simple and does not need additional sub-circuit components, making it appropriate for implementation in integrated circuits. The experimental demonstration has been carried out by making a prototype on a breadboard using ICs, which exhibits good agreement with theoretical and simulation results. Single/parallel combinations of memristor, chaotic oscillator, and high pass filter have been presented to demonstrate its application.

KEYWORDS

current mode circuit, memristor, pinched hysteresis loop (PHL), chaotic oscillator, CMOS technology

1 Introduction

A two-terminal, nonlinear, memory-equipped component is called a memristor. The memristor was deduced as the fourth fundamental circuit component that fills the gap between magnetic flux and the electric charge by Chua (1971) based on symmetrical reasoning. Memristor functions as a resistive device with distinct dynamic properties that may store information by remembering the charge flowing through it, hence justifying its name (resistance with memory). As demonstrated by Chua and Kang (1976), memristor circuits display pinched hysteresis loops (PHL) that have an inverse relationship with frequency in the current-voltage (I–V) plane. Such PHL differs significantly from those of resistors, capacitors, and inductors in terms of their physical characteristics. The amazing development that confirmed the notion put out before was the physical creation of a memristor device in 2008 by the HP research team (Strukov et al., 2008). Researchers from all across the globe are interested in this discovery. The emphasis is now on creating simple and affordable emulator circuits that imitate the characteristics of an ideal memristor due to the difficulties of constructing Nano-scale memristor devices as well as their high

production costs. For the purpose of simulating this novel gadget, there are a few SPICE equivalent models (Rak and Cserey, 2010; Batas and Fiedler, 2011). Researchers are motivated to create simple, inexpensive, and application-specific memristor emulator circuits because memristor and CMOS transistor compatibility (Batas and Fiedler, 2011; Sánchez-López and Aguila-Cuapio, 2017; Babacan et al., 2017; Ranjan R. K. et al., 2019; Ranjan R. K. et al., 2019; Raj et al., 2020; Ayten et al., 2017; Petrović, 2018; Yadav et al., 2020; Bhardwaj and Srivastava, 2021; Yesil et al., 2020; Prasad et al., 2021; Ranjan et al., 2017) encourages them to do so. Several memristor emulator models based on active elements exist, including the second-generation current conveyor (CCII) (Sánchez-López and Aguila-Cuapio, 2017; Ranjan R. K. et al., 2019; Raj et al., 2020), operational transconductance amplifier (OTA) (Babacan et al., 2017; Ranjan R. K. et al., 2019; Raj et al., 2020; Bhardwaj and Srivastava, 2021; Yesil et al., 2020; Prasad et al., 2021), analogue multiplier (Sánchez-López and Aguila-Cuapio, 2017; Babacan et al., 2017; Ayten et al., 2017; Petrović, 2018), current conveyor transconductance amplifier (CCTA) (Ranjan R. K. et al., 2019), differential voltage current conveyor (DVCC) (Bhardwaj and Srivastava, 2021), current feedback transconductance amplifier (CFTA) (Prasad et al., 2021), and differential voltage current conveyor transconductance amplifier (DVCCTA) (Ranjan et al., 2017). Numerous memristor emulator designs reported in (Iu et al., 2014; Kim et al., 2012; Sozen and Cam, 2016; Cam and Sedef, 2017; Yesil et al., 2014; Abuelmatti and Khalifa, 2015; Sánchez López et al., 2015; Sánchez-López and Aguila-Cuapio, 2017) consist of a higher number of passive components along with an increased count of transistors. The article in (Chua, 2013) outlines that memristors may be used in numerous domains, including neurobiology, to study complicated processes. The material provided shows toy memristors that replicate habituation and LTP learning. It also indicates that sodium and potassium ion-channel memristors generate the action potential in the Hodgkin–Huxley equations and address some unsolved oddities. The subject matter explains that neurons and synapses are locally-active and locally-passive memristors. The work in Chua (2022) challenges Hodgkin-Huxley's "time-varying conductance" notion and introduces the "Edge of Chaos Kernel" as nature's best method for establishing an "action potential," or "all-or-none" response. Galvani's 240-year-old enigma on the physical mechanism behind the near-abrupt all-or-none phenomenon is resolved by a precise characterization of excitability. This mechanism involves a global saddle-node bifurcation, where a stable and unstable periodic orbit grow in size and gradually morph into a single orbit. In Pickett et al. (2013) neuristor employing two nanoscale Mott memristors, which display transitory memory and negative differential resistance due to Joule heating-driven insulating-to-conducting phase transitions have been discussed. This neuronal device demonstrates all-or-nothing spiking, signal gain, and different periodic spiking employing materials and topologies suitable for high-density integration with or without silicon transistors. The work in Wu et al. (2024) discusses the only MOS-based memristor design while (Xu et al., 2024) depicts the memristor emulator based on Taylor expansion for the reconfigurable FPGA implementation. The article (Raj and Kumar Ranjan, 2024) discusses the multi-memelements emulator design using the current mode building block.

This work illustrates the grounded memristor concept, which calls for a single active block and a grounded passive element. It functions in both decremental and incremental topologies. It also has features like tunability and resistorless. The suggested memristor model is straightforward and simple to construct as an integrated circuit thanks to all these features. The suggested model does not implement it using either the multiplier or the mutator circuit. The article is structured such that Section 2 discusses the OTA block's brief introduction and the suggested memristor circuit. In this section authors have proposed a novel resistorless grounded memristor emulator circuit, the mathematical analysis is presented along with the frequency analysis and non-ideal, parasitic analysis of the proposed circuit. The suggested emulator is simulated on a computer in Section 3. This part discusses the non-linear properties of the I–V plane and its preformation analysis for different variables. Section 4 deals with the comparative analysis of the presented design with existing literature and the potential application of the proposed circuit has been discussed in Section 5. Section 6 ends with a conclusion to the work.

2 Circuit description and mathematical modelling

An operational transconductance amplifier may be used in place of an operational amplifier in a number of situations. A voltage-regulated current source and a transconductance that produces output current make up the current mode active analog building block known as OTA (g_m). The link between the transconductance parameter and port may be written as Equation 1.

$$I_O = g_m (V_P - V_N), g_m = \frac{k}{\sqrt{2}} (V_B - V_{ss} - 2V_{th}) \quad (1)$$

where k is a MOS device parameter. The OTA receives characteristics for external tunability from VB. OTA's architectural structure and aspect ratio of its MOS transistors (Raj et al., 2020) are shown in Supplementary Figure S1.

2.1 Proposed memristor emulator circuit

A flux-controlled memristor emulator design with 1 OTA and 2 transistors is shown in this section. No resistor is required for the circuit. The typical configuration of a flux-controlled memristor has an initial value of β and an incremental/decremental term α that is roughly represented by $(\beta \pm \alpha\varphi(t))V(t)$, where φ(t) is the time integral of the voltage. In Supplementary Figure S2A, the circuit implementation of the memristor emulator design is shown. One OTA with one PMOS and one NMOS transistor makes up the circuit. Connecting switch S to the OTA's N terminal and P terminal, respectively, will result in incremental and decremental configurations. When considering the memristor's incremental mode of operation, routine analysis reveals that when switch S is connected to the N terminal in incremental configuration, the applied input voltage (V_{IN}) appears at the gate terminal of transistors (M1 and M2) and at the N terminal of the OTA. The output

current of the transconductor stage, which comprises M1 and M2 transistors, can be written as below in Equation 2.

$$I_{OUT1} = g_{m12} V_{IN}(t) \tag{2}$$

where g_{m12} is the transconductance gain of the transconductor stage. This current flows into the capacitor (C) and develops a potential across it which can be written as Equation 3.

$$V_C = V_B = \frac{g_{m12}\phi_{IN}(t)}{C} \tag{3}$$

The voltage (V_B) at the biasing terminal of OTA is the same as the potential across the capacitor shown in Equation 3. Since the circuit is operating in an incremental configuration, the voltage at the N terminal of OTA is the same as the applied input voltage while the P terminal is grounded. The output current of the OTA is the multiplication of the transconductance *(gm)* and N terminal voltage of OTA. This output current of OTA is equal but opposite in direction to that of the applied input current (I_{IN}). The same has been indicated using the arrow in Supplementary Figure S2A and using the port relationship can be written as in Equation 4.

$$I_O = -g_m V_{IN} = -I_{IN} \tag{4}$$

Using Equation 1 and Equation 3, the above equation can be re-written to result in the memductance of the proposed memristor circuit as Equation 5.

$$W(\phi_m) = \frac{I_{IN}}{V_{IN}} = -\frac{k}{\sqrt{2}}(V_{SS} + 2V_{th}) + \frac{k g_{m12}\phi_{IN}}{\sqrt{2}C} \tag{5}$$

The derived memductance expression follows the typical form of flux-controlled memristor, as can be seen from Equation 5 above. Linear time-invariant and linear time-variant components make up the Equation 5. It can be observed from Equation 5 that the memductance depends on the mobility of the carrier in the channel, which is a temperature-dependent parameter. Therefore, the memductance of the proposed design changes due to temperature variation. It can be observed from the equation for the memristance of the HP TiO_2 memristor (Strukov et al., 2008) model depends on the mobility of the oxygen vacancies, which relies on temperature-dependent conductivity. Therefore, the presented memristor emulator design has temperature dependency due to the presence of μn, which is mobility of carrier in the channel while HP TiO_2 memristor has temperature dependency due to the presence of mobility of the oxygen vacancies. Both the memristors have different materials used for their fabrication/implementation. It has also been found through simulation results updated in the revised manuscript that the change in leakage current depends on the operating temperature and its effect on the hysteresis loop can be decreased by using a proportional to absolute temperature (PTAT) biasing voltage source. Flux (φ_{IN}) is the variable parameter in the linear time-variant portion. Additionally, it can be seen that the proposed circuit's memductance has tunability properties, allowing the time-variant portion to be adjusted by altering the transconductance gain of the transconductor stage. The time-variant portion of the memductance and the capacitor have an inverse relationship, which is important. In order to study the frequency domain behavior of the proposed memristor circuit, the sinusoidal signal $V_{in} = A_m Sin(\omega t)$ has been applied. Here A_m and ω are the amplitude and angular frequency ($2\pi f$) respectively. The input flux (φ_{IN}) in terms of the applied sinusoidal signal is computed as $A_m Cos(\omega t - \pi)/\omega$. Substituting the value of φ_{IN} in Equation 5, the memductance can be written as Equation 6.

$$W(\phi_m) = -\frac{k}{\sqrt{2}}(V_{SS} + 2V_{th}) + \frac{k g_{m12} A_m Cos(\omega t - \pi)}{\sqrt{2}\omega C} \tag{6}$$

By looking at the memductance formula in Equation 6, it can be seen that the variable term relies directly on the applied signal's amplitude but inversely on the applied input frequency (ω). In other words, when the memristor's operating frequency increases, the variable component decreases, and the device begins to operate more like a linear resistor. Hence, obey the fingerprint characteristics of a perfect memristor. Additionally, the ratio (λ) between the variable and the fixed component of memductance is provided by Equation 7.

$$\lambda = \frac{g_{m12} A_m Cos(\omega t - \pi)}{-\omega C(V_{SS} + 2V_{th})} \tag{7}$$

The fact that the λ drops as frequency *(ω)* increases and turns into zero for infinite frequency is seen from Equation 7. Memristor loss is thus of a non-linear character. The value of λ must lie between zero and one in order to maintain the non-linear character. Supplementary Figure S2B shows the fully MOS-based resistorless proposed design of the memristor emulator circuit. Here the capacitor C in Supplementary Figure S2A has been implemented using an MOS transistor. The presented memristor emulator circuit has been validated by applying a sinusoidal signal which is a pinched hysteresis loop and square waves which is non-volatile memory. Memristor is still not available as a commercial component due to the cost and technical difficulties in fabricating nano-scale devices. Memristance is a phenomenon observed with nano-scale thin film layer while the presented design uses CMOS technology utilizing analog current mode techniques. Both presented circuit and thin-film have memristance but the origin of it is totally different. In thin film resistors, memristance is due to molecular rearrangement occurring after the application of terminal voltage. In the proposed circuit memristance is realized by the voltage-current relationship of the device with the help of an active element. The memristor emulators can be used in various applications in spite of having mature memristor technology. The presented memristor emulator provides advantageous properties over available emulators. Memristor emulator circuits mimic the distinctive features of genuine memristors by combining passive and active parts. Capacitors are essential for regulating the voltage and current dynamics in a memristor emulator circuit so that it behaves like a real memristor. The memristive hysteresis behavior, which imitates the relationship between charge and flux, is partially produced by the capacitor. The capacitor integrates the current and stores the charge in a resistorless memristor emulator. A MOSFET might enable current to flow into the capacitor depending on the gate voltage, simulating the behavior of a changing resistance. The voltage across the capacitor grows as it charges, but the current flow is regulated by the behavior of the active components.

2.1.1 Charging of the capacitor

The capacitor begins charging as soon as a voltage is introduced into the circuit. The circuit resistance and the applied voltage determine how quickly the battery charges. An integration of the current passing through the capacitor yields the voltage across it. To mimic the memristor's fluctuating resistance over time or with a voltage history, the resistance is often dynamically changed. This charging procedure integrates the current gradually, simulating the memristor's history-dependent behavior, which involves "remembering" the amount of charge that has passed through it. The capacity to store charge contributes to the "pinched" appearance of the hysteresis loop by generating the memory effect.

2.1.2 Discharging of the capacitor

Capacitor discharge begins when input voltage or current is cut off or lowered. The resistance in the circuit affects how quickly this occurs as well. As the voltage across the memristor gradually drops during discharge, the capacitor may simulate the memristor's "forgetting" or "resetting" behavior. This is similar to how, depending on the circuit design, a memristor's resistance can either return to its original state or remain in an altered state. Transistors or other active components may be used in emulator designs to regulate the discharge rate, enabling more accurate simulation of memristive behavior.

Major role of capacitor in Memristor emulator circuit:

1. Charge Storage: The capacitor stores electrical charge, which can be interpreted as the internal state of the memristor.
2. Voltage-Current Relationship: The voltage across the capacitor relates to the current through the circuit, analogous to the charge-flux relationship in a real memristor.

2.2 Non-ideal analysis and parasitic effect

The non-ideal and parasitic impedance behavior at different building block terminals are examined in this part to better understand how transistor mismatch affects the memristor emulator design. The port relationship of the OTA blocks might be shown as follows in the case of tracking faults as shown in Equation 8:

$$I_O = g_m\left(\gamma_1 V_P - \gamma_2 V_N\right) \tag{8}$$

Ideal values for the linked parasitic capacitances and impedances at the input and output terminals of an OTA are zero and infinity, respectively. The parasitic resistances, capacitances, and non-idealities caused by the mismatch of transistors significantly reduce the flux-controlled memristor emulator's overall performance. The parasitic capacitances and resistances are connected in parallel at the P, N, and O terminals of OTA. The parasitic capacitances of the transconductor stage (M1 and M2) are not taken into consideration for the sake of simplicity. The non-ideal gain from the input to the output of the transconductor stage is "α". Considering all these parasitic components and tracking errors, the memductance Equation 5 can be rewritten as

$$W\left(\phi_m\right) = -\frac{k\gamma_2}{\sqrt{2}}\left(V_{SS} + 2V_{th}\right) + \frac{k\alpha\gamma_2 g_{m12}\phi_{IN}}{\sqrt{2}C} \tag{9}$$

Equation 9 demonstrates that tracking errors, non-idealities, and parasitic involvement at higher frequencies may cause the memductance value to deviate from the ideal one. However, at lower frequencies, these values are the less influential.

3 Results and discussion

The Cadence Virtuoso tool was used to assess the suggested memristor emulator circuit using 180 nm TSMC technology with a ± 1.2 V supply voltage in order to correctly verify the existing theory. Section 2 provides a discussion of the MOS structure of the OTA (Raj et al., 2020). The transistors used in the CMOS implementation of OTA are in the saturation region. The selected OTA structure offers 630 phase margins, 2.35 V/μs slew rate, 9.9 MHz UGB, and 89 dB CMRR. The sinusoidal input voltage and input current of a memristor are seen to be in a hysteresis loop. In order to analyze the frequency dependence of the PHL, a sinusoidal input with a 700 mV amplitude at various frequency values has also been added to the circuit. V_B = 0.4 V and C range from 200 pF to 800 pF are the component values used in the simulation. The input frequency often affects the variable parameter, capacitor C. The suggested memristor emulator designs have been subjected to simulation. When exposed to bipolar sinusoidal stimulation, memristor results in a hysteresis curve that is pinched at the origin between the input voltage and input current. Therefore, we utilized a 700 mV sinusoidal wave input at various frequencies to demonstrate the relationship of the proposed memristor circuit in its incremental structure. To demonstrate the hysteresis loops' frequency-dependent character, Supplementary Figure S3 displays them for circuits with sinusoidal input voltage signals at different operating frequencies. The suggested design has an operating frequency range of up to 20 MHz. Like a conventional resistor, the curve progressed towards linearity with rising frequency, and the variable component becomes less as frequency rises. From Supplementary Figure S4, it is clear that the area under the suggested memristor circuit's frequency-dependent pinched curve is inversely related to the capacitor value, which is in accordance with the equations' theoretical predictions (9). The simulation was run for various capacitance values at various frequencies while maintaining the constant relationship between frequency and capacitor (C), as shown in Supplementary Figure S5. The figure demonstrates that because of the fixed value of the frequency capacitor product, all hysteresis curves meet at the same point and resemble one another. By conducting corner analysis, as shown in Supplementary Figure S6A, to evaluate the efficacy of the circuit, the reliability and robustness of the memristor design have been confirmed. Corner analysis involves replicating a circuit or system under both the worst-case and the most likely circumstances. The frequency-dependent PHL curve for the SS, SF, FS, and FF corner analyses is evaluated at room temperature. The difference between the loop areas for the SS and FF process corners, which is smaller in the case of the SS and more in the case of the FF, also shows that the SS process corner has a lower current flow than the FF. A statistical method called Monte Carlo simulation is used to simulate the likelihood of several outcomes in an intrinsically uncertain process. To comprehend how changes in input parameters might

affect a system's output, random sampling and repeated trials are used. Since Monte Carlo simulation does not mimic the actual physical functioning of a circuit, it is not directly connected to circuit simulation. To evaluate the effect of variations and uncertainties on circuit performance, it is often used as a statistical tool in the area of circuit design and analysis. Incorporating Monte Carlo simulation with conventional circuit simulators such as SPICE enables designers to guarantee dependability and resilience in practical scenarios. Small component modifications may have a big impact on performance in analog circuits. Monte Carlo aids in the prediction of these circuits' realistic behavior. By assessing how resistant a circuit design is to changes in environmental parameters (such as temperature or supply voltage fluctuations), Monte Carlo simulation may aid in the optimization of circuit designs. This guarantees that under various circumstances, the circuit will continue to operate within specifications. The setup used for Monte Carlo Simulation is as follows: Beginning with a conventional circuit design, then we entered the nominal values of each component. Values for each component are chosen at random by the Monte Carlo simulation, considering changes in the process, ambient factors, and component tolerances. A predetermined statistical distribution (such as a Gaussian or uniform distribution) is followed when applying these modifications. The circuit simulation is performed many times, using various sets of randomly selected component values each time. Depending on the level of accuracy needed, this might need thousands or even hundreds of runs. The distribution of output parameters is ascertained by statistically analyzing the data of the simulation runs. This helps determine the probability of certain performance outcomes and provides insight into how sensitive the circuit is to alterations in its constituent parts. The performance of the proposed flux controlled memristor emulator has been examined for transistor mismatch at 1 MHz by Monte Carlo Sampling (MCS) simulation for checking the uncertainty and robustness of the designed circuit. MCS simulation has been done for 100 runs by considering random sampling method for mismatch and process statistical variation. MCS simulation has been performed considering the overall process corner and transistor mismatch. It can be observed from Supplementary Figure S6B that the presented memristor is still operational within the acceptable limits even though there is a slight deviation in the pinched hysteresis loop. As illustrated in Supplementary Figure S7, which further examines the impact of temperature fluctuation on the curve, this part deals with the behavior of the memristor emulator, which is having a design that can perform at a broad range of temperatures around 500 kHz frequency. It is shown that the emulator is functional and operational within the set parameters. It is also vital to remember that the current flow in the memristor is improved when temperature levels drop. As shown in Supplementary Figure S8, a simulation study was performed to examine the behavior of the memristor emulator circuit for various input signal amplitudes. It should be noted that the circuit functions well even with an applied signal amplitude of 300 mV. Investigating non-volatility as a crucial circuit property is vital since the memristor is an electrical storage circuit. The proposed memristor is shown to display short-term non-volatile behavior in Supplementary Figure S9 which shows a step-like fluctuation, meaning that there is no memductance change between the pulse inputs that have been applied. Due to the capacitor charge leakage with respect to time, the retention capability of the capacitor will vanish after some time. The emulator design presented performs the short-term non-volatile memory property. In the device level memristor, there is a change in the physical level which provides retention property but in the proposed circuit, we are mimicking the memristor property by storing the charge across the capacitor which has a leakage with respect to time. The nonvolatile switching property of the memristor can be useful for representing long-term adaptation behavior in the memristor-based neuron, the short-term adaptation behavior can also be emulated directly using the same memristor-based circuit due to the volatile switching property of the memristor. By sending a series of pulses to the memristor circuit's input, we were able to achieve and verify the circuit's non-volatility. For the purpose of testing the non-volatility feature, an input pulse signal was applied at the input. This signal had an amplitude of 1 V, a pulse width of 10 ns, and a pulse length of 100 ns at a 500 kHz frequency having a 400 pF capacitance value. It is important to remember that the memductance is non-volatile and changes very little without a pulse. The responses for single memristor and parallel linked memristors are contrasted in Supplementary Figure S10 to demonstrate the memristor-based circuit's resistive character. From the following figure, it can be seen that the resistive character is satisfied by the nonlinear nature, which practically doubles for parallel connections. With the use of commercially accessible off-the-shelf components like the ICs CA3080, the suggested memristor model may be physically realized. The presented flux-controlled memristor emulator circuit utilizing the current-mode approach was built on the breadboard using commercially available ICs CA3080 and IRF840 to experimentally verify the working of the emulator circuit. The experimental results discussed in Supplementary Figure S11 have been obtained using BJT-based commercial IC of OTA and MOS transistors used in Supplementary Figure S2A. The distortions have been observed in the hysteresis loop when the frequency is further increased due to the frequency limitations of the ICs. The prototype circuit made on a breadboard has frequency limitations and it can be noted that the operating bandwidth of the experimental setup is around 2 MHz since these commercial ICs have frequency limitations and parasitic effects due to interconnection. However, it can be observed from Supplementary Figure S3 that at higher frequencies the nature of the pinched hysteresis loop matches with the experimental hysteresis loop obtained in Supplementary Figure S11. The alleviation in the nature of the hysteresis loop between simulation and experimental is because of the change in the technology, i.e., from CMOS of BJT. The gain of the OTA can be adjusted through the passive elements. The proposed memristor emulator is suitable for both CMOS realizations and breadboard implementations. A sinusoidal voltage signal is applied at the input of the emulator circuit to obtain a frequency-dependent pinched hysteresis loop, which is the fingerprints of an ideal memristor. The values for the supply voltages and resistor are chosen as ±12 V, 52 kΩ, and the capacitor value varies with operating frequency. The pinched hysteresis loop in the current voltage plane at different frequencies has been obtained in the digital storage oscilloscope using Keysight - DSOX3054A as shown in Supplementary Figure S11. The experiment has been performed at frequency 800 kHz,

1 MHz, and 1.2 MHz. The distortions have been observed in the hysteresis loop when the frequency is further increased due to the frequency limitations of the ICs. It can be noted that the hysteresis loop becomes deformed, resulting in an asymmetrical behavior due to the tracking errors, parasitic components, and mismatches in the transistors. The loop becomes narrower when the frequency is increased. It can be observed that the pinched hysteresis loop depends on the operating frequency and behaves as a linear resistor when the operating frequency increases validating the theoretical analysis and simulation results. The layout of the circuit has been made as shown in Supplementary Figure S11D to check the impact of parasite on the overall performance of the memristor emulator design. It consumes an effective layout area of 1848 μm^2 (42 $\mu m \times 44 \mu m$).

4 Comparison and discussion

Memristors are a novel technology. Although promising, their fabrication technologies are not as mature, standardized, or scalable as CMOS. However, decades of research make CMOS a dependable and scalable manufacturing platform. CMOS replication lets researchers and designers' study memristive characteristics until memristors become more widely available. Most ICs and digital/analog systems are developed on CMOS platforms, the leading semiconductor fabrication technique. CMOS makes memristive circuits simpler to integrate into designs, tools, and production procedures. Despite its non-volatility and neuromorphic nature, memristors must interact with logic circuits. Replicating memristors in CMOS improves compatibility with logic, memory, and signal processing blocks. In research, many memristive models are theoretical or developing. CMOS circuits can imitate memristors, allowing engineers to study their behavior and build solutions before actual memristor technology matures. Memristors offer quick switching and minimal power, however some technologies have uncontrolled switching, delayed reaction times, or limited durability. A CMOS-based emulation circuit may improve memristive-like switching control. By changing circuit settings, CMOS-based memristor emulators let designers test linear, nonlinear, threshold switching, and other behaviors. In early development, pure memristive devices struggle to attain this versatility. CMOS circuits may emulate memristive behavior to adjust resistance ranges, switching thresholds, and hysteresis profiles for adaptive filters, learning circuits, and non-volatile memory. CMOS-based memristor emulators allow hybrid systems with CMOS and physical memristors. It allows co-integration in future designs when both technologies are mature. Since CMOS technology is widely accessible, duplicating memristive components with it is cost-effective for early prototypes. It lets designers easily construct, test, and improve memristive systems without costly and experimental memristor manufacture. Hybrid systems using actual memristors and CMOS circuits may be created by recreating them. This permits experimental comparisons of actual and simulated behaviors or memory, logic, and neuromorphic computing capabilities enhancements. Memristive devices should provide energy-efficient, high-density non-volatile memory. By recreating memristive behavior using CMOS, researchers may construct power-efficient and high-density storage circuits to prepare for memristive devices. The presented emulator design consists of only 13 transistors. However, several other memristor design using lesser number of transistors are available in the literature but these memristor circuit can only operate in either incremental or decremental configuration which is the demerit of such design. Memristor is still not available as a commercial component due to the cost and technical difficulties in fabricating nano-scale devices. Memristance is a phenomenon observed with nano-scale thin film layer while the presented design uses CMOS technology utilizing analog current mode techniques. Both presented circuit and thin-film have memristance but the origin of it is totally different. In thin film resistors, memristance is due to molecular rearrangement occurring after the application of terminal voltage. In the proposed circuit memristance is realized by the voltage-current relationship of the device with the help of an active element. The memristor emulators can be used in various applications in spite of having mature memristor technology. The presented memristor emulator provides advantageous properties over available emulators. A CMOS-based emulator circuit has been presented because CMOS circuits are used for traditional analog signal, processing as well as in digital circuits. Therefore, interfacing with the existing circuit requires little effort. With integration technology, the proposed emulator can be fabricated on the same chip with other circuits but the real memristor, when memristor technology becomes mature and commercially available, can only be used as a discrete element with other circuits. At the same time, the proposed emulator circuit characteristics can be varied using active and passive parameters and provide the flexibility of tunability. The performance of the presented emulator circuit has been compared with the available existing emulator circuit in literature as shown in Supplementary Table S1 in terms of maximum operating frequency, power supply, number of MOS required, number of passive components, technology used and topology. It can be observed from Supplementary Table S1 that the maximum frequency attained (Iu et al., 2014; Kim et al., 2012; Sozen and Cam, 2016; Cam and Sedef, 2017; Abuelmatti and Khalifa, 2015; Sánchez López et al., 2015; Sánchez López and Aguila Cuapio, 2017) is in Hz and kHz range, MHz range in (Raj et al., 2020; Yesil et al., 2014) but the proposed memristor emulator circuit can operate up to 20 MHz range with less number of transistor count compared to (Raj et al., 2020). The presented emulator circuit has been implemented using both CMOS technology and commercially available BJT based ICs. The emulator circuits presented in (Raj et al., 2020; Iu et al., 2014; Kim et al., 2012; Sozen and Cam, 2016; Cam and Sedef, 2017; Yesil et al., 2014; Abuelmatti and Khalifa, 2015; Sánchez López et al., 2015; Sánchez López and Aguila Cuapio, 2017) consist of more passive components as compared to the proposed memristor emulator circuit. The presented emulator circuit consumes 4.76 mW power. Moreover, the circuit can be used for implementing various analog processing circuit showing its potential application. The emulator circuit designed using commercial BJT based ICs performs well up to 1.2 MHz as shown in Supplementary Figure S11. The distortions have been observed on further increasing the frequency.

5 Applications

5.1 Chua oscillator

The non-linear characteristics of memristor make it eminently suitable for incorporating into chaotic circuits. The memristor-based chaotic circuit is presented by replacing the non-linear element in Chua's circuit with memristor. The simplest electronics circuit that is capable of generating chaos is well known Chua's circuit. Chua's circuit exhibits a wide variety of chaos, hyperchaos, bifurcation phenomena and attractors, thus making it useful in many non-linear dynamic systems. The Chua's oscillator designed using the proposed flux controlled memristor emulator is another application of the circuit. It is designed by replacing Chua's diode with memristor in the Chua's circuit. The circuit implementation for generating Chua's oscillation is shown in Supplementary Figure S12. It consists of one linear resistor, one linear inductor, two linear capacitors and non-linear flux controlled memristor. The dynamics of the circuit is governed by the following set of Equations 10–13:

$$\frac{d\phi}{dt} = V_{C1} \tag{10}$$

$$\frac{dV_{C1}}{dt} = \frac{1}{C_1}\left[\frac{V_{C2} - V_{C1}}{R} - I_M\right] \tag{11}$$

$$\frac{dV_{C2}}{dt} = \frac{1}{C_2}\left[\frac{V_{C1} - V_{C2}}{R} - I_L\right] \tag{12}$$

$$\frac{dI_L}{dt} = \frac{V_{C2}}{L} \tag{13}$$

The values of passive components R, L, C1, and C2 are taken as 2.2 kΩ, 9 mH, 5 nF and 72 nF respectively. The simulated chaotic oscillation outputs VC1 and VC2 for the chaotic circuit are shown in Supplementary Figures S13A, B. Chaotic systems are predictable for a while and then appear to become random. Chaos is a non-linear variation that exists between the realms of periodic and random. At first glance, some chaotic systems may appear regular and periodic whereas others will appear strictly random. After a short interval, the system effectively becomes unpredictable. The plot of simulated response for VC1 versus VC2 is shown in Supplementary Figure S13C. It is the classic chaotic double scroll attractor also known as Chua's attractor. It is a sequence of bifurcations. It is obtained when the value of resistance in the memristor-based chaotic circuit is fixed at 2.2 kΩ. The double scroll attractor looks similar to two Saturn-like rings connected by swirling lines. A sequence of bifurcations can be obtained by varying the resistance value of the memristor-based chaotic circuit. The implementation of Chua's circuit uses the CMOS-based proposed emulator circuit shown in Supplementary Figure S2A. The deformed hysteresis loop will be obtained using the macromodel implementation of the circuit. The experimental results of chaotic oscillation have been included in the updated manuscript in Supplementary Figure S13D to provide a comparison with the simulated result. Chaotic systems are predictable for a while and then appear to become random. Chaos is a non-linear variation that exists between the realms of periodic and random. At first glance, some chaotic systems may appear regular and periodic whereas others will appear strictly random. After a short interval, the system effectively becomes unpredictable.

5.2 High pass filter implementation using proposed memristor

The presented emulator circuit has been utilized to create a memristor-based first-order high-pass filter. In this setup, the resistor in a traditional RC high-pass filter is replaced by a memristor, allowing for a comparison of the filter's characteristics. The design includes incremental and decremental memristors, as illustrated in Supplementary Figures S14A–C. The memductance of the emulator circuit is adjustable, enabling changes in the high-pass filter's characteristics. This feature allows the cut-off frequency of the filter to be varied, which is not possible with a conventional RC circuit. As shown in Equation 6, the memductance of the emulator changes continuously in response to a time-varying signal. So, the memductance will have an average value, which can be denoted by G_{avg}. Due to a sinusoidal signal $V = A_m \sin(2\pi f_m t)$ applied across the memristor emulator, an oscillation of G_m is produced around G_{avg} and can be written as in Equation 14.

$$G_m = G_{avg} \mp \Delta G_m \, Sin\left(2\pi f_m t + \phi\right) \tag{14}$$

Where ΔG_m is the variation due to the applied input signal. Considering only peak values, Equation 11 can be rewritten as Equation 15.

$$G_m = G_{avg} \mp \Delta G_m \tag{15}$$

The value of ΔG_m can be given as Equation 16.

$$\Delta G_m = \frac{kA_m}{2\sqrt{2}\pi f_m RC} \tag{16}$$

Equation 13 indicates that ΔGm is influenced by both the amplitude and frequency of the input signal. Changes in these parameters will alter the value of ΔGm. Therefore, the amplitude, duration of excitation, and frequency of the input signal are key factors in determining the memductance value. The inverse of G_m can be written as Equation 17.

$$R_m = \frac{1}{G_m} = \frac{1}{G_{avg} \mp \Delta G_m} \tag{17}$$

Thus, the cut-off frequency and gain of the filter can be controlled. The cut-off frequency of the memristor-based high-pass filter can be written as Equation 18

$$f_{-3dB} = \frac{1}{2\pi C\left[\frac{1}{G_{avg} \mp \Delta G_m \, Sin\left(2\pi f_m t + \phi\right)}\right]} \tag{18}$$

For the RC-based high-pass filter, the capacitor and resistor values are set to 1 pF and 10 kΩ, respectively. By substituting the resistor with a memristor emulator, both incremental and decremental configurations of the high-pass filter can be realized. Supplementary Figure S4D displays the simulation results of the frequency response for the high-pass filter with an input signal of 0.7 V amplitude. The figure clearly shows that the RC-based and memristor-based high-pass filters, in both configurations, exhibit different cut-off frequencies, which are influenced by the amplitude, frequency, and excitation time of the input signal.

6 Conclusion

This article provides a resistorless, tunable grounded flux-controlled memristor emulator model. One OTA is needed, acting as the active element with two MOS transistors. The whole emulator paradigm is straightforward and attractive. With the OTA input port flipped it works in both setups. Simulator testing was effective in supporting theoretical investigation. Numerous simulations and analyses are conducted to evaluate the proposed circuit's resilience. Its applicability in parallel and series connections is evaluated and satisfactorily confirmed. The performance of the circuit has been verified by simulation and experiment results using commercially available ICs on a breadboard. The total power consumed by the presented emulator circuit is 4.76 mW. Single/parallel combinations, chaotic oscillators, and high pass filters using the presented memristor emulator circuit have been designed to show the potential applications of the proposed emulator circuit.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material, further inquiries can be directed to the corresponding author.

Author contributions

AM: Conceptualization, Data curation, Formal Analysis, Investigation, Methodology, Project administration, Software, Validation, Writing–original draft, Writing–review and editing. AA: Conceptualization, Data curation, Formal Analysis, Investigation, Methodology, Software, Supervision, Writing–review and editing. MA: Conceptualization, Data curation, Formal Analysis, Methodology, Project administration, Software, Supervision, Validation, Writing–review and editing.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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Supplementary material

The Supplementary Material for this article can be found online at: https://www.frontiersin.org/articles/10.3389/felec.2024.1377080/full#supplementary-material

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