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Two-dimensional semiconductors based field-effect transistors: review of major milestones and challenges

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Two-dimensional (2-D) semiconductors are emerging as strong contenders for the future of Angstrom technology nodes. Their potential lies in enhanced device scaling and energy-efficient switching compared to traditional bulk semiconductors like Si, Ge, and III-V compounds. These materials offer significant advantages, particularly in ultra-thin devices with atomic scale thicknesses. Their unique structures enable the creation of one-dimensional nanoribbons and vertical and lateral heterostructures. This versatility in design, coupled with their distinctive properties, paves the way for efficient energy switching in electronic devices. Moreover, 2-D semiconductors offer opportunities for integrating metallic nanoribbons, carbon nanotubes (CNT), and graphene with their 2-D channel materials. This integration helps overcome lithography limitations for gate patterning, allowing the realization of ultra-short gate dimensions. Considering these factors, the potential of 2-D semiconductors in electronics is vast. This concise review focuses on the latest advancements and engineering strategies in 2-D logic devices.

KEYWORDS

field-effect transistors, two-dimensional semiconductors, nanoribbons, metal-contact, Boltzmann's tyranny

Introduction

In 2004, a groundbreaking discovery marked the beginning of a new era in materials science: isolating a single layer of graphite from its bulk form (Novoselov et al., 2004; Novoselov et al., 2005; Novoselov, 2011). This revolutionary achievement led to the emergence of an exciting family of 2-D materials. The remarkable graphene is at the forefront of this family, composed of just a single layer of graphite. Graphene's extraordinary physical and electronic properties have captivated researchers worldwide, making it the most extensively studied 2-D material. Its unique characteristics hold the promise of unlocking a multitude of transformative applications across various fields. From revolutionizing electronics and optoelectronics to advancing biomedical and electrochemical technologies, graphene's potential knows no bounds. This incredible material has opened doors to innovation and sparked a wave of scientific exploration, fueling hopes for a brighter and more technologically advanced future. It has the minimum possible thickness, is the strongest material (~200 times stronger than steel), is an exceptional heat conductor, is almost transparent, lightweight, flexible, and the best electrical conductor at room temperature. The

electrons in this material behave differently than other known materials, manifesting in several fundamental discoveries like Klein tunneling, the half-integer quantum Hall effect, and electrons as massless particles, to name a few. In 2010, the "Nobel Prize" was awarded to Andre Geim and Konstantin Novoselov for this remarkable discovery. A zero band gap in graphene makes it undesirable for logic applications. Different approaches have been used to introduce band gaps in graphene, but they increase the fabrication complexity and reduce the mobility to the level of strained Si (Obradovic et al., 2006; Han et al., 2007; Jiao et al., 2009).

Around 2010, another class of 2-D material was discovered beyond graphene, known as transition metal dichalcogenides (TMDCs) (Mak et al., 2010; Splendiani et al., 2010). Unlike semi-metallic graphene, they are semiconductors with moderate bandgaps, which open other application fields like logic devices. MoS_2, a member of the TMDCs family, has a band gap ~ 1.8 eV, which is satisfactory for logic switches to discriminate between two logic states sharply. Also, combining a low dielectric constant (ϵ_{ch}) and the ability to grow atomic layers within channels (t_{ch} = # of layers × thickness of monolayer) results in a reduced characteristic length ($\lambda \propto \sqrt{t_{ch} t_{ox} (\epsilon_{ch}/\epsilon_{ox})}$), where t_{ox} is the gate oxide thickness and ϵ_{ox} is the dielectric constant of gate oxide. This reduction signifies effective control over short-channel effects, improving device performance (Chhowalla et al., 2016; Kanungo et al., 2022). For the first time, a group of researchers at EPFL, Lausanne (Switzerland), published a paper in *Nature Nanotechnology* on January 2011, demonstrating the monolayer MoS_2 transistor (Radisavljevic et al., 2011; Kis, 2021). In this, the monolayer MoS_2 is exfoliated using the scotch-tape micromechanical cleavage technique. This work gave momentum to the field of 2-D materials in logic electronics. Furthermore, several works demonstrated the electrical properties investigation of transistors based on MoS_2 and other members of the TMDCs family and logic operation based on these devices (Liu et al., 2012a; Liu et al., 2012b; Fang et al., 2012; Huang et al., 2012; Kim et al., 2012; Lin et al., 2012; Wang et al., 2012). Beyond TMDCs, other semiconductors from the 2-D family have shown promising performance, viz. BP, pentagonal $PdSe_2$, InSe, $HfSe_2$, $ZrSe_2$, Bi_2O_2Se, and $MoSi_2N_4$, to name a few promising materials, in aspects of logic devices. Initial results were obtained using mono- or few-layer flake exfoliated from bulk crystal using scotch tape micromechanical cleavage and lithium intercalation, to name a few, also known as the top-down approach. These are nice and simple ways to find new layered materials and study their properties. Nevertheless, these methods cannot produce large-area 2-D materials unsuitable for manufacturable technology.

The crystallinity, purity, large-area growth, and thickness controllability of the grown 2-D channel material are essential for manufacturable device technology. For 2-D channel material growth, these targets must be fulfilled for industrialization. For large-area production, different methods have been used; promising ones are chemical vapor deposition (CVD) (Li et al., 2017; Lin et al., 2017), metal-organic chemical vapor deposition (MOCVD) (Lee et al., 2020; Maxey et al., 2022), liquid-phase exfoliation Shen et al., 2015; Coleman et al., 2011), epitaxial growth (Dong et al., 2020; Dong et al., 2022), and molecular beam epitaxy (MBE) (Cheng et al., 2020), to name a few. CVD is a widely used method to grow high-quality 2D materials. It allows scalability and is suitable for large-area growth, making it essential for industrial applications, but it requires precise temperature and pressure control. MOCVD is a variation of CVD that uses metal-organic precursors to grow 2-D materials. It offers reasonable control over film thickness and uniformity. MBE is a precise technique where atoms or molecules are deposited on a substrate to create thin films layer by layer. While it allows excellent control over layer thickness and composition, it is generally more complex and expensive than CVD. Epitaxy involves growing a crystalline film on a single-crystal substrate, producing high-quality, uniform 2-D layers.

Over the last decade, tremendous progress has been made in logic devices based on 2-D materials (see Figure 1). These include wafer-scale production of single-crystalline 2-D semiconductors and fabrication of logic devices at large scale, high-quality and ultralow-resistance metal contact to 2-D semiconducting channels, high-quality integration of 2-D channels with high-k oxides, demonstration of state-of-the-art devices on a wafer scale, breaking Boltzmann's tyranny using the exotic and versatile $E - k$ dispersion of 2-D materials, alleviation of the lithography limitations on gate patterning, and facilitation of ultra-short gate dimensions using CNTs, graphene, and metallic nanowires, to name a few. Several reports have been presented, discussing: i) the critical performance metrics for aggressively scaled 2-D transistors, offering their extraction and reporting guidelines (Das et al., 2021), materials preparation (Liu et al., 2017), electrical characterization Mitta et al. (2020), and ii) the promising potential of 2-D FETs in very large scale integration (VLSI) design (Fiori et al., 2014; Dorow et al., 2022; Knobloch et al., 2023; Naylor et al., 2023; Sheng et al., 2023). Here, we discuss the family of 2-D materials from the perspective of device design, recent developments to improve the performance of 2-D logic devices, and the unique features facilitated by 2-D semiconductors.

Nanoelectronics-specific applications of the 2-D family

The versatile family of 2-D materials offers a broad spectrum of material properties, ranging from metallic and semi-metallic to semiconductor, insulator, topological insulator, ferroelectric, magnetic, and superconducting properties (Liu et al., 2016; Qi et al., 2021; Zhang et al., 2022a; Elahi et al., 2022). This extensive array of 2-D materials with customizable characteristics opens the door to atomic-scale heterogeneous integration. This, in turn, allows for the creation of innovative hybrid structures that showcase novel physical phenomena and provide unique functionalities (Geim and Grigorieva, 2013; Novoselov et al., 2016; Jie et al., 2018; Ghiasi et al., 2019). One can find a suitable material for integrated circuit applications within this diverse family. Figure 2 provides a glimpse of some nanoscale device applications employing materials from this class. In the following sections, we will explore the essential properties pertinent to front-end devices.

Milestones in the development of 2-D materials based logic electronics

Metal contacts on 2-D semiconductors

Since doping foreign atoms into 2-D semiconductors is difficult and problematic because of the high probability of causing damage, source and drain electrodes' work function is engineered to inject carries into a 2-D semiconductor channel. So, contact with these ultra-thin semiconductors is vital for harvesting their potential. During the

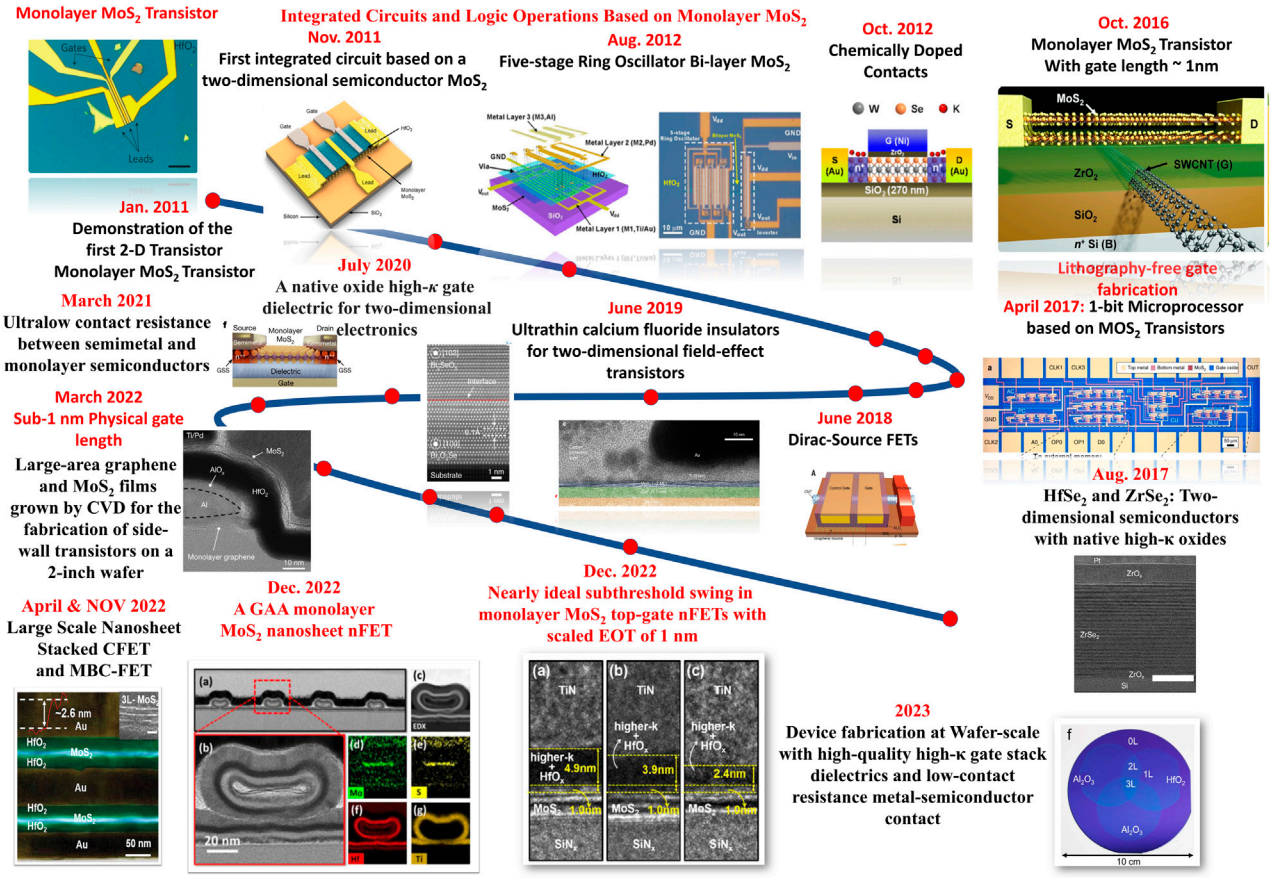

FIGURE 1
Major Milestones in the Development of 2-D Logic Devices: In 2011, a research breakthrough emerged from EPFL as they showcased the inaugural transistor utilizing monolayer MoS_2. Following this milestone, subsequent years witnessed a series of demonstrations involving transistors crafted from transition metal dichalcogenides (TMDCs). The primary thrust was to enhance their performance while delving into integrated circuits built upon these materials. However, a notable stumbling block in this journey was achieving large-scale, single-crystalline growth and favorable interface properties with high-k oxides and metallic contacts. Over the past few years, commendable strides have been taken to overcome these hurdles, resulting in successful demonstrations that validate the progress made in tackling these significant issues.

initial years of development, reliable n-and p-type contacts have not been made to these ultra-thin semiconductors as direct metal deposition leads to interface defects and defects in the semiconductors. These undesirable effects pin the Fermi-level, and theoretically expected Schottky–Mott model (Mott, 1939; Schottky, 1939) results are not observed experimentally (Liu et al., 2018; Mleczko et al., 2019). For example, it is expected theoretically that Ag and Ti will work as n-type contact to $MoTe_2$ and Ni, Au, and Pt will act as p-type contact. However, due to Fermi-level pinning (FLP) resulting from defects, the n-type contact is observed for all the metals with pinning factor (S) ~ 0.06 (Mleczko et al., 2019). This value for S is almost close to pinned materials (S = 0). However, the ideal case is S = 1, which means ideal charge neutrality. Different strategies have been used to eliminate these defects and deepen the Fermi level. Prominent approaches include side metallic contact, use of hBN as a buffer layer over 2-D (Lizzit et al., 2022), ultraclean Ohmic vdW contacts (Boandoh et al., 2018; Wang et al., 2019; Kim et al., 2021; Jang et al., 2022; Wang and Chhowalla, 2022), different phases of 2-D material (Jiang et al., 2023), local doping, mechanical transfer of metal over 2-D (Liu et al., 2018), and semi-metallic contact (Chou et al., 2021; Shen et al., 2021; Jiang et al., 2023; Li et al., 2023; Wang et al., 2023), to name a few. The performance metrics of 2-D based FETs (fabricated devices) are plotted in Figure 3 for $L_G \leq 50$ nm. The best performance is achieved in InSe FET with semimetallic Y-InSe contact.

Except for semi-metallic contact, other methods to decouple the metal-semiconductor interaction result in R_C in the order of kΩ μm, which is one order higher than R_C in Si-metal (Chhowalla et al., 2016). Also, local doping and mechanical transfer strategies are technologically challenging. However, the significant tunneling barrier in vdW contacts results in high R_C, in the order of kΩ. Alternatively, semi-metallic contact with 2-D semiconductors suppresses metal-induced gap states (MIGS), resulting in gap state saturation (GSS) and Schottky barrier-free interface with ultralow R_C, approaching the quantum limit. The devices with semi-metallic contact can potentially deliver performance for future Å technology nodes.

Insulator for 2-D electronics

Integrating channel material and scalable gate insulators with a high-quality interface, i.e., low defect density, is a stringent

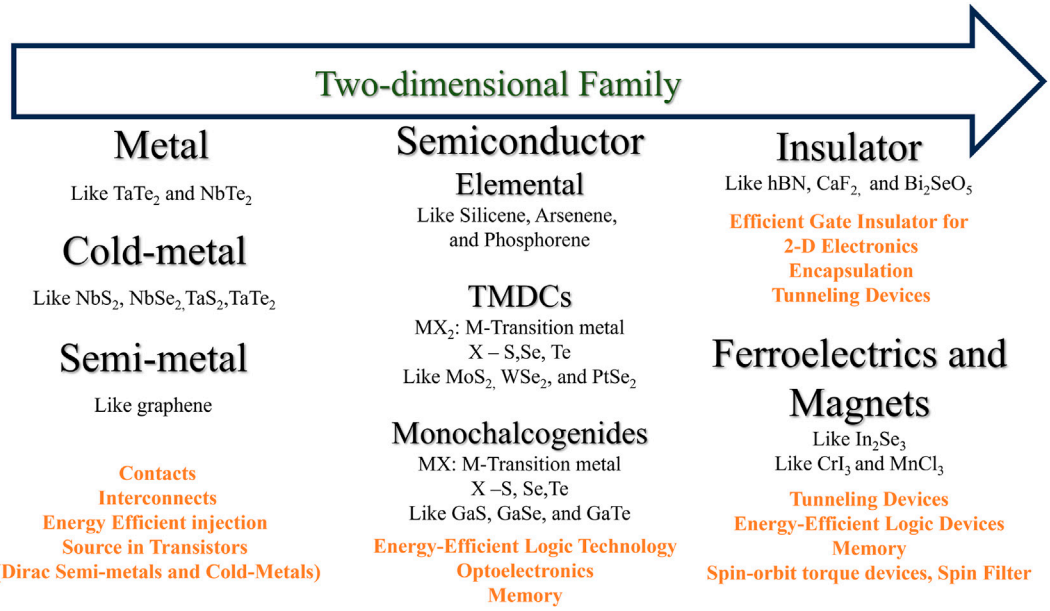

FIGURE 2
The 2-D material family encompasses a wide range of unique properties, each with its own set of applications when viewed through the lens of nanoscale devices.

requirement in the semiconductor industry. Defects lead to undesirable effects in metal-oxide-semiconductor field-effect transistors (MOSFETs) and distort the characteristics, viz. charge trapping and de-trapping, bias temperature instabilities (BTI) (contributed by charge de-trapping), and mobility degradation (coulomb scattering due to trapped oxide charge), to name a few. Si technology is blessed due to the availability of a native oxide with a low defect density SiO_2, also integrated with high-*k* insulators (like HfO_2) with SiO_2 as an interfacial layer using atomic layer deposition (ALD) (Green et al., 2001). However, this integration technique is not suitable in the case of 2-D materials due to its natural van der Waals (vdW) bonding in out-of-plane directions, which results in poor interfacial properties if one deposits oxides using ALD (Lemme et al., 2007). Surface treatments, like rapid thermal annealing (RTA), could reduce defects. Still, the defect density is high after surface treatments, which deteriorates the device's performance. Another way is to use a molecular seeding layer of thickness ~ 0.3 nm to grow HfO_2 using ALD, resulting in uniform HfO_2 with a minimum thickness of ~ 1.5 nm (Li et al., 2019). The molecular seeding layer's thickness is insufficient to block charge trapping due to oxide defects.

The widely known 2-D vdW insulator, hBN, has been used and shown ultra-clean interface with 2-D semiconductors. However, higher leakage and non-scalable process make the sub-1 nm EOT integration in 2-D electronics unsuitable (Britnell et al., 2012; Knobloch et al., 2021). Another crystalline insulator, CaF_2, has been shown to have good interface quality and scalable down to 0.9 nm EOT (Illarionov et al., 2020). It is a good gate insulator for 2-D electronics. High-*k* native oxide, $Bi_2O_2Se_5$, has been synthesized by layer-by-layer oxidation of Bi_2O_2Se, a high-mobility 2-D semiconductor with outstanding stability and excellent mechanical properties, and suitable for sub-0.5 nm EOT electronics (Li et al., 2020; Zhang et al., 2022b; Zhang et al., 2023). Recently, LaoBr, a rare earth oxyhalide, was synthesized with a static dielectric constant of ~ 9 and a band gap of ~ 5.3 eV. Also, it can be integrated with 2-D channels with low defect density for high-performance applications (Söll et al., 2023).

Sub-1 nm gate length: lithography-free process

Recent experimental reports demonstrate the feasibility of lithography-free ultra-short gate length in 2-D FETs, gated with core/shell nanowire with a minimum diameter of 6 nm (Cao et al., 2016), CNT with the physical gate length of ~ 1 nm (Desai et al., 2016), and graphene with a physical gate length of ~ 0.34 nm (Wu et al., 2022). The core/shell nanowire gating enables the direct growth of dielectrics on 2-D materials, which can aid in preserving the pristine character of the 2-D channel and its exceptional properties. CNT-gated devices exhibit excellent switching characteristics with an ideal subthreshold swing of ~ 65 mV/dec and an ON/OFF current ratio of ~ 10^6. The vertical MoS_2 channel transistor, gated using the edge of 2-D graphene, shows ON/OFF ratios up to 10^5 and subthreshold swing values down to 117 mV/decade. This device is fabricated on a wafer scale of 2 inches.

Breaking Boltzmann tyranny/energy-efficient switching: originating from intrinsic properties of 2-D materials

Overcoming Boltzmann's tyranny is indeed a significant challenge in designing ultralow-power transistors. The concept refers to the fundamental limit imposed by thermal energy (kT)

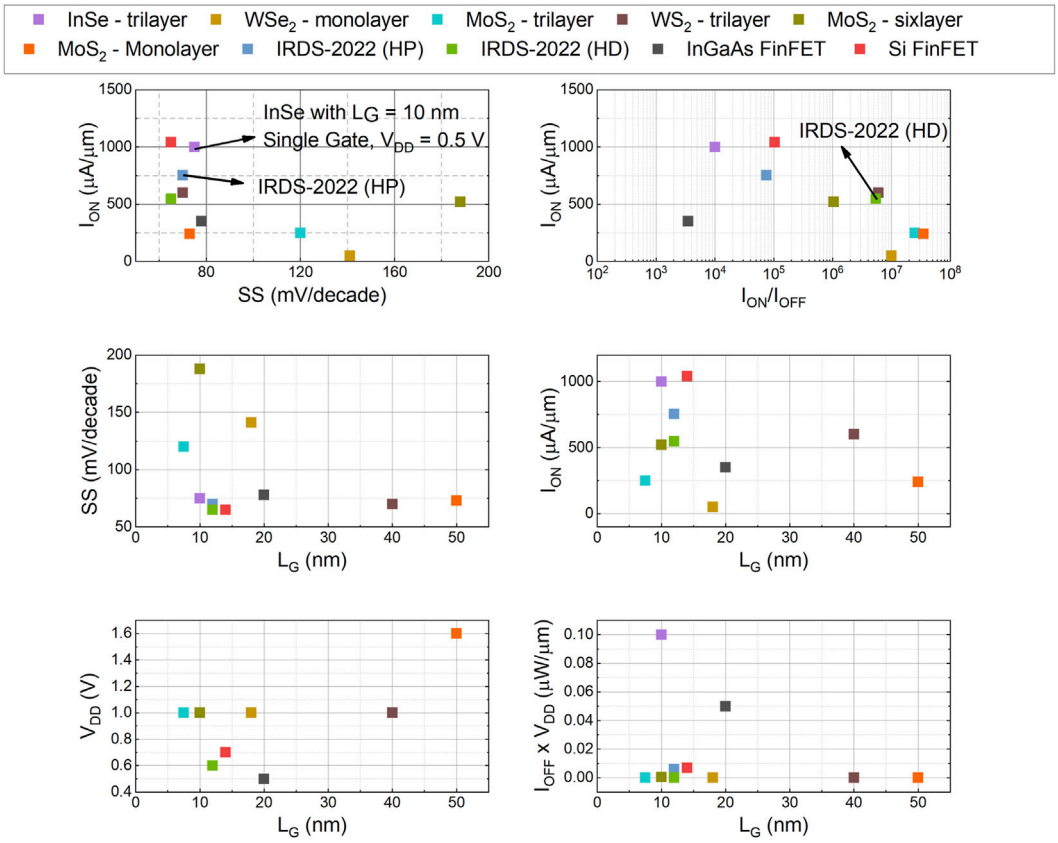

FIGURE 3
Comparision of performance metrics for 2-D based FETs with $L_G \leq 50$ nm (Natarajan et al., 2014; Yang et al., 2015; Nourbakhsh et al., 2016; Convertino et al., 2018; Zhu et al., 2018; Pang et al., 2020; O'Brien et al., 2021a; IRDS, 2021; Jiang et al., 2023). Metrics for IRDS expectation for 2037, Si FinFET, and InGaAs FinFET are also plotted for comparison.

at room temperature, which sets a lower bound on traditional transistors' subthreshold swing (SS). The subthreshold swing is related to the steepness of the current-voltage curve and directly impacts the transistors' energy efficiency and power consumption. Two strategies have been explored to address this challenge: tunnel FETs (Appenzeller et al., 2004; Zhang et al., 2006; Nagavarapu et al., 2008) and Landau FETs (Salahuddin and Datta, 2008; Salvatore et al., 2008; Rusu et al., 2010). Tunnel FETs leverage quantum tunneling for carrier transport instead of traditional thermionic emission. By using a thin tunneling barrier, they can achieve steeper switching behavior, leading to lower SS and reduced power consumption. However, TFETs suffer from a limitation in the ON-state current due to the nature of tunneling transport. This restriction makes achieving sufficiently high current levels for practical applications challenging. Landau FETs rely on increasing the barrier height's steepness with the application of gate voltages. This approach can potentially reduce the subthreshold swing and allow for ultralow-power operation. However, significant technological challenges are associated with Landau FETs, both at the material and device levels. One major issue is achieving low hysteresis while maintaining the required ON-state current (Lee et al., 2015; Li et al., 2015; Khan et al., 2016; Si et al., 2018). Hysteresis refers to the dependence of the transistor's behavior on its history, and excessive hysteresis can negatively affect device performance and reliability.

The intrinsic exotic *E-k* dispersion in 2-D materials and their heterostructures offers alternative solutions to overcome Boltzmann's tyranny in conventional FETs with 2-D materials as channel (Qiu et al., 2018; Liu et al., 2020a; Nadeem et al., 2021a; Liu et al., 2021; Tang et al., 2021). Below, the physical concepts of these devices are briefly described.

Dirac-source (DS)-FETs: Dirac materials, like graphene, as source in FETs

The carrier density decays sub-exponentially and exponentially with infinity thermal tail in conventional source FETs comprised of 3-D (like Si, Ge, III-V) and 2-D (like MoS_2, $MoSi_2N_4$) semiconductors, respectively. Therefore, the SS is limited to ≥60 mV/decade at room temperature. However, the carrier density decays superexponentially in graphene and cuts down the infinite thermal tail, owing to linear dispersion *E-k* and Dirsc point in graphene. As a result, the FETs with graphene sources overcome Boltzmann's tyranny and facilitate energy-efficient switching.

For the first time, in 2018, a group of researchers from China and Canada demonstrated the concept of DS-FETs by integrating graphene in a source of CNT-FET (Qiu et al., 2018). Unlike

negative capacitance FETs, the reported device shows negligible hysteresis and meets the desired performance metrics for sub-60 mV/decade devices. The I_{60} lies in the range 1–40 $\mu A/\mu m$ and SS < 60 mV/decade for more than four decades of change in drain current. The reported devices are desirable for low-power applications and better than other reported sub-60 mV/decade devices (like tunnel FETs and negative capacitance FETs). This device shows I_{ON}, same as Intel 14 nm technology at lower V_{DD} with an average SS of 50 mV/decade.

In principle, graphene/2-D semiconductors hetero-bilayers can show sub-60 mV/decade characteristics. Other reported system is graphene-MoS_2 hetero-bilayer in conventional device structure (Liu et al., 2020b; Liu et al., 2021), state-of-the-art (GAA) device structure (Tang et al., 2021), and diode (Myeong et al., 2022). Graphene/MoS_2 device shows $I_{60} > 1\ \mu A/\mu m$ with sub-60 SS over more than thee decades of drain current. In GAA structure, improved switching characteristics and 40% enhanced ON-state current. The diode based on graphene has shown a sub-unity ideality factor over more than four decades of change in current with a minimum ideality factor of 0.8 and rectification ratio > 10^8.

Topological FETs

The bandgap can be tuned in topological materials by applying a vertical electric field. Alternatively, the conduction is enabled by applying a vertical electric field due to quantum spin Hall effects resulting from Rashba spin-orbit interaction (Vergniory et al., 2019; Kumar et al., 2020; Gilbert, 2021). Recently, it has been shown that by using 2-D topological insulators as channels in conventional FETs, the incompressible limit on SS at room temperature can be overcome, and SS could be lowered by > 25% more than Boltzmann's limit at room temperature (Nadeem et al., 2021b).

All the above demonstrations are paving the path toward low-power electronic circuits.

Wafer-scale demonstration of 2-D fin field-effect transistors, multibridge-channel field-effect transistors (MBC-FETs) and complementary field-effect transistors (C-FETs)

The current mainstream device architecture, FinFETs, has taken us far in terms of CMOS scaling, but as we venture into sub-5 nm territory, we confront new challenges. The quest for enhanced performance, energy efficiency, and integration density necessitates the exploration of alternative materials and designs that can overcome the issues posed by ultrathin Si fin-oxide heterostructures. In pursuit of next-generation logic devices offering higher integration density and lower power consumption, researchers have achieved a significant milestone: developing TMDC FinFETs with fin widths of less than 1 nm. These ultra-thin fins exhibit an impressive ON-to-OFF current ratio of approximately 10^7, making them promising candidates for advanced semiconductor technology (Chen et al., 2020).

Recently, vertically aligned arrays of 2-D fin-oxide heterostructures have been demonstrated, ushering in a new era of 3-D architectural design (Tan et al., 2023). This cutting-edge method involves using epitaxial integration to combine two important parts: a high-mobility 2-D semiconductor material, like B_2O_2Se, and a single-crystal high-k gate oxide, like Bi_2SeO_5. These 2-D fin-oxide epitaxial heterostructures with atomically smooth interfaces and remarkably thin fin thickness can be whittled down to just one unit cell, measuring a mere 1.2 nm. This groundbreaking achievement empowers the large-scale, precisely targeted growth of high-density arrays, all with a consistent orientation. These devices achieve electron mobility levels of up to 270 $cm^2/(V\text{-}s)$, signifying the rapid movement of charge carriers. For 400 nm channel length, with off-state currents as low as approximately 1 pA/μm, they demonstrate minimal leakage when in the off-state with a high ON-to-OFF ratio (10^8) and high ON-state current 830 μA/μm. These performance metrics align with the low-power specifications projected by the International Roadmap for Devices and Systems (IRDS) (IRDS, 2021), making them highly suitable for low-power applications. Developing these 2-D fin-oxide epitaxial heterostructures paves the way for exciting opportunities in advancing semiconductor technology, potentially extending the boundaries of Moore's law.

The GAA nanosheet structures, also known as MBC, are contenders for sub-3 nm technology nodes owing to superior gate control, better area scaling, and large drive current per footprint. With Si nanosheet, the thickness cannot be scaled below 5 nm, and excessive leakage with large number nanosheet stacking. It has been demonstrated that the channel thickness in MoS_2 nanosheet FETs can be scaled down to a thickness of monolayer ~ 0.7 nm with L_G ~ 40 nm (Chung et al., 2022). The device is nearly free from DIBL with I_{ON} ~ 410 μA/μm at V_{DS} = 1 V.

Nearly ideal SS ~ 60 mV/decade at room temperature has been demonstrated in two stacked multilayers MoS_2 MBC-FET of channel thickness ~ 2 nm with I_{ON}/I_{OFF} ~ 4 × 10^8. The current density in this device exceeds the recently demonstrated seven stacked Si MBC-FETs (Huang et al., 2021). Two vertically stacked MBC-FETs have been shown with three monolayer thick MoS_2 channels on wafer-scale (Xia et al., 2022). Also, NAND and NOR logic circuits comprised of two vertically stacked channels have been fabricated on wafer-scale (Xia et al., 2022).

Vertically stacked MoS_2 n-type nanosheet FET and WSe_2 p-type nanosheet, also known as C-FETs, has been demonstrated on wafer scale (Liu et al., 2023), as possible device configuration for sub-1 nm technology node. Statistical data of devices indicates excellent uniformity, desirable for large-scale applications (Liu et al., 2023). Also, C-FETs based on MoS_2 n-type FET and $MoTe_2$ p-type have been demonstrated on wafer scale for large-scale applications (Xia et al., 2022).

Monolithic integration of 2-D FETs and Si FinFETs

The fabrication of a monolithic 3-D CMOS inverter with a vertically integrated p-type Si FinFET and an n-type MoS_2 FET represents a significant achievement in semiconductor technology (Guan et al., 2023). It combines a p-type silicon FinFET with a 20 nm fin width and an n-type molybdenum disulfide (MoS_2) FET. To accomplish this integration, a sequence of low-temperature processes was strategically employed. Both the p-type Si FinFET and the n-type MoS_2 FET demonstrated comparable on/off current

ratios and on-currents. This indicates that they exhibit compatible performance, which is essential for CMOS technology. It achieved a maximum voltage gain of approximately 38.

Challenges

Numerous factors drive the evolution of technology, from its initial discovery to its eventual commercial production. The foremost criterion is its ability to outperform existing technologies. However, the challenges specific to that technology heavily influence the trajectory from discovery to commercialization. Take, for instance, the realm of 2-D semiconductors. These hold exceptional promise for logic device applications, boasting capabilities beyond current technologies. Nonetheless, their journey to fruition requires the development of cost-effective and scalable manufacturing processes—a pivotal requirement for widespread adoption. Several vital considerations underscore the advancement of 2-D semiconductor technology:

Large-Scale Synthesis: Achieving a scalable and reproducible synthesis of high-quality 2-D materials across expansive surfaces presents an ongoing challenge. Ensuring uniformity and consistent properties across a substrate is imperative for practical, real-world applications.

Disorder in FETs based on 2-D materials and their Heterostructures: To unleash the full potential of 2-D channel materials in electronic devices, we must prioritize high-quality 2-D channels, gate stacks, and reliable metal contacts. Simultaneously, addressing sources of disorder is crucial to maintaining material properties and device performance. Poor gate stack quality can introduce mid-band-gap interface states in 2-D materials, significantly hampering device sub-threshold characteristics. Solutions include using crystalline insulators like hBN or CaF_2 with vdW interaction or integrating native oxide to reduce these states. Suboptimal metal contacts can cause mid-gap states and FLP, affecting devices' Schottky barrier height (SBH) tunability and carrier injection control. These could be minimized through semimetallic contacts or buffer layers, making vdW stacking possible.

Heterostructures present exciting opportunities for advanced electronics but also have notable challenges. Engineering interfaces between different 2-D materials with varying properties can be challenging, as defects and misalignment can degrade device performance. Aligning electronic band structures in heterostructures is essential but complex. Achieving low-resistance electrical contacts in 2-D materials, especially in heterostructures, can be difficult. Carrier tunneling due to vdW gaps between layers poses a challenge. Scalability for high-density integration, thermal management, materials integration, device variability, stability, and optoelectronic integration also demand attention. Overcoming these challenges requires ongoing research to harness the potential of heterostructured 2-D FETs in future electronics.

Standardized Performance Metrics: Establishing standardized methods for characterizing and benchmarking the performance of 2-D electronic devices is paramount. Such metrics facilitate meaningful comparisons and catalyze progress within the field.

Long-Term Reliability: A critical concern pertains to the long-term reliability and operational lifespan of 2-D electronic devices, especially under diverse and changing conditions. Ensuring sustained functionality over time is a crucial aspect of technology maturation.

Benchmarking and Comparison: Reiterating the significance, standardized methods for characterizing and benchmarking performance are essential. They serve as a cornerstone for enabling effective comparisons among various 2-D electronic devices and thus propelling the field forward.

Stable Interfaces and Electrical Contacts: A pivotal factor for successful commercialization revolves around achieving low-resistance electrical contacts and stable interfaces between 2-D materials on a large scale. This stability is a linchpin for seamlessly integrating 2-D materials into practical applications.

In summation, the evolution of 2-D semiconductor technology hinges on surmounting multifaceted challenges. By establishing scalable manufacturing processes, standardized performance metrics, and robust interfaces, the pathway to widespread adoption becomes increasingly viable. As these challenges are met and overcome, the potential for 2-D semiconductors to reshape the technological landscape comes one step closer to realization.

Conclusion

Much research is being conducted on novel device architecture and alternate channel materials to discover a feasible solution for sub-3 nm nodes. On the geometry front, nanowire and nanosheet FETs are being investigated. These topologies exhibit exceptional electrostatic control and a relatively simple production method compared to previous technology. Regarding alternative channel materials, 2-D semiconductors are intriguing because of their atomic-scale thinness, bond-free interfaces, and quick turn-on of the density of states near band boundaries. This makes them promising candidates for future technology nodes. This mini-review presents the recent progress in logic devices based on two-dimensional semiconductors.

The field of logic devices based on 2-D materials has witnessed tremendous progress over the last decade. The demonstrated devices using 2-D channel material primarily involve planar architecture. Currently, one of the better planar FET is InSe FET (Jiang et al., 2023) with the ultra-scaled channel of 10 nm length, ultra-low contact resistance (~62 Ω-μm), and low-power supply, V_{DD}, of 0.5 V. Ideal performance is observed with ballisticity ~ 83%, SS ~ 75 mV/dec., DIBL ~ 22 mV/V, and ON-state current > 10^3 μA/μm. In recent years, state-of-the-art device architecture such as FinFETs (Chen et al., 2020; Tan et al., 2023), MBC-FETs (Chung et al., 2022), and C-FETs (Dorow et al., 2021; O'Brien et al., 2021b) with 2-D channel materials have been demonstrated. The nearly ideal electrostatic control in MBC-FET based on monolayer MoS_2 has been demonstrated. In stacked MBC-FETs, 2-D materials facilitate improved scaling and power metrics (O'Brien et al., 2021b).

In the current landscape of 2-D device technology, significant progress has been made in integrating 2-D materials into various aspects of integrated circuits despite ongoing challenges at the device level. Developing synthesis and fabrication methods compatible with industrial processes is crucial to fully unlock the potential of 2-D devices in the electronics industry. Encouragingly, major semiconductor giants like the Taiwan Semiconductor Manufacturing Company (TSMC) are heavily investing in

research to explore incorporating 2-D materials. While silicon will undoubtedly remain essential for the foreseeable future, the prospect of commercial electronics built upon 2-D materials may be closer than anticipated.

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