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Engineering Bilayer AlO_x /$YAlO_x$ Dielectric Stacks for Hysteresis-Free Switching in Solution-Processed Metal-Oxide Thin-Film Transistors

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Solution processing and low-temperature annealing (T < 300°C) of the precursor compounds promise low-cost manufacturing for future applications of flexible oxide electronics. However, thermal budget reduction comes at the expense of increased charge trapping residuals in the dielectric layers, which result in hysteretic switching of transistors. This work reports on a novel bilayer dielectric scheme combining aluminum oxide (AlO_x) as a positive charge trapping insulator and yttrium aluminum oxide ($YAlO_x$) as a negative charge trapping dielectric to obtain hysteresis free switching in the solution-processed metal-oxide thin-film transistors. Devices were processed at a thermal budget of 250°C, without an encapsulation layer. The presence of H^+ and OH^- in the AlO_x were found responsible for the hysteresis in the switching, which was suppressed successfully with the thickness optimization of the $YAlO_x$ in the dielectric stack. Fabricated devices yield ON/OFF ratios of 10^6, sub-pA level gate leakage currents, a subthreshold swing of 150 mV/decade, and field-effect mobility of 1.5 cm^2/V-sec.

Keywords: solution processing, metal oxides, dielectrics, low temperature curing, charge trapping, thin-film transistor (TFT)

INTRODUCTION

The driving element of flexible electronics is the thin-film transistor (TFT), finding applications in flat panel displays (Barquinha et al., 2012), digital and analog circuitries (Petti et al., 2016), and sensors (Smith et al., 2014; Knobelspies et al., 2018). Metal-oxide semiconductors are implemented in the mainstream TFTs for today's display industry, thanks to their intrinsically high motilities (μ~ 50–100 cm^2/V-sec) (Paterson and Anthopoulos, 2018). The sputtering method, commonly employed for depositing metal-oxide semiconductors, offers excellent uniformity over large areas necessary/required for displays. Encapsulated metal-oxide TFTs have several years of lifetime stability, solving the issue of the formerly dominant technology with a-Si-based TFTs (Fortunato et al., 2012). Thanks to the wide band-gap (E_G > 3 eV) of the semiconductor, ultralow leakage current in the off operation (I leakage < pA) is obtained from oxide based TFTs.

In the rising era of flexible electronics and optoelectronics, solution-processing methods are investigated as low-cost alternatives to vacuum-based processing (Kim et al., 2014). The ease of manufacturing and availability of inexpensive precursors make solution processing attractive for

researchers. The conventional synthesis route of the materials from precursor solutions to dense metal oxide networks requires thermal treatment at high temperatures (T > 400°C) (Lee et al., 2018). Alternative methods, such as light-assisted annealing (Kim et al., 2012; Bolat et al., 2019; Gilshtein et al., 2020; Mancinelli et al., 2020), microwave annealing (Hwang et al., 2011; Cheong et al., 2015) and solution-combustion synthesis (Kim et al., 2011; Liu et al., 2017) enable lower process temperatures compatible with flexible substrates.

Because of the low-temperature processing, residuals of the forming precursors and solvents can remain in the solution-processed layers (Wang et al., 2018). These residuals can create intrinsic defects in the layers, resulting in unexpected charge trapping/migration under a field effect (Jin et al., 2016). This property, if happens in the dielectric layer, results in hysteretic switching behavior of the TFTs. Depending on the behavior of the defects (or residuals) clockwise (Bolat et al., 2019) or counterclockwise hysteresis (Bolat et al., 2020) can be observed in the transfer characteristics of the device. Counterclockwise hysteresis was reported with various dielectrics cured at low temperatures (T < 300°C) such as AlO_x (Liang et al., 2020a), GdO_x (Zhou et al., 2020), and ZrO_x (Kim et al., 2020). This behavior was usually complemented with unprecedentedly high mobility values compared to vacuum-based counterparts, which were reflected as mA range ON currents in the transistors (Daunis et al., 2018). There have been several hypotheses to explain the underlying mechanism for the high mobility in these devices, such as electron donation from dielectric to channel layer during the device operation (Zeumault and Subramanian, 2016), and or electron migration from the dielectric towards the gate contact (Daunis et al., 2018), gate capacitance dependent mobility behavior (Lee et al., 2014), together with the underestimated dielectric constant in the studies due to the use of a high frequency (>kHz) capacitance value to extract the mobility from static transfer characteristic measurements. Such behavior was closely related to the presence of the water within the dielectric (Daunis et al., 2018). In addition to the electron migration hypothesis, Liang et al. (Liang et al., 2020b) underlined another phenomenon existing in solution-processed AlO_x dielectrics. It was observed that at the quasi-static frequencies, in addition to the readily existing high electric double-layer (EDL) capacitance, a bias dependent capacitance was present due to faradaic charge transfer at the interfaces of the dielectric with semiconductor and metal layers, which increased the gate capacitance by almost two orders of magnitude (the so-called pseudo capacitance effect). This effect was held responsible for the increased ON current in the transistors. Consequently, the mobility values of TFT devices had to be revised and were significantly lower than those estimated without considering the pseudo capacitance effect.

Hysteresis-free electrical switching is desired for stable operation of the TFTs in their implementation for flat panel displays and digital circuits (Fortunato et al., 2012; Wager, 2020). One way of minimizing the hysteresis of the bottom gated TFTs in the transfer characteristics is to increase the post-deposition annealing temperature of the solution-processed dielectrics, contradicting the needs of flexible electronics processing or by encapsulation of the fabricated devices (Wang et al., 2018). We explore an alternative approach to engineering the dielectric stack using various insulators, with counterbalancing charge-trapping properties, when combined in a TFT offering minimal hysteresis. This approach is advantageous over the former methods, as it does not hinder the properties of the layers processed after the dielectrics. Also, it diminishes the need for the via hole opening of the source-drain contacts, which is required after the encapsulation layer deposition. The flexible TFTs with DUV annealed $YAlO_x$ dielectrics (Bolat et al., 2019) included positive shifts in the V_T due to positive gate bias stress, which is a sign of negative charge trapping within the dielectric. In contrast, the devices with DUV annealed AlO_x dielectrics (Bolat et al., 2020) (Mancinelli et al., 2020) had counter clockwise hysteresis in their transfer characteristics as a sign of positive charge trapping in the dielectric layer. In this study tuning the sign and magnitude of the hysteresis in the transfer characteristics of the TFTs is implemented by stacking solution-processed AlO_x and $YAlO_x$ layers cured with deep ultraviolet assisted annealing at 250°C as the insulators of the devices. Thicknesses of the layers and their respective position in the devices were optimized to achieve a hysteresis-free operation. Detailed electrical and chemical analyses were performed to shed light on the origin of the charge trapping mechanism.

RESULTS AND DISCUSSION

Initial experiments were conducted with devices having only one type of dielectric, i.e., AlO_x or $YAlO_x$. Two layers of dielectrics were inkjet printed to ensure pinhole-free deposition (resultant thickness ~50 nm). Cross-sectional schematics of the TFTs are shown in **Figures 1A,B**. Full-sweep transfer characteristics of the TFTs are shown in **Figures 1C,D**. Transfer characteristics of the devices with various W/L ratios (W/L = 2–20) are shown in **Figures 1E,F**. A microscope image from the top of a fabricated TFT is given in **Figure 1G**. Device parameters extracted from transfer characteristics are given in **Table 1**.

The devices with AlO_x dielectrics have four orders of magnitude higher ON current than their $YAlO_x$ employing counterparts. This behavior can be related to the electrolyte behavior of the solution-processed AlO_x dielectrics. $YAlO_x$ dielectrics have been reported to have minimal to almost no dispersion in their capacitance values at the 0.1 Hz- 1 MHz frequency range (Gillan et al., 2021). The permittivity of $YAlO_x$ was extracted as 9.1 in our previous study (Bolat et al., 2019). The permittivity of the printed and low-T (250°C) cured AlO_x can be as high as 40 at the quasi-static frequency levels. Still, this would yield only one order of magnitude difference in the ON current by itself. In addition to the electric double-layer capacitance, faradaic charge exchanges at the quasi-static frequency levels (Liang et al., 2020b), reflects as several orders of magnitude increase in the capacitance of the MOS capacitor. This can explain the difference in the ON current of the devices observed here, as well.

The TFTs with AlO_x dielectrics suffer from counterclockwise hysteresis (positive charge trapping) in their turn-off transients

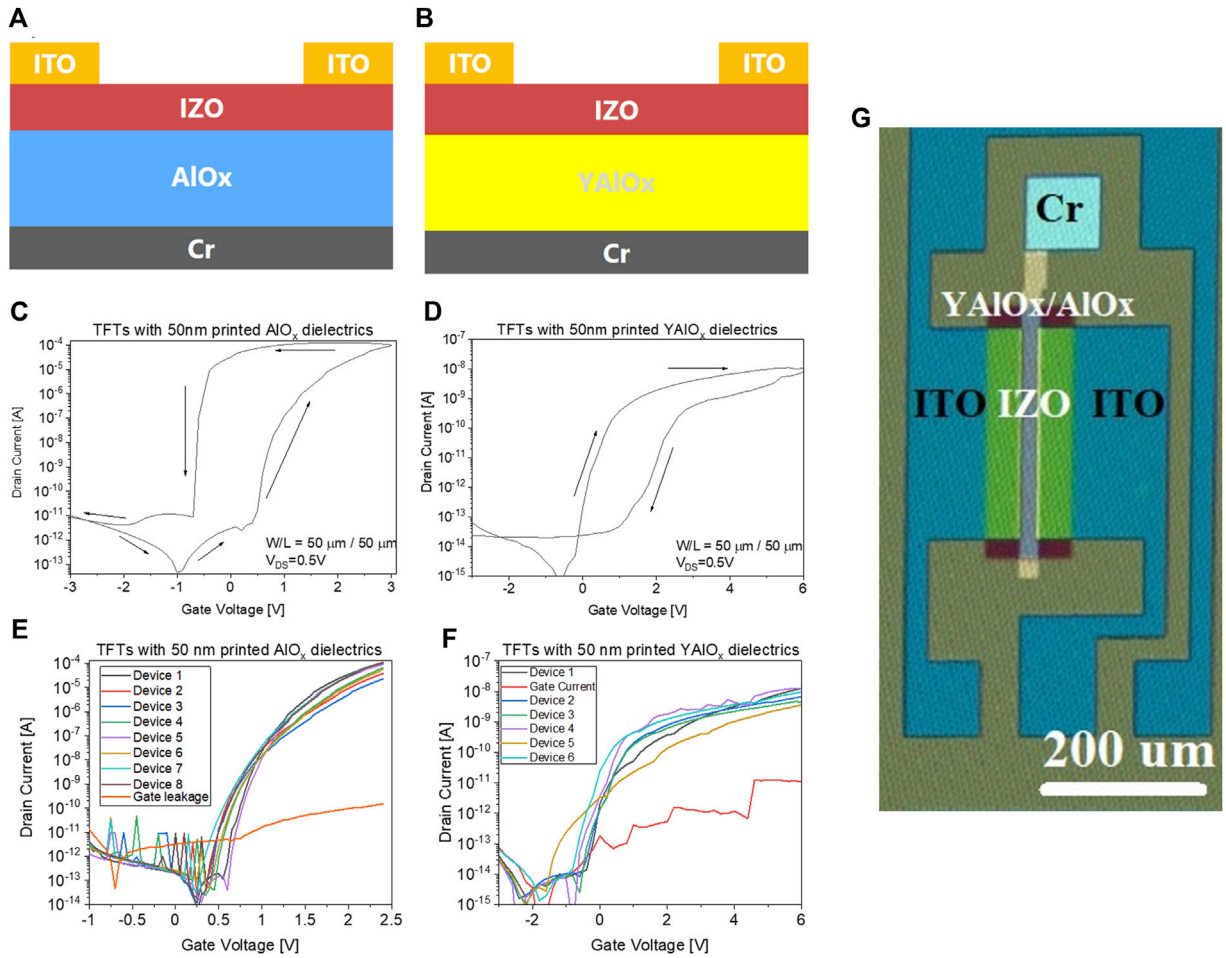

FIGURE 1 | (A) Schematic of the TFTs with AlO_x only dielectrics. **(B)** Schematic of the TFTs with $YAlO_x$ only dielectrics. **(C,D)** Full sweep of the gate bias in the transfer characteristics resulting in the opposite direction of hysteresis. **(E,F)** Transfer characteristics of several TFTs **(G)** Optical microscope image of a fabricated TFT.

TABLE 1 | Device parameters of the TFTs with a single type of dielectric layers.

Extracted parameter	TFTs with AlO_x dielectrics	TFTs with $YAlO_x$ dielectrics
ON current (A)	10^{-4}	10^{-8}
ON/OFF ratio	10^{8}	10^{5}
Subthreshold swing (mV/decade)	80	200
ON voltage (V)	0.45 ± 0.15	−0.6 ± 0.2
Threshold voltage (V)	1.6	0.35
Gate leakage current at the threshold voltage (A)	10^{-10}	10^{-13}

(**Figure 1C**). The full sweep of the transfer characteristics of the $YAlO_x$ employing devices instead reveals clockwise hysteresis (**Figure 1D**). Clockwise hysteresis results from negative charge trapping within the dielectric and/or in the dielectric semiconductor interface (Cross and De Souza, 2006). The trapped negative charges screen the effect of the gate bias, and the accumulated channel region depletes at higher voltages than expected during the turn-off transient. A conclusion on these results is that, on the one hand, the gate stacks employing printed AlO_x or $YAlO_x$ are not suitable by themselves for hysteresis-free switching applications. Observation of the opposite direction of hysteresis (countersign charge trapping), on the other hand, ignites the idea of implementing a bilayer scheme, which can minimize the hysteretic behavior in the switching after the thicknesses are optimized. To prove the hypothesis, TFTs with bilayer $AlO_x/YAlO_x$ dielectric stack were manufactured *via* spin coating of the metal-oxide layers and following the fabrication as mentioned in the experimental section for device manufacturing.

TABLE 2 | Thicknesses of the $AlO_x/YAlO_x$ bilayer dielectrics.

$AlO_x/YAlO_x$	Thickness (nm)	n
4 layers/0 layer	28.8	1.564
3 layers/1 layer	29.2	1.595
2 layers/2 layers	29.9	1.606
1 layer/3 layers	30.0	1.602
0 layer/4 layers	30.8	1.604

The total thickness of the dielectric layer stack was reduced to ~30 nm to provide better gate control and reduce the operating voltage of the devices. Ellipsometry measurements were performed to determine the thickness of the layers. **Table 2** shows the extracted refractive index from the dielectric stacks along with the measured thickness. A Cauchy model was used for fitting the data.

The thicknesses of the layers are in the ~30 ∓ 1 nm range, with the refractive index increasing in line with the amount of $YAlO_x$ in the stack. Y_2O_3 has a higher refractive index than Al_2O_3, which supports the observed behavior.

Dielectric stacks with the configurations shown in **Table 2** are later implemented in bottom gated TFTs. As the TFTs with AlO_x only case and initial experiments with bilayer scheme yielded higher ON currents with AlO_x in contact with the channel layer (**Figure 1A**; **Supplementary Figure S1**), the AlO_x layer was used as the uppermost layer in contact with the semiconducting IZO channel in these experiments, too. Electrical characterizations were performed on the TFTs to investigate the hysteretic behavior. Transfer characteristics of the devices are shown in **Figure 2**. For an easy understanding, the samples were given the names according to the number of $YAlO_x$ layers inside, i.e., 0 layer $YAlO_x$, 1 layer $YAlO_x$, 2 layers $YAlO_x$, and 3 layers $YAlO_x$.

Obtained characteristics reveal that the counterclockwise hysteresis is present for the 0 layers $YAlO_x$ and 1-layer $YAlO_x$ dielectrics cases. Devices with 2 layers of $YAlO_x$ dielectrics show minimal hysteresis, whereas the 3 layers $YAlO_x$ employing devices have clockwise hysteresis in their transfer characteristics. From these results, one can conclude that by alternating the layer thicknesses in the insulator stack, it is possible to obtain hysteresis-free switching in the bottom gated solution-processed oxide TFTs, even without an encapsulation layer. **Table 3** shows the device parameters extracted from the transfer characteristics.

C-V characteristics were obtained from MOS capacitors with 100 μm × 100 μm areas at various frequencies to understand the device operation better. **Figure 2A** shows the frequency dispersion of the dielectric constant for the bilayer dielectrics. **Figure 2B** shows the measurement results at 10 Hz, the lowest measurement frequency, which is later, used to minimize the overestimation in the extracted mobility of the devices.

Electrolyte behavior supported by the low-frequency dispersion of capacitance is diminished with the insertion of 2 layers (~15 nm $YAlO_x$) dielectric into the insulator stack.

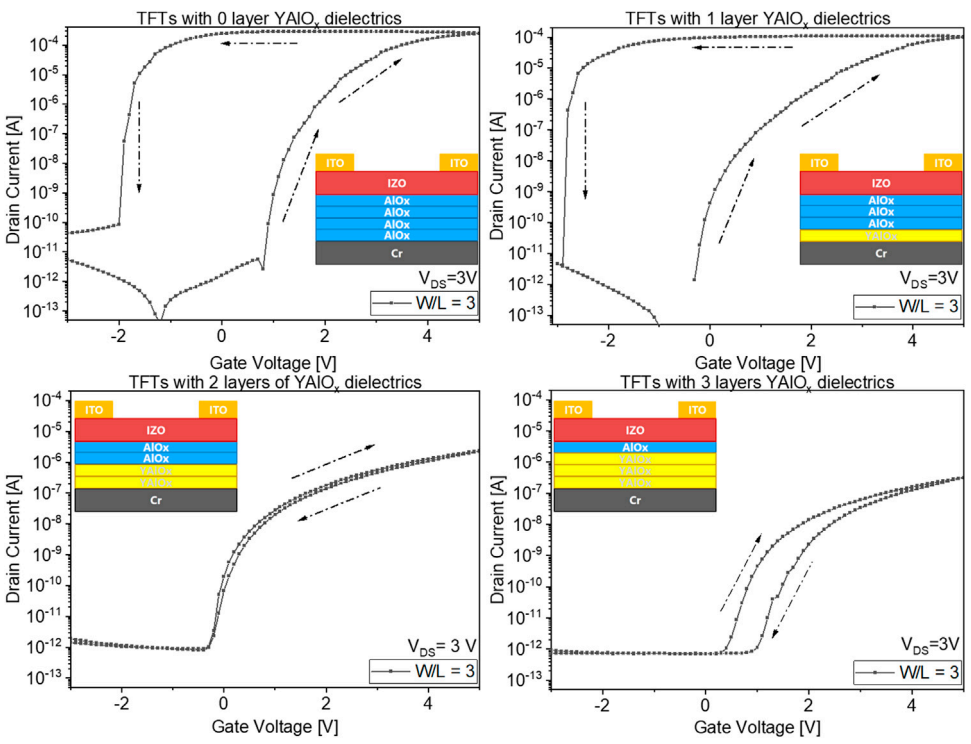

FIGURE 2 | Transfer characteristics of the TFTs with bilayer $AlO_x/YAlO_x$ dielectrics of alternating layer configurations.

TABLE 3 | Device parameters of the TFTs with bilayer dielectric layers.

Extracted parameter	0 layer $YAlO_x$	1 layer $YAlO_x$	2 layers $YAlO_x$	3 layers $YAlO_x$
ON current (A)	3×10^{-4}	2×10^{-4}	3×10^{-6}	5×10^{-7}
ON/OFF ratio	10^8	10^8	10^6	10^5
Subthreshold swing (mV/decade)	80	100	150	300
ON voltage (V)	0.45 V	−0.6	−0.15	0.20
Threshold voltage (V)	1.6 V	1 V	1.2 V	1.8 V
Gate leakage current at threshold voltage (A)	10^{-10}	10^{-11}	$<10^{-12}$	$<10^{-12}$

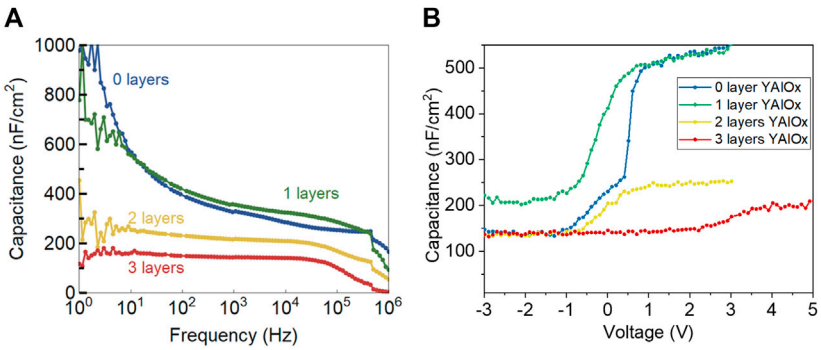

FIGURE 3 | (A) Frequency dispersion of the areal capacitance in the bilayer $AlO_x/YAlO_x$ dielectrics measured at 3 V. **(B)** C-V characteristics of the MOS capacitors with bilayer $AlO_x/YAlO_x$ dielectrics and IZO channel layer.

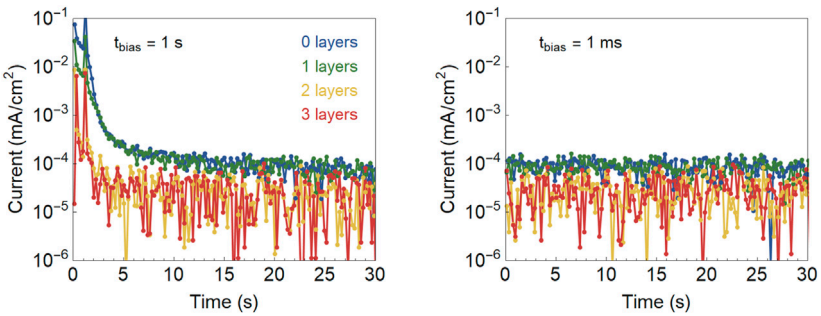

FIGURE 4 | Transient current measurements from MOS capacitors with alternating bilayer dielectric thicknesses.

Transient current analyses were performed on the MOS capacitors to estimate a time-dependent behavior for the effective charge trapping in the structures. Pulses of 3 V were applied to the gate for two different periods, while the semiconductor contact was kept at ground level. Finally, the resulting transient current was measured at a gate bias of −3 V. **Figure 3** shows the obtained results.

Since long filling times (~seconds range) are required to observe transients, the measured signals can be assigned to ionic rather than electronic defects, since electronic defects should already be visible at a filling time of 1 ms, but not ionic defects. (Futscher et al., 2020). Residuals in the AlO_x dielectrics, such as H^+ and OH^- ions, were reported partly responsible for the enhanced quasi-static frequency polarization in the dielectric (Daunis et al., 2018; Bolat et al., 2020; Liang et al., 2020b). Secondary ion mass spectroscopy (SIMS) measurements were performed on the bilayer dielectrics spin-coated on Si wafers to investigate the hypothesis in detail. OH^- and H^+ and C signals were measured across the dielectric stack, and the results are demonstrated in **Figure 4**.

H^+ signal level is higher in the 4 layers AlO_x and 1 layer $YAlO_x$ samples compared to the samples with thicker $YAlO_x$ layers. C signal is at the detection noise level in all the layers. A closer look at the H^+ and OH^- signals from the layers is provided in **Figure 5**.

H^+ and OH^- signals have significantly higher levels for the AlO_x and 1 layer $YAlO_x$ samples, supporting the positive charge trapping in the dielectric due to ion movement and charge

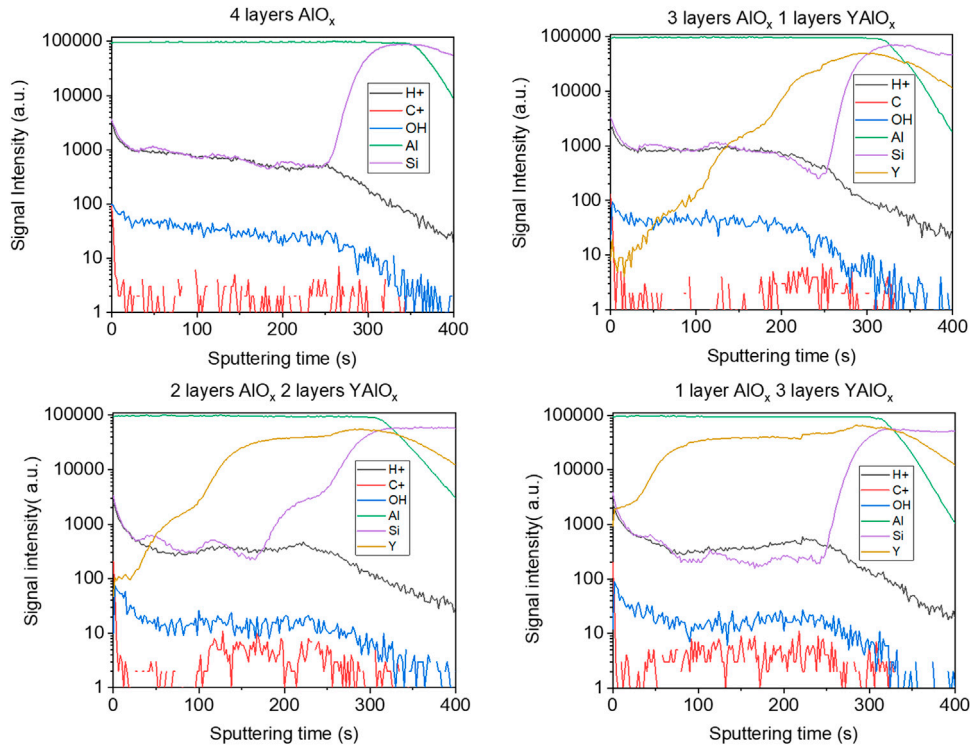

FIGURE 5 | SIMS profile shows residuals' behaviors (H^+, OH^-, and C) across the $AlO_x/YAlO_x$ layer stacks.

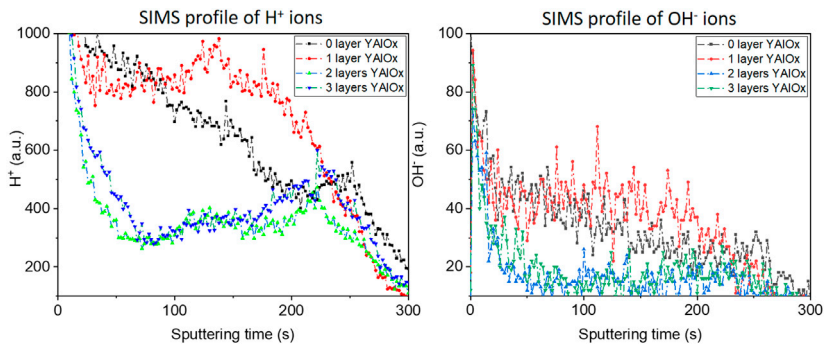

FIGURE 6 | Comparison of SIMS profiles of H^+ and OH^- through the depth of the bilayer dielectrics.

exchange in the vicinity of the gate-dielectric interface. The H^+ and OH^- signal suppresses at the onset of $YAlO_x$ layer in the samples with thicker $YAlO_x$ layers (blue and green curves), which can explain the decrease of the dielectric constant at the low-frequency regime. As the OH^- and H^+ ion movement towards the bottom of the dielectric is blocked, the ionic charge movement and charge exchange between gate and dielectric diminishes, which suppresses the electric double-layer capacitance.

For an ease of understanding, we explain the charge trapping, ion migration and suppression of such migration mechanism in the bilayer dielectrics as follows:

Under the field effect of the gate bias, the water molecules in the AlO_x dielectric dissociate into H+ and OH- ions. H+ and OH- ions move towards the semiconductor and gate contacts, respectively. This results in the electric double layer formation at the interfaces as also reported in previous works (Yuan et al., 2010; Daunis et al., 2018; Liang et al., 2020b). Existence of the H+ ions at the oxide semiconductor interface further enhances the field effect by orders of magnitude due to the faradaic charge exchange between the adsorbed H+ ions and semiconductor, resulting in the pseudocapacitance. This process can be considered as protonation of the semiconductor dielectric interface and was

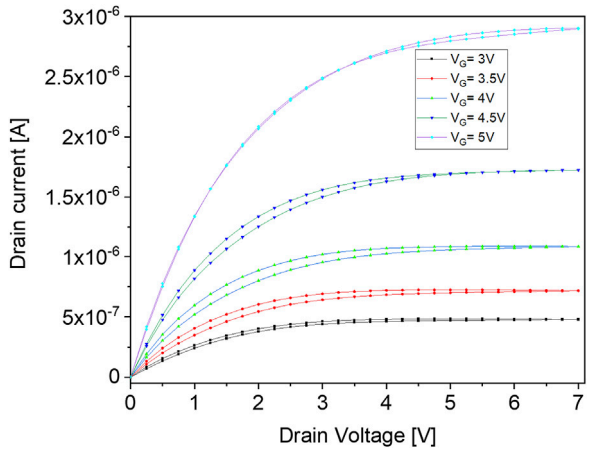

FIGURE 7 | Output characteristics of the TFTs with 2 layers $YAlO_x$ dielectrics.

also reported by Yuan et al. for a H_2O doped electrolyte ZnO interface (Yuan et al., 2010). Since the dehydrogenation requires a large energy, channel stays ON until a large negative bias is applied from the gate contact (**Figure 6**). For the devices with $YAlO_x$ dielectrics, the ion movement blocking takes effect for the scenarios where the $YAlO_x$ thickness is more than 10 nm. For the single layer case (1 layer $YAlO_x$), the H+ and OH- ions are not suppressed and can reach until the gate, as confirmed by SIMS measurements (**Figure 5**). For the bilayer dielectric containing stacks with $YAlO_x$ thickness >10 nm, use of AlO_x at the insulator semiconductor interface results in a higher ON current than the devices where $YAlO_x$ is placed in contact with the semiconducting channel layer, despite using identical thicknesses for each material. This can be seen in **Supplementary Figure S1** and be related to the hydrogen rich nature of the AlO_x resulting in the electron donation to the channel, as reported by Daunis et al. and also by Zermault and Subramanian. (Zeumault and Subramanian, 2016; Daunis et al., 2018).

Devices with two layers $YAlO_x$ dielectrics were characterized electrically to obtain their output characteristics since the minimal hysteresis was obtained for this dielectric configuration. Results are shown in **Figure 7**. μ_{FE} is extracted from the output characteristics at a drain voltage of 3 V in the saturation region using **Eq. 1** as ~1.5 cm^2/V.sec.

$$\mu_{FE} = \frac{2L}{WC_{Ox}}\left(\frac{d\sqrt[2]{I_{DS}}}{dV_{GS}}\right)^2 \quad (1)$$

It is important to consider that the mobility is not affected only by the dielectric itself, the low temperature processing also results in high amount of hydroxides in the semiconducting layers, thereby reducing the mobility of the devices. Daunis et al. also reported reduction of the extracted mobility with the insertion of ion blocking dielectric layer into the gate stack, where they observed a reduction from 117 cm^2/V.sec to 4.6 cm^2/V.sec after the suppression of the hysteretic behavior (Daunis et al., 2018).

CONCLUSION

Solution processing promises low-cost manufacturing of oxide electronics on flexible substrates. This requires temperature reduction of the post deposition annealing of the as-deposited precursors, which results in anomalous charge trapping in the dielectric layers. In this work, the effects of implementing two counterbalancing charge-trapping dielectrics ($YAlO_x$ and AlO_x) in low-temperature cured solution-processed TFTs were investigated. Increasing the thickness of the negative charge trapping $YAlO_x$ in the bilayer dielectric stack was observed to diminish the EDL capacitance thought to be originated from H^+ and OH^- ion migration in the AlO_x dielectrics. Detailed SIMS analysis revealed the significant decrease of the H^+ and OH^- ions in the $YAlO_x$ dielectrics, supporting the hypothesis. A stack of 15 nm $YAlO_x$ 15 nm AlO_x offered hysteresis-free transistor switching, providing an alternative methodology to obtain stable operation. This methodology can be extended to various insulators with counterbalancing charge trapping and provide a general manufacturing route for high-performance, stable switching low-temperature solution-processed oxide transistors.

EXPERIMENTAL

Ink preparation: $YAlO_x$ (Y: Al, 2:8) and AlOx inks were prepared by dissolving $Al(NO_3)_3 \times 9H_2O$ and $Y(NO_3)_3 \times 6H_2O$ salts in 50%/50% volume 2-Methoxyethanol/Ethylene glycol. Nominal metal ion concentration was adjusted as 0.4 M for printed dielectrics and 0.1 M for spin-coated layers. Solutions were stirred at 70°C for 12 h and filtered with a 0.2 µm PFTE filter. The viscosity of the printing ink was measured at 25°C by a strain-controlled rheometer (Anton-Paar MCR 301) with plate/plate geometry (25 mm diameter, 0.1 mm gap). It was obtained as 12 cP falling in a suitable range for inkjet printing.

IZO ink was prepared by dissolving $In(NO_3)_3$. xH_2O and $Zn(NO_3)_2 \times 6H_2O$ with a total metal ion concentration of 0.2 M (In: Zn, 7:3) in 2-Methoxyethanol. The nominal metal ratio was chosen according to the reported literature (Mancinelli et al., 2020). The solution was stirred at 60°C for 12 h and filtered with a 0.2 µm PFTE filter before deposition.

TFT fabrication: A test-grade silicon wafer serving as the substrate was sonicated in acetone (5 min), isopropanol (5 min), and DI water (5 min). Cleaned substrates underwent a buffered oxide etchant exposure to remove the native oxide from the wafers. 100 nm thick SiN_x was deposited via plasma-enhanced chemical vapor deposition at 150°C to isolate the devices from the substrate. E-beam evaporated Cr (35 nm) was used as gate contact and patterned via photolithography. Dielectric layers were deposited as follows:

Printed AlOx and YAlOx dielectrics: AlOx and YAlOx were inkjet printed with a resolution of 400 drops-per-inch via LP50 inkjet printer with Dimatix cartridges of 10 pL nozzle volume. Two layers of dielectric ink were printed to avoid pinholes in the insulator.

Printed layers were dried at 250°C, and were exposed to DUV with N_2 flow (6 L/min) for 30 min. DUV annealing is performed with a low-pressure mercury lamp (Filgen Inc. UV253H) with two emission peaks at 184 and 253 nm and output power density of 25–28 mW/cm^2. Final annealing at 250°C (60 min) in air ambient was applied to densify the cured layers further.

Spin-coated AlOx and YAlOx dielectrics: 4 layers of dielectrics layers were created by spin-coating at a speed of 4,000 rpm and subsequent drying at 150°C for 5 min. Before every spin-coating, the substrates were exposed to 1 min of oxygen plasma to enhance the wetting of the subsequent layers. Dried layers were exposed to DUV with N2 flow (6 L/min) for 30 min and later annealed in air at 250°C for 30 min.

Spin-coated IZO channel layer: Two consecutive layers of IZO ink were spin-coated with a speed of 2000 rpm for 30 s and dried at 150°C. The dried semiconductor layer underwent the DUV exposure in the air for 30 min and the last annealing step at 250°C for 60 min 30 nm thick semiconductor channel was photolithographically patterned and etched with a 1:121 diluted hydrochloric acid solution.

Sputtered ITO contacts: Source and drain contacts were realized via sputtering and lift-off of ITO layers with the following parameters: Sputtering pressure: 0.4 Pa, O_2 Flow:0 sccm, Ar Flow: 60 sccm, RF sputtering power: 180 W, deposition temperature: room temperature, the thickness of the layer ~100 nm. The sheet resistance of the layer was ~25 ohms/square.

Electrical characterizations: DC characteristics of the TFTs were acquired in the dark with a Keithley 4,200 Semiconductor parameter analyzer. C-V, C-f, and transient measurements on MOS capacitors were performed by using Paios from Fluxim AG. C-V and C-f measurements were performed using an AC voltage of 50 mV.

SIMS measurements: The primary beam was 25 keV Bi+ ions with a total current of 1.1 pA and a raster size of 50 × 50 μm^2. For detection of negative ions, Cs^+ ions were used with 500 eV ion energy, 30 nA pulse current on a 300 × 300 μm^2 raster size to bombard and etch the film.

Optical characterizations: Optical characterization and thickness measurement of the AlO_x/$YAlO_x$ bilayer dielectrics deposited on Si(<100>) was acquired by ellipsometry (J.A. Woollam M-2000V). The bilayer was modelled as a Bruggeman effective medium approximation (EMA) layer. The fitting was performed using the CompleteEASE software by J.A. Woollam Co.

DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/**Supplementary Material**, further inquiries can be directed to the corresponding authors.

AUTHOR CONTRIBUTIONS

SB and YR conceptualized the idea. SB fabricated the devices. EA performed the electrical characterizations on the TFTs with bilayer AlO_x/$YAlO_x$ dielectrics, critically analyzed the obtained results, and discussed them with SB, YR, EA, SB, and MF performed the C-f, C-V, and transient current measurements on the MOS capacitors. IS supervised the electrical characterizations. S-CY optimized the sputtering recipe for the ITO contacts and performed the SIMS characterization and analysis on the bilayer dielectrics. AA performed ellipsometry measurements and fitted the obtained results for thickness and optical constant extractions of the layers. YR supervised the study. SB and YR wrote the manuscript with the inputs from all the coauthors. SB and EA contributed equally to this work.

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SUPPLEMENTARY MATERIAL

The Supplementary Material for this article can be found online at: https://www.frontiersin.org/articles/10.3389/felec.2021.804474/full#supplementary-material

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