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RECEIVED 28 August 2024

ACCEPTED 15 October 2024

PUBLISHED 13 November 2024

CITATION

Cruz C and De Vicente J (2024) Charge-coupled device readout by digital-correlated double sampling.

Front. Detect. Sci. Technol. 2:1487623.
doi: 10.3389/fdest.2024.1487623

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Charge-coupled device readout by digital-correlated double sampling

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Charge-coupled devices (CCDs) play crucial roles in astronomy owing to their widespread use in the optical band, offering high sensibility, low noise, high dynamic range, and high spatial resolution. Recent advancements in CCDs have focused on improving the sub-electron noise levels for particle detection and enhancing readout speeds through simulation studies. The main objective of this study is to replace the analog processing of CCD signals using the digital-correlated double sampling (DCDS) technique. DCDS allows post-acquisition noise correction through intermittent sampling of an internal reference voltage to provide compact and flexible performance. In this study, DCDS was evaluated using two digital processing systems, namely, a 2.5 mega-samples per second (MSPS) 24-bit analog-to-digital converter (ADC) board and a 250 MSPS 16-bit ADC field-programmable-gate-array (FPGA)-based buffer memory board. The readout noise value at 74 kpix/s (7.1 e) was a significant improvement over that obtained with analog processing (9.7 e). The DCDS implementation demonstrates optimal signal-to-noise ratio for a wide range of readout speeds. Parameters such as the sample positions per pixel, number of samples, and number of pixels were identified to be essential in achieving an accurate gain value. Finally, hardware implementation of the DCDS IP core algorithm on a Xilinx Zynq-7000 AP system-on-a-chip (SoC) showed a significant improvement in power dissipation (7.1 W) compared to the analog Monsoon correlated double sample (CDS) circuit (13.6 W). The DCDS IP core implementation also showed a background noise reduction of up to 34% compared to DCDS offline readout processing using a Python algorithm.

KEYWORDS

charge-coupled device, image sensor, dynamic range, digital-correlated double sampling, readout noise, gain, photon transfer function, field-programmable gate array

Abbreviations: ASIC, application-specific integrated circuit; CCD, charge-coupled device; SNR, signal-to-noise ratio; DCDS, digital-correlated double sampling; FFT, fast Fourier transform; PT, photon transfer; RMS, root mean square; PTC, photon transfer curve; FWC, full-well capacity; RON, readout noise; FPN, fixed-pattern noise; DR, dynamic range; MSPS, mega-samples per second; FPGA, field-programmable gate array; CDS, correlated double sampling.

1 Introduction

Scientific charge-coupled devices (CCDs) are currently used in various applications that require very low noise performances. CCD readouts are often implemented via correlated double sampling (CDS) using switched-capacitor circuits or digital signal processing algorithms after analog-to-digital conversion. By adjusting the interval between the clamping and sample-and-hold stages, the CDS approach can flexibly filter low-frequency noise to enhance the signal-to-noise ratio (SNR) and reduce the noisy electrons. Although CDS cancels offset and flicker noise (a type of electronic noise with a frequency spectrum that follows the $1/f$ law with increasing frequency in sensor signal conditioning), it requires substantial circuitry for the conversion of the received photons to digital data (Dobrev and Neycheva, 2020). CDS integration with low-noise amplifiers and analog signal processing blocks in application-specific integrated circuits (ASICs) can also contribute to noise suppression. Different approaches have been developed to optimize CCD readouts, such as specialized ASICs for CCD controllers (Juramy et al., 2014; Bessia et al., 2023) and novel analysis methods to reduce the pixel readout times (Gach et al., 2003; Moroni et al., 2020). Additionally, the use of CCDs in scientific instrumentation like telescopes underscores the importance of selecting a detector with a low readout noise (RON) and designing efficient controllers for driving the CCDs (Howell, 2000). Advancements in gamma-ray astronomy have highlighted the significance of readout electronics design, especially for detectors like photomultiplier tubes and silicon photomultipliers, emphasizing the need for integrated microelectronic implementations and different signal readout strategies (Carminati and Fiorini, 2024).

In this context, digital-correlated double sampling (DCDS) is an innovative sensor readout approach that allows low-frequency noise and offers post-acquisition noise correction through intermittent sampling of an internal reference voltage. This feature allows real-time acquisition using digital techniques for high bandwidth (Paul et al., 2022; Bourgeois et al., 2017). The present study entails a DCDS implementation system that offers a cost-effective, low-power, and digital compact solution for CCD readout, which makes it a promising technique in astronomical observations and imaging systems.

1.1 Related works

DCDS technology has been applied in astronomical cameras with mathematical models to aid with noise suppression. Several DCDS methods have been developed theoretically, whose performances have to be compared, as emphasized by Clapp (2012). Numerical simulations demonstrate the possibility of predicting the point with the lowest RON for a DCDS model, enhancing the selection of optimal parameters for noise reduction (Duan et al., 2021). For instance, Yao et al. (2023) demonstrated through simulations that noise reduction could be achieved with more sample processing. The RON in CCDs can be significantly reduced (i.e., by 4 e, requiring up to 300 sampling points at 83.3 kHz operating frequency), as highlighted by Liu et al. (2015). DCDS not only minimizes the reset noise in detectors but

also provides low RON to balance the digital sampling rate against the pixel rate (Clapp et al., 2016). In this context, Clapp et al. (2017) proposed an experimental weighting method for comparisons against theoretical predictions, where the integration of transition samples does not significantly affect the gain value. DCDS has also been applied to complementary metal-oxide semiconductor (CMOS) detectors, as presented by Zou et al. (2019). The responses of specific pixel circuits at low light levels with DCDS are evaluated by subtracting the reset noise from the pixel signals off-chip. Although this approach cannot remove flicker noise completely, the column noise (a type of noise arising from mismatches in the column-parallel readout circuits of image sensors) can be reduced. The selection of timing parameters has also been evaluated for noise subtraction from video signals (Weatherill et al., 2019). Given these efforts, numerical sampling optimization is a promising method to optimize the tradeoff between the linearity and SNR of the sensor readout.

Characterization of the CCD is an essential step before its use in astronomical observations. The spectral response is a vital measure for accurately capturing and interpreting astronomical data across different wavelengths. In this regard, the significance of CCD characterization was detailed by Scuderi et al. (2023), highlighting the importance of understanding the technical specifications of CCDs before deploying them as electronic readouts. Additionally, Drluca-Wagner et al. (2020) discussed the validation of skipper CCDs by showcasing their potential to achieve stable and high quantum efficiencies as well as single-electron resolutions, which in turn refer to the detector capacity to identify and precisely measure signals generated by the absorption of individual electrons. Cruz and de Vicente (2018) underscored the critical role of detector characterization for performance optimization following the CCD photon transfer curve (PTC) method (Janesick et al., 1987; Janesick, 2007). Detectors were initially calibrated in an optical testbench and then characterized under different exposure times as CCD performances are quite sensitive to the system ground. As highlighted by Casas et al. (2014), the dark current and gain conversion factor of a CCD detector were determined in electrons per analog-to-digital unit (e/ADU) using a radioactive Fe^{55} source within the cryostat placed in front of the detector; this is considered an accurate test to measure the gain conversion factor. However, the emitted X-rays can also be used for a short period owing to the decay of the isotopes (half-life of 2.74 years). Jiménez et al. (2012) developed a testbench with a flat-field monochromatic light source by integrating a sphere with the ability to select different light exposure times. A data acquisition system was used to control the video bias and clock boards, the front-end electronics provided the signal distribution, and preamplifier stages were available inside the cryovessel.

Field-programmable gate array (FPGA)-readout-based processors that provide high-speed correlations based on the fast Fourier transform (FFT) (Altaf et al., 2015) or very-large-scale integration architectures using FFT (Jridi and Alfalou, 2017) have enhanced digital processing for many applications. Furthermore, multichannel single-chip correlations for photon spectroscopy based on FPGAs allow simultaneous processing of multiple input channels with high dynamic ranges (DRs) (Jakob et al., 2007; Jiang et al., 2013). These advancements showcase the power and versatility of FPGA-based systems in digital

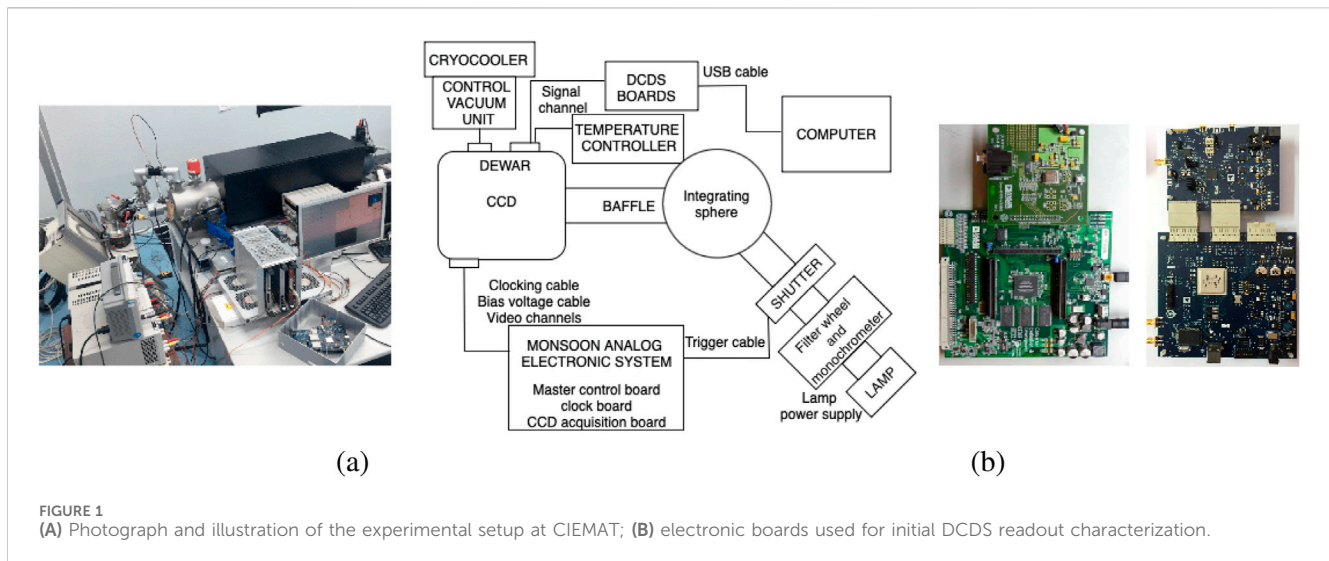


FIGURE 1
(A) Photograph and illustration of the experimental setup at CIEMAT; (B) electronic boards used for initial DCDS readout characterization.

applications that require high accuracy and flexibility. For DCDS-related advances with FPGAs, [Tulloch \(2016\)](#) suggested using a Xilinx Spartan-3E FPGA board to implement a customized DCDS method with analog-to-digital converter (ADC) frequencies of up to 25 MHz. A differential averaging scheme with over 100 samples per pedestal pixel has been used to achieve low noise (4.2 e) at a low pixel rate (67 kpix/s). [Liu et al. \(2015\)](#) considered 350 effective sampling points at an operating frequency of 83.3 kHz to obtain a RON value of 44.2 e; this implementation was validated using an Fe^{55} radioactive source without accounting for the full-well capacity (FWC) and DR of the detector.

1.2 Research gaps

Traditional analog CDS methods suffer from thermal noise or Johnson–Nyquist noise limitations such as kT/C noise as well as settling time constraints that impact the sampling frequencies in sensing systems ([Cho et al., 2023](#)). Several researchers have explored the advantages of using digital techniques for waveform processing, given only the theoretical frameworks and simulation results ([Smith and Kaye, 2013](#); [Alessandri et al., 2015](#)). Additionally, integrating DCDS circuits into large-area or mosaic cameras poses space and energy consumption constraints, making it difficult to implement traditional analog CDS circuits. DCDS experimental studies have also highlighted the linearity limitations occurring near clock and clock-edge transitions during sampling that can increase the total integrated noise.

1.3 Specific contributions

The main contribution of this study is the validation of innovative algorithms to analyze and process digital samples obtained from CCD readouts. Accordingly, two digital processing systems were tested over the complete DR of the CCD. Then, readout characterizations were performed based on the photon transfer (PT) method under vacuum and controlled temperature conditions to confirm the effectiveness of the digital processing

approaches. However, some caveats are noted with respect to sample selection to cover the FWC by assessing both the gain (K) and RON. A customized DCDS was implemented on an FPGA, and its electronic noise accuracy was compared with that of offline DCDS. This study also reports a significant improvement in power dissipation compared to those of analog circuits; the noise values achieved were similar to those for analog processing, given the technical specifications of the CCD, demonstrating the feasibility and benefits of digital processing in the CCD readout.

The remainder of this paper is structured as follows. The CCD experimental setup and readout system capabilities are described in [Section 2](#); [Section 3](#) presents the DCDS technique; the characterization procedures and their results are detailed in [Section 4](#); the DCDS implementation in IP core and its validation on an FPGA are explained in [Section 5](#); and, finally, the discussion and conclusions of this study are presented in [Sections 6, 7](#), respectively.

2 System description

The experimental setup was established in the clean room at Centro de Investigaciones Energéticas Medioambientales y Tecnológicas (CIEMAT), Madrid, Spain ([Figure 1A](#)) and is composed of a cryostat allowing a CCD readout. The detector used was a 200- μm -thick, fully depleted, back-illuminated device with an n-type silicon base provided by Hamamatsu Photonics Company. Then, a specific coating was developed that was sensitive in the range of 300–1,100 nm. The CCD was operated in the cooled state at 160 K after the experimental space was pumped to below 5×10^{-5} mbar, and these conditions were controlled using a heater. The temperature controller ensures highly stable experimental conditions and maintains the setpoint such that the fluctuations are below 1%. A minimum duration of 1 h is always required to ensure that the contaminant does not freeze onto the detector; furthermore, the experiments are commenced at least 1 h later to ensure stable operating conditions. The signals detected by the CCD were connected to a preamplifier board located inside the cryostat using a Kapton cable that was maintained at a distance of 20 cm below the CCD. This board separates the biases, clocks, and video signals, and

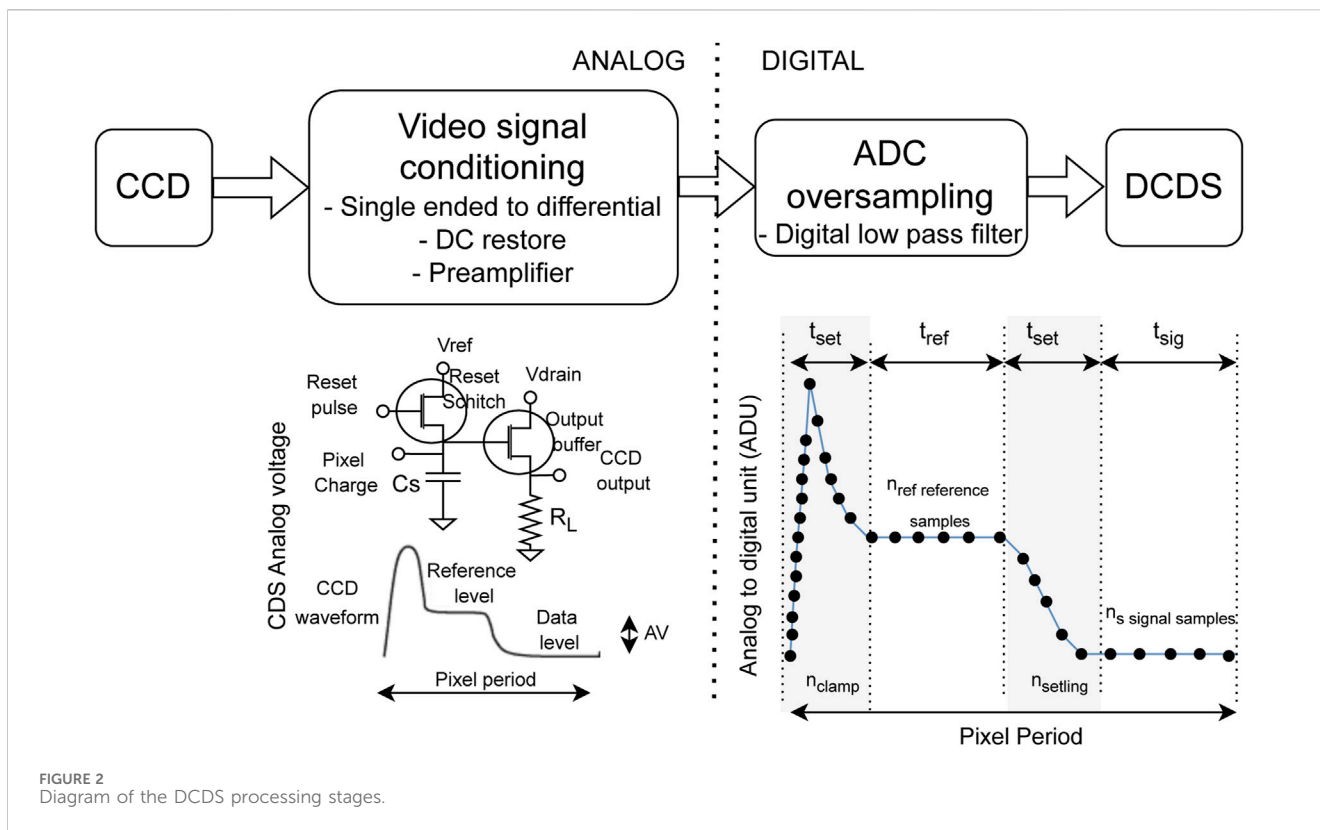


FIGURE 2
Diagram of the DCDS processing stages.

shielding layers were included to prevent electrical coupling. Finally, single-point grounding was used to minimize the noise and ground loops as well as ensure system stability, as noted by Casas et al. (2012).

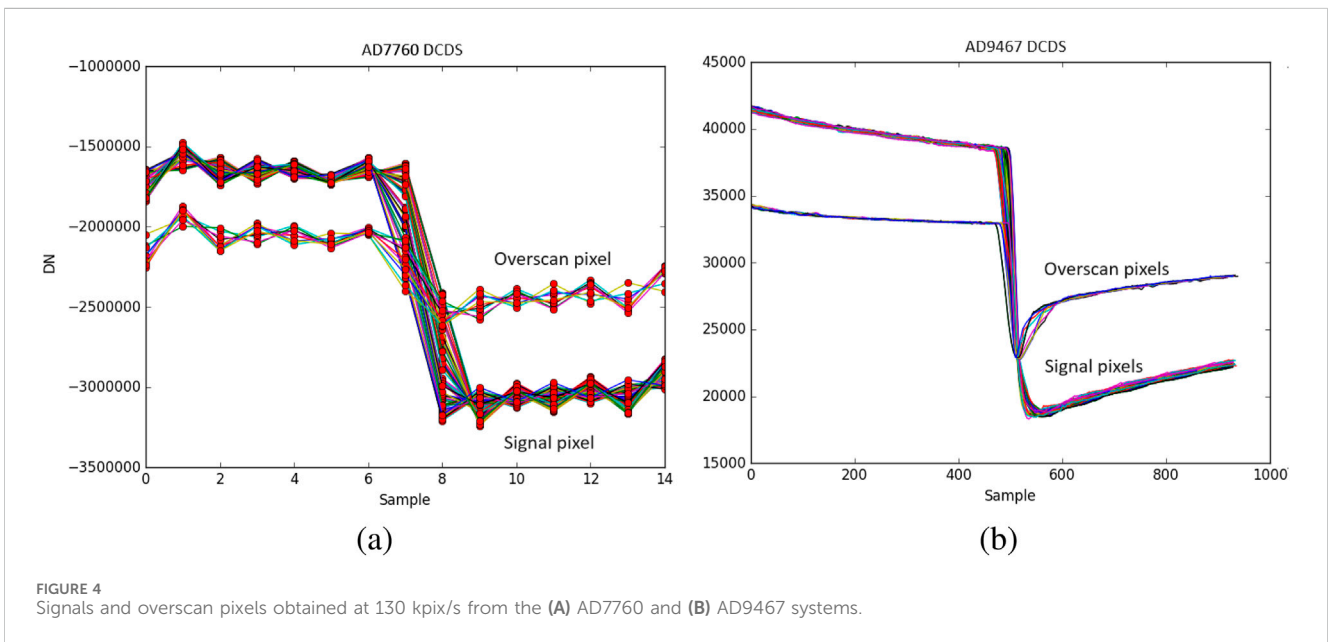
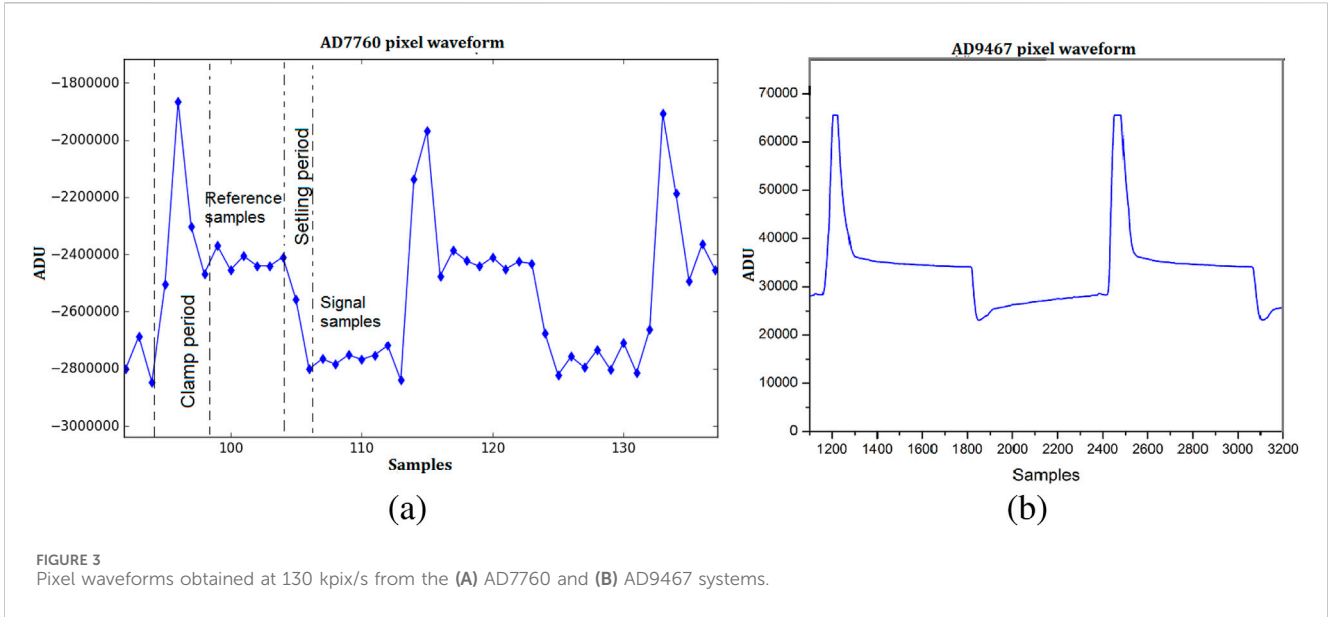
The analog readout was based on the Monsoon architecture (Jiménez et al., 2016), which comprises a master control board in charge of the pixel acquisition node, an acquisition board that provides different CCD voltages, and a clock board that generates analog clocks for sequencing and shifting the burden within the CCD. Analog CCD characterization was performed by collecting image sequences with the CCD for different exposure times up to saturation. Two digital processing systems were used for the DCDS readout (Figure 1B). We also studied the impacts of oversampling using the 2.5 mega-samples per second (MSPS), 24-bit, AD7760 sigma-delta high-performance ADC board along with an Intel Altera Cyclone FPGA. The maximum internal clock frequency used is 20 MHz, and the decimation rate can be selected from the following values: 8, 16, 32, 64, 128, and 256. The pixel signals were obtained with the HSC-ADC-EVALCZ (Analog Devices, 2024), which is a high-speed converter evaluation platform that uses an FPGA-based buffer memory board to capture blocks of digital data from the AD9467; this 16-bit monolithic ADC is perfectly suitable for DCDS owing to its high conversion rate of up to 250 MHz. The memory board was connected to a personal computer via a USB port under VisualAnalog software to quickly evaluate the ADC capabilities for DCDS readout. The analog signal conditioning circuit designed with the ultralow differential amplifier ADL5562 was modified by removing the input impedance such that the input pixel signal could be increased to the full DR of the ADC. The data

capture was synchronized to an external trigger that activated the three CCD readout systems for the same experimental conditions.

3 Oversampling method and DCDS readout

CDS reduces noise by taking two samples of the output signal, one before and one after the charge transfer, and subtracting them to cancel out the noise and offset error; it compares the reference and data levels of the CCD signals to reduce some of the noise components. The DCDS readout is usually composed of signal conditioning and oversampling processing (Figure 2). The number of ADC samples is related to the ADC frequency and system bandwidth. Furthermore, the pixels should not be sampled at the following intervals: 1) clamp period, which is the time required to restore the DC output (t is largely dependent on the system design and is commonly considered to be less than 10% of the pixel period); 2) settling period, which is the time required to stabilize the final value after a CCD charge transfer. Both these intervals are considered to be essential for ensuring accurate signal processing.

The simplest filter function is the averaging function that aims to replicate the ideal analog CDS function (Equation (1)) and requires at least two samples per pixel (i.e., reference and signal levels) to obtain the pixel value (P). The value of P is computed as the ratio of the sum of all reference samples to the total number of reference samples minus the ratio of the sum of all signal samples to the total number of signal samples; here, r_i refers to the reference samples, s_i corresponds to the signal samples, and n represents the total number of reference and signal samples. Assuming that all noise sources are white, it can be



shown that the root mean square (RMS) noise σ_p of the pixels is proportional to the RMS noise of the samples σ_{sample} , which is inversely proportional to the square root of the number of samples.

$$S(ADU) = P = \frac{1}{n_r} \sum_{i=1}^{n_r} r_i - \frac{1}{n_s} \sum_{i=1}^{n_s} s_i; \quad \sigma_p = \frac{\sigma_{sample}}{\sqrt{n}} \sqrt{2}. \quad (1)$$

DCDS characterization was conducted using the optimal number of samples per pixel. Figure 3 shows the different readout capabilities for ADC selection. AD7760 (2.5 MSPS) achieves a maximum of 20 samples per pixel at 130 kpix/s, and AD9467 (250 MSPS) provides about 1,200 samples per pixel at 130 kpix/s. As the first step, the offline algorithms for CCD readout processing were developed and tested. Each pixel was evaluated by subtracting the reference voltage from the signal

value. The absolute offset level indicates the signal measured from a region on the array where photoelectrons are not generated. For a CCD, the zero-electron level is determined by overscanning the detector's horizontal register, where the average of the overscanned pixels represents the desired ADC offset level. For instance, the overscan pixels are virtual pixels generated by the electronics when the CCD is read, and this can be configured as extra rows of pixels to provide a measure of the electronic reference level. Hence, these pixels appear as strips along one or more sides of the CCD images, and the ADC offset is calculated as the signal from the overscan pixels that is subtracted from the signal value. The pixels must also be processed to remove samples associated with the clamp period. Figure 4 shows a part of this process by including up to 100 pixels as both the signal and

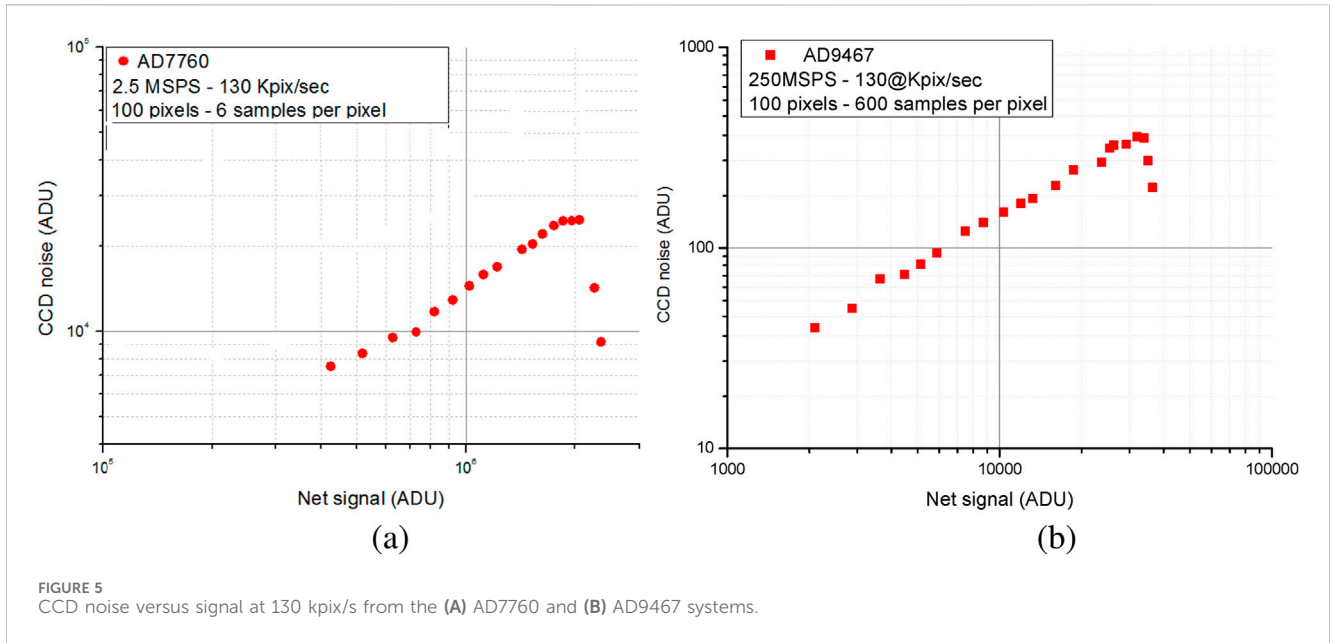


FIGURE 5
CCD noise versus signal at 130 kpix/s from the (A) AD7760 and (B) AD9467 systems.

overscan pixels. The clamp period was removed automatically during the preprocessing stage in the two DCDS systems.

4 Characterization results

According to [Janesick et al. \(1987\)](#), the PT method is a valuable tool for characterizing CCD imaging systems as it enables evaluation of the linearity, RON, dark current, SNR, and DR, among other parameters. The resulting pixel value S is determined using [Equation \(2\)](#) based on the average number of incident photons per pixel (P), quantum efficiency (η_e), quantum yield gain (η_i), sensitivity of the sense node of the output amplifier (S_v), source follower gain (A_{SF}), CDS gain (A_{CDS}), and ADC gain (A_{ADC}). The detector input is quantified in units of incident photons, and the final output is obtained by converting each pixel signal to a digital number represented by S (in ADUs). Instead of measuring the individual transfer functions, all are combined into a single transfer function given by [Equation \(3\)](#). The noise is calculated from the standard deviation (SD) of the pixel values from the subarray after removing the offset value. Furthermore, the total noise, which includes RON, shot noise, and fixed-pattern noise (FPN), is the quadrature sum of the individual noise sources ([Equation \(4\)](#)).

$$S = P \cdot \eta_e \cdot \eta_i \cdot S_v \cdot A_{SF} \cdot A_{CDS} \cdot A_{ADC}. \quad (2)$$

$$K = \frac{S(\text{ADU})}{\sigma_{\text{shot}}^2}; \quad \eta_i = 1. \quad (3)$$

$$\sigma_{\text{total}}^2 = \sigma_{\text{RON}}^2 + \left[\frac{S}{K} \right]^2 + [P_N \cdot S]^2. \quad (4)$$

The PTC is used to determine the detector's gain constant by converting the relative digital numbers from the detector to absolute units of electrons; this includes all data points spanning the DR from those with minimal light exposure to saturation. Typically, the exposure time is varied while maintaining the charge integration period and frame readout time constant in the PTC sequence. The

noise is then calculated from the SD of the pixel values from the subarray after removing the offset value. [Figure 5](#) shows the relationship between the CCD pixel noise and net signal, providing insights into the tradeoffs between noise and signal levels in CCD systems when using different ADCs. The CCD saturation levels were determined from the CCD noise for both DCDS systems.

[Table 1](#) shows the K and FWC values obtained for the two readout systems compared with those for the analog Monsoon CDS. The FWCs obtained are in concordance with the values provided by the manufacturers (typically 150,000 e). The readout at 223 kpix/s was not possible from the AD7760 ADC owing to limitations. The K values obtained at 130 kpix/s for the analog CDS system, DCDS AD7760, and DCDS AD9467 were 0.46, 0.046, and 3.93 e/ADU, respectively.

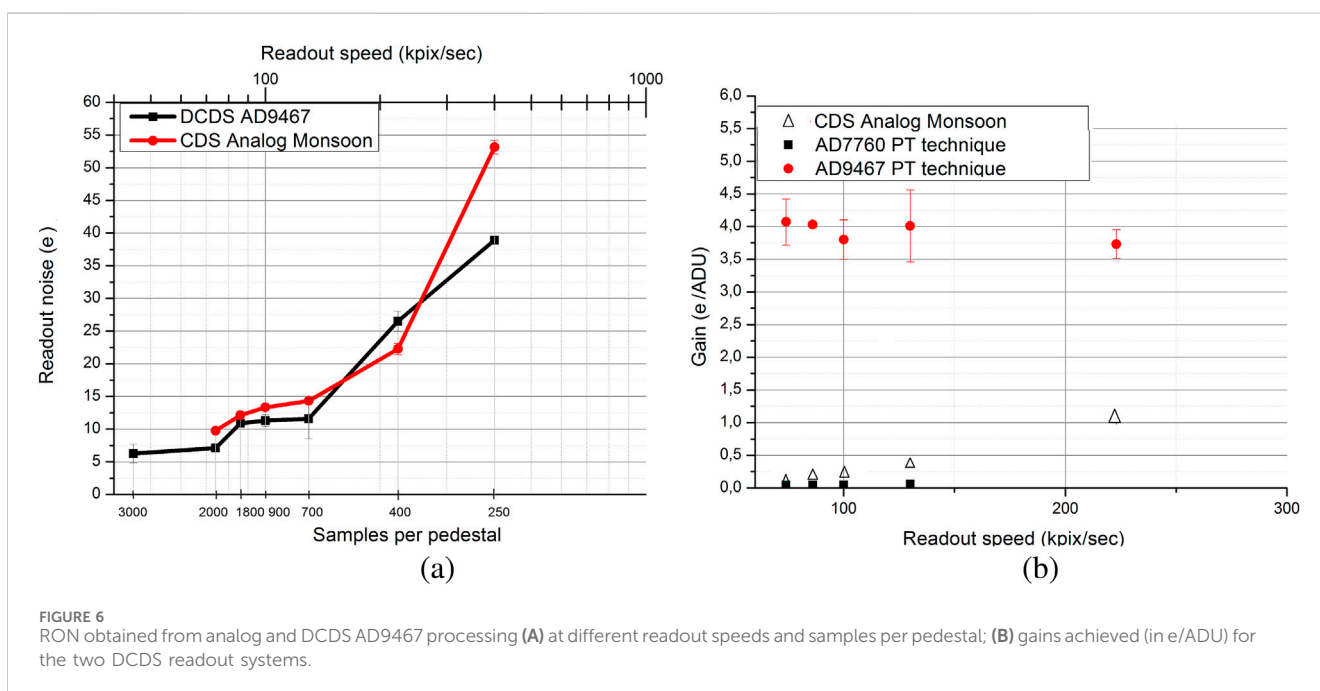
[Clapp et al. \(2016\)](#) emphasized optimization of the weighted averaging approach and characterized the system performance using the unsettled samples within the pixel period. Considering this work as the reference, the PT method was applied along with different samples per pixel at 130 kpix/s. However, this produced an undesirable effect related to the signal level. Although the reference and signal regions are clearly differentiable from the clamp and settling periods at low signal levels, these intervals expand at high signal levels and invade the regions corresponding to the reference and signal samples. Consequently, the CCD noise increases for higher signal values.

RON was calculated from the SD of the pixels in the overscan region. [Figure 6](#) presents performance comparisons of different readout techniques in terms of noise and gain, which are critical parameters for optimizing the CCD readout. The RON decreases as the number of samples per pixel increases, resulting in an RMS noise value of 6.26 e at 45 kpix/s, and gradually increases with readout speed. The RON obtained with the DCDS AD9467 is an improvement over that obtained with the analog Monsoon CDS system for a wide range of readout speeds. The RON obtained with the DCDS AD7760 is considerably higher at 130 kpix/s, with an out-of-scale value (285 e

TABLE 1 Performance comparisons between the three systems at different readout speeds.

Readout speed (kpix/s)	DCDS AD7760 PT (20* - 6**)		DCDS AD9467 PT (1,200* - 700**)		Analog Monsoon CDS PT	
	FWC (e)	K (e/ADU)	FWC (e)	K (e/ADU)	FWC (e)	K (e/ADU)
74	133,757	0.07± 0.01	142,450	4.07± 0.35	51,904***	0.20± 0.01
86	134,958	0.05± 0.01	141,050	4.03± 0.04	64,487***	0.25± 0.01
100	145,668	0.05± 0.02	134,900	3.80± 0.30	77,184***	0.32± 0.04
130	143,789	0.06± 0.02	140,570	4.01± 1.05	115,306***	0.45± 0.02
223	No samples	No samples	136,932	3.73± 0.22	146,572	1.07± 0.04

* indicates the total number of samples per pixel at the readout speed. ** indicates the number of samples selected per pixel. *** indicates the FWC limited by the video board ADC. DCDS, digital-correlated double sampling; CDS, correlated double sampling; PT, photon transfer; K, gain; e/ADU, electrons per analog-to-digital unit.



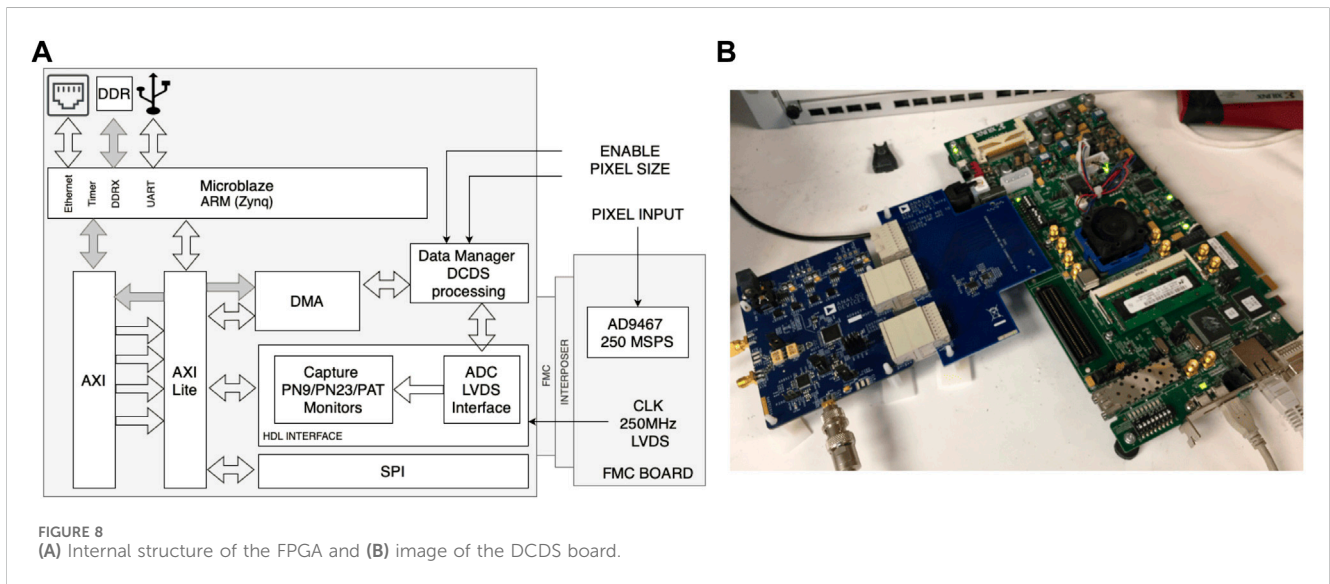
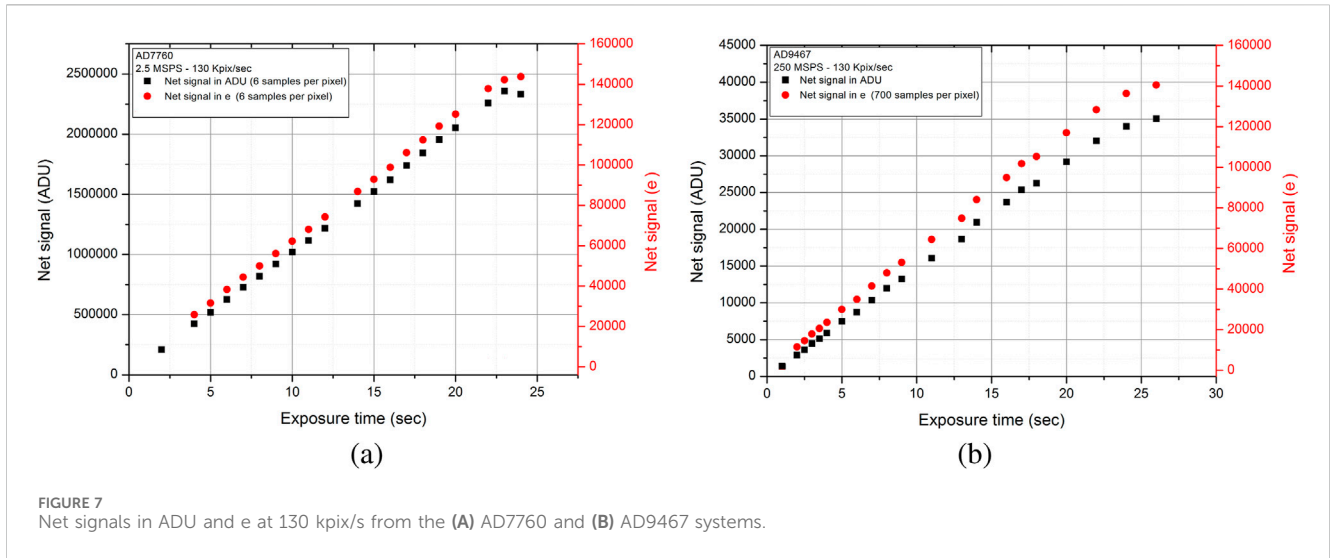
with $K = 0.06$ e/ADU) owing to the limitation of the maximum selected samples per pixel (6 samples) compared to the 700 samples per pixel selected for the AD9467. The number of samples per pixel is a crucial consideration for determining the performance at any given pixel rate, suggesting that careful control over the sampling can further influence the RON and overall system performance.

Figure 7 illustrates the net signal increases with exposure time for the two ADCs. Despite the differences in sampling rates, the net signal values in terms of electrons (red points) show similar ranges (up to 150,000 e) for both ADCs. Furthermore, saturation occurs after 25 s of exposure, demonstrating extremely good linearity. The SNR value of 19,853 (86 dB) obtained with AD9467 at 74 kpix/s was calculated as the ratio of the FWC to the RON of the detector system. The analog Monsoon CDS system provided an SNR value of 5,318 (75 dB) at the same frequency (the result was limited by the video board ADC).

The FPN is caused by the variations in charge collection from one pixel to another. Although the FPN may appear to be insignificant, with only a 1% pixel non-uniformity observed in

CCD detectors, it significantly impacts the sensor’s DR and dramatically limits the signal-to-noise performance. Typically, the FPN is eliminated from images prior to data processing by subtracting consecutive images. This expands the region limited by the shot noise and enables gain calculation across the full DR of the system. The FPN is computed by subtracting the photon variance and RON from the overall noise, where $\sigma\Delta$ is the SD of the difference, as noted in Equation (5). The FPN is obtained as the pixelwise difference between two identical frames captured consecutively at the same exposure level; thus, an FPN value (P_N) of 0.01 was obtained for the synchronized AD9467 board with the analog system in the CCD region of interest. However, P_N could not be determined for the AD7760 platform owing to the lack of synchronization with the analog system. Thus, the value obtained with the analog system was used in the AD7760 PTC analysis.

$$\sigma_{FPN}^2 = \sigma_T^2 + \frac{\sigma_A^2}{2}, \quad \sigma_{FPN} = P_N \cdot S. \quad (5)$$



5 DCDS implementation on an FPGA

Previously, DCDS characterizations were conducted using offline DCDS Python algorithms involving analysis after data collection. In this section, we propose the implementation of real-time DCDS, where the data are instantaneously processed during acquisition. This approach enables immediate noise reduction and error correction, thereby enhancing the accuracy and quality of the results in real time. In this regard, the DCDS was implemented on a versatile and powerful platform that allows both high-performance processing and customized hardware acceleration. The Zynq-7000 FPGA system-on-a-chip (SoC) device from AMD Xilinx ZC706 (Xilinx, 2024) combines a dual-core ARM Cortex-A9 processing system with Xilinx programmable logic and is tightly integrated on a single device. Figure 8 illustrates the block diagram of the data acquisition and processing system as well as the electronic board used for the DCDS implementation.

The DCDS system is built around a customized hardware data manager IP core (Figure 9A). The algorithm offers great flexibility for weighting the ADC samples on each pedestal based on the input frequency of the DCDS signal. The operating mode of the IP core can be controlled with the clock ADC and three external signals, namely, the enable signal that initiates the CCD row, pixel size, and DCDS signals that provide the pixel rate information. The IP core module defines the ADC sample operating mode in the pixel region of interest; the samples captured in the reference region operate in the up-accumulator mode, while the samples captured in the signal region operate in the down-accumulator mode. The resulting values are then divided by the number of samples in the signal region. The operations are performed during the clamp period, and the results are output after 30 ADC clock cycles. At the end of the signal region, the final pixel value is transmitted via direct memory access (DMA) to the DDR memory. The DCDS post-implementation FPGA design and usage of FPGA resources are shown in Figure 9B. Less than 10% of the Zynq resources

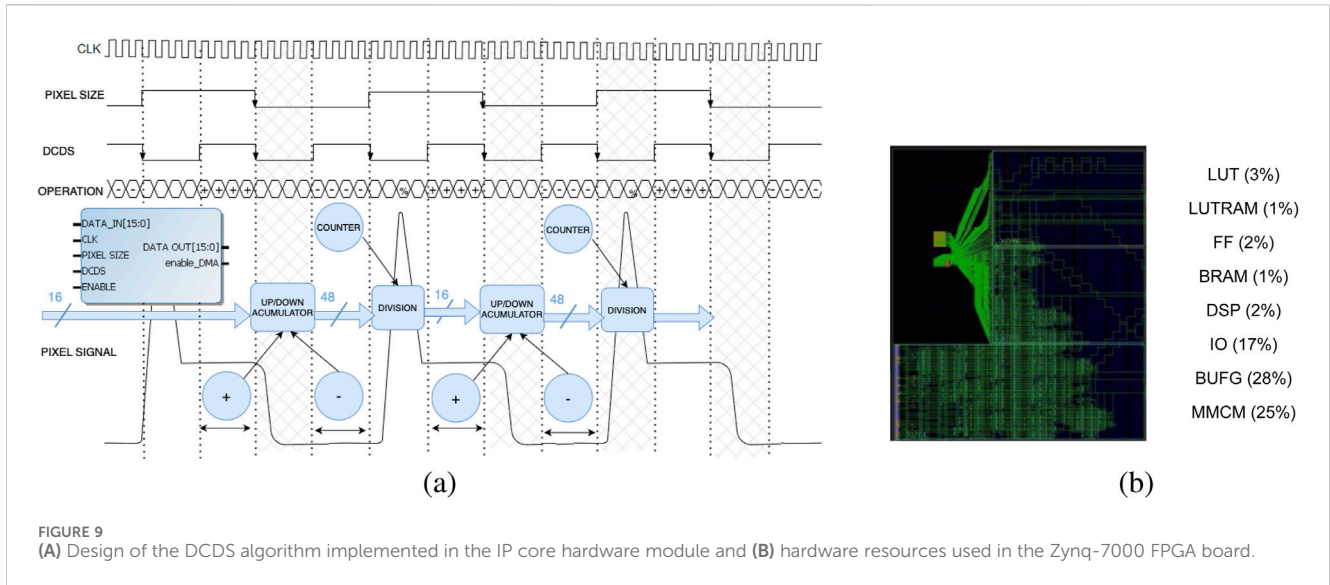


FIGURE 9 (A) Design of the DCDS algorithm implemented in the IP core hardware module and (B) hardware resources used in the Zynq-7000 FPGA board.

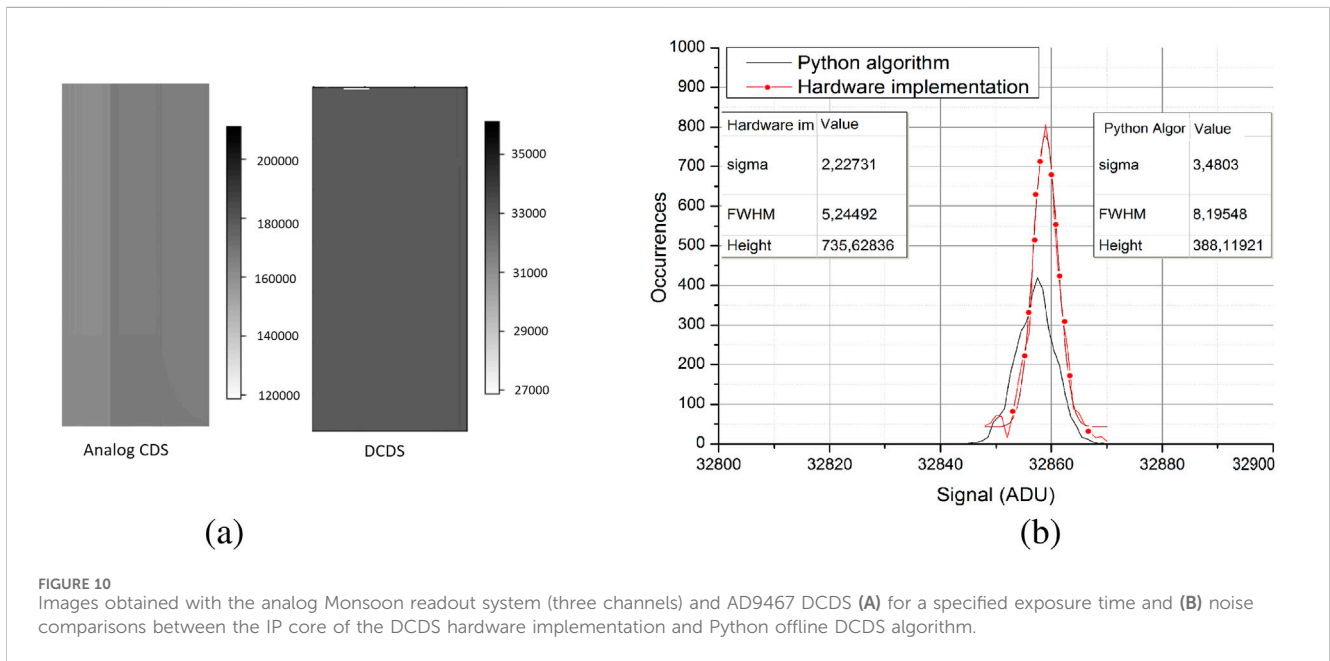


FIGURE 10 Images obtained with the analog Monsoon readout system (three channels) and AD9467 DCDS (A) for a specified exposure time and (B) noise comparisons between the IP core of the DCDS hardware implementation and Python offline DCDS algorithm.

are used in the implementation, ensuring that the hardware design fits comfortably within the selected FPGA. The behaviors of the different IP cores comprising the DCDS readout were tested through simulations using the Vivado-integrated testbench. The final step was to provide a synthetic CCD video waveform for verification.

Figure 10A compares the different readout techniques and corresponding noise performances for the generated images. As examples, an image of the entire CCD under analog readout and a small CCD pixel size under DCDS readout are presented. Figure 10B shows a further comparison of the noise performances of a Python-based offline DCDS algorithm and the hardware-based DCDS implementation. To analyze the two methodologies, the same number of pixels from the overscan region were selected for each method, and the noise performances were evaluated by calculating the standard deviation of

the selected pixels. The offline DCDS Python algorithm shows a higher noise characteristic ($\sigma = 3.5$) with a wider distribution and a higher σ value compared to the DCDS hardware implementation ($\sigma = 2.3$). Quantization issues are not a concern in this comparison as both methods use the same ADC. Assuming equal K values, the numbers of samples per pixel may vary between the methods, and this could be the key parameter for the observed differences in the results. Nevertheless, the outcomes demonstrate the absence of significant rounding errors and background electronic noise reduction of up to 37%.

Finally, according to the Monsoon report, the power dissipation for the analog Monsoon acquisition board with 12 channels states a is $25.1 \text{ W} \pm 5\%$, of which $12.5 \text{ W} \pm 5\%$ of the total power corresponds to the common circuitry shared between all channels and is equal to the power needed per channel. Consequently, the estimated power

consumption per channel was $13.6 \text{ W} \pm 5\%$. The power dissipation of the AD9467 DCDS readout system in the acquisition mode was $7.1 \text{ W} \pm 5\%$, which is much lower than that required for a single channel of the analog Monsoon board (47% power reduction).

6 Discussion

Developing an effective DCDS algorithm requires a thorough understanding of both the signal characteristics and noise sources, which adds complexity to the readout system design. According to the dataset of the Teledyne E2V CCD used in this study (Photronics, 2024), it is possible to achieve a noise level of approximately 4 e at 50 kpix/s . The results obtained for the AD9467 DCDS and Monsoon analog readout systems at 74 kpix/s (7.1 e and 9.7 e , respectively) during characterization approach this value. The use of low-power operational transconductance amplifiers and power scaling capabilities allow further optimization of the performances of the signal acquisition amplifiers, which are mainly developed for analog CDS readouts (Coln and Mueck, 2020). In our research, the noise observed at low frequencies is attributable to an issue with the preamplifier's bandwidth, which does not allow adequate responses at these frequency levels. This work experimentally demonstrates that the "weighted samples" method can significantly reduce the RON at low signal levels. Concurrently, research on the design of low-noise differential preamplifiers or even an ASIC preamplifier that can be mounted next to the detector also offers significant advantages for developing low-noise systems. DCDS readout systems have been shown to offer optimal strategies for selecting CDS timings, highlighting the linearity of the operations and their impacts on the final pixel values (Weatherill et al., 2019). However, many studies still aim to suppress flicker noise in the CCDs using special methods that require experimental validation (Stefanov, 2015).

7 Conclusion

Although CDS techniques have shown significant promise in reducing RON, challenges remain in balancing noise suppression with system complexity and power efficiency, particularly for high-density applications. Advancements in DCDS approaches have emerged as solutions to the limitations of traditional analog methods, particularly in large-scale systems. DCDS offers enhanced capabilities through real-time processing, greater flexibility, and improved precision, thereby overcoming many limitations of the traditional analog CDS implementations.

In this study, the challenge of optimizing the CCD readout was addressed by implementing advanced hardware and digital processing techniques. The goal was to validate innovative algorithms by analyzing and processing the digital samples obtained from CCD readings and explore the potential of digital processing for enhancing performance. To this end, a hardware system was developed for implementing the DCDS technique and was characterized across the full DR of the CCD. This system was built using a 16-bit ADC with a high sample rate of 250 MSPS , which provided significant improvements over a slower 24-bit ADC operating at 2.5 MSPS . As the number of samples per pixel

increased, the RON decreased, which resulted in a minimal RMS noise level of 6.26 e at 45 kpix/s for the AD9467 system. These results show noise level improvements (9.7 e) achieved with analog processing at equivalent readout speeds. The PT method was crucial in assessing the performance of the DCDS readout. The experimental results indicate that the number of samples per pixel, their positions within the pixel readout cycle, and the pattern noise factor are essential parameters for achieving accurate K values. It is also noted that high signal levels can introduce difficulties, such as expanded transition regions and unreliable PT parameters, due to unwanted transition samples in the reference and/or signal regions.

Finally, the DCDS technique was designed around a customized hardware data manager IP core, offering great flexibility for weighting the ADC samples on each pixel pedestal. A real-time DCDS CCD readout system implemented using a Zynq FPGA demonstrated improved noise performance ($\sigma = 2.3$) compared to offline processing ($\sigma = 3.5$). Moreover, the power dissipation achieved with the AD9467 board (7.1 W) represents a substantial improvement over the 13.6 W observed with a single channel of the Monsoon analog acquisition board. The preliminary images obtained from online DCDS processing are promising and encourage further development of the customized digital system for comprehensive CCD readout. Future research efforts will thus be focused on developing adaptive algorithms to dynamically adjust the DCDS parameters in real time based on the observed noise characteristics and environmental conditions during CCD readout. The selection of a low-noise preamplifier and its optimization are also possible improvements to reduce the noise at low frequencies.

Data availability statement

The original contributions presented in this study are included in the article/supplementary material; further inquiries can be directed to the corresponding author.

Author contributions

CC: conceptualization, data curation, formal analysis, investigation, methodology, resources, software, validation, visualization, writing—original draft, and writing—review and editing. JD: conceptualization, funding acquisition, investigation, project administration, supervision, validation, and writing—review and editing.

Funding

The authors declare that financial support was received for the research, authorship, and/or publication of this article. The research leading to these results were supported by Comunidad de Madrid undergrants (SPACETEC-CM S2013 ICE-2822, MINECO FPA2015-68048) and Centro de Excelencia Maria de Maeztu (MDM-2015-0509).

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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