



Electrodeposition as an Alternative Approach for Monolithic Integration of InSb on Silicon

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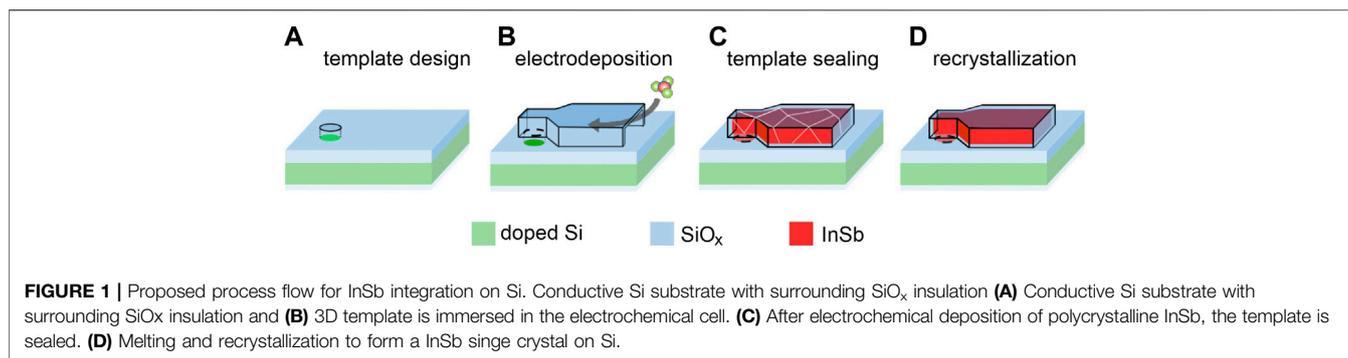
High-performance electronics would greatly benefit from a versatile III-V integration process on silicon. Unfortunately, integration using hetero epitaxy is hampered by polarity, lattice, and thermal expansion mismatch. This work proposes an alternative concept of III-V integration combining advantages of pulse electrodeposition, template-assisted selective epitaxy, and recrystallization from a melt. Efficient electrodeposition of nano-crystalline and stoichiometric InSb in planar templates on Si (001) is achieved. The InSb deposits are analysed by high resolution scanning transmission electron microscopy (HR-STEM) and energy-dispersive X-ray spectroscopy (EDX) before and after melting and recrystallization. The results show that InSb can crystallise epitaxially on Si with the formation of stacking faults. Furthermore, X-ray photoelectron (XPS) and Auger electron (AE) spectroscopy analysis indicate that the InSb crystal size is limited by the impurity concentration resulting from the electrodeposition process.

Keywords: integration, InSb, electrodeposition, recrystallization, III-Vs, TASE

INTRODUCTION

Globally, one of the fastest-growing industries is electronic devices manufacturing based on silicon technology. With an increasing demand for faster, smaller, and better-performing devices, growth CAGR (compound annual growth rate) of 4.6% from 2020 to 2027 for this field is expected. Nonetheless, recently both academia and industry have focused efforts on the search for alternative technologies for which performance in the long run could considerably surpass that of Si (Ramirez et al., 2020), especially in more futuristic applications like quantum computing. These include III-V semiconductors for sensing and high-speed electronics where high value is created (Riel, 2017). The best solution would be to combine the advantages of Si and III-Vs (Hopkinson et al., 2013). However both economic and technological difficulties, like crystal lattice and polarity mismatch, have prevented the integration of foreign materials directly on a silicon platform.

One approach to address this problem, the so-called Template-Assisted Selective Epitaxy (TASE), was developed by IBM a few years ago (Schmid et al., 2015). By directing the growth by an oxide template and using metal-organic vapor phase deposition (MOCVD) to fill the designed structures, successful integration of InGaAs, InP, GaSb, etc. for high-performance MOSFETs or lasers on silicon was possible. However, MOCVD growth is limited by its low growth rates, difficulty of filling high aspect ratio structures, and the use of toxic precursors. Furthermore, not every III-V semiconductor is well suited for this technique. Examples for challenging materials include aluminum containing compounds due to the high sticking coefficient of Al on the mask material and antimonides due to



the small process window to suppress droplet formation. InSb is a particularly interesting material with properties such as one of the smallest direct band gap (0.17 eV at 300 K) and highest electron mobility ($77,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) among III-Vs and can ensure applications in a wide range of modern devices, starting from terahertz (Liu et al., 2018a) and gamma rays detectors (Hishiki et al., 2005), through IR (Xie et al., 2016; Shi et al., 2019) and neutron-resistant Hall (Jankowski et al., 2019) sensors, ending on topological quantum devices for Majorana investigation (Chen et al., 2021). As an alternative synthesis path, electrochemical technique is considered since it was demonstrated to fill different shapes and sizes of templates efficiently, with control over composition, and using a simple set-up with water-based electrolytes (Hnida et al., 2015; Hnida et al., 2019). However, due to the characteristics of the InSb electrodeposition, the obtained material is polycrystalline, which significantly limits its practical use. To overcome this, concepts borrowed from micro zone recrystallization (Billings, 1969) and rapid melt growth (Liu et al., 2018b) can be applied. Here, the samples are subjected to a short high temperature step exceeding the melting temperature. During this step the polycrystalline sample melts and recrystallizes from a seed interface, resulting in a single crystalline structure with epitaxial relationship to the substrate.

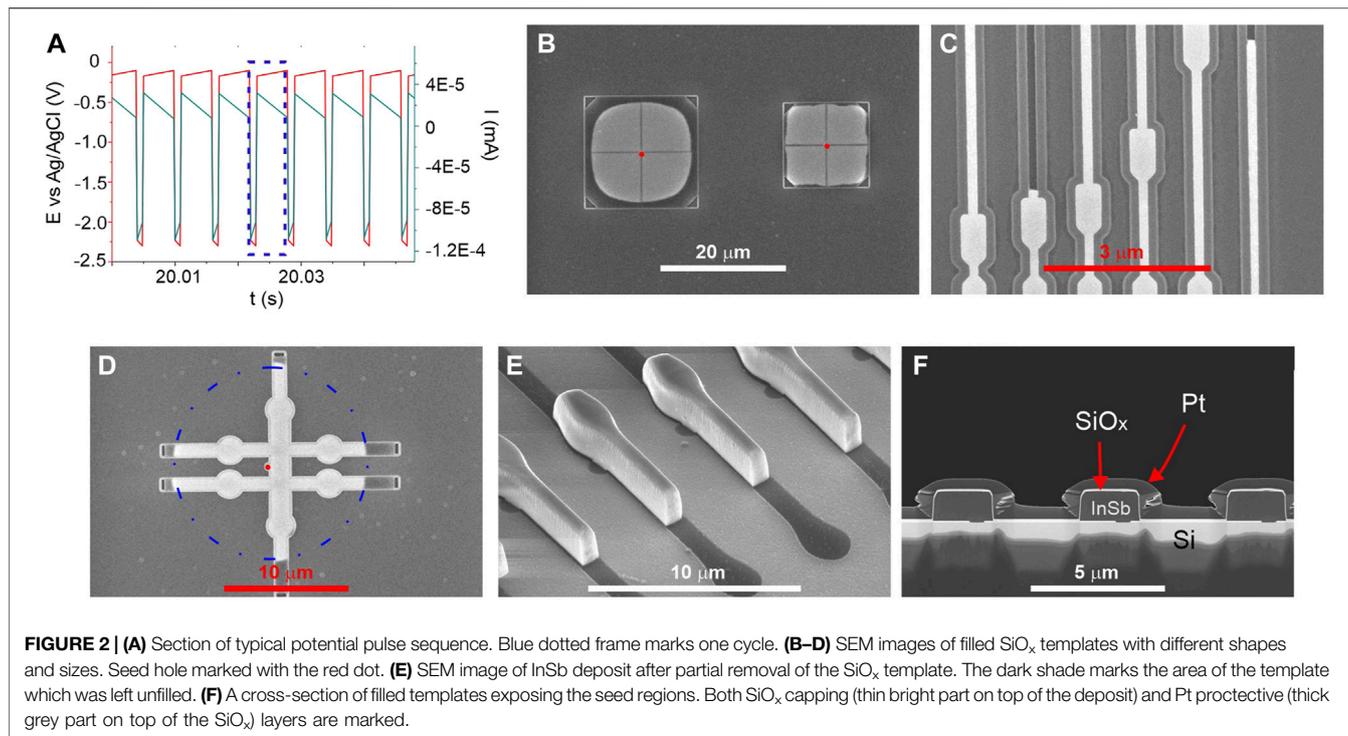
The goal of this work is to directly integrate InSb on a silicon platform. To reach that we propose combining the three techniques, namely TASE, pulse electrodeposition, and recrystallization. The proposed process is designed to resolve the identified issues and is summarized in **Figure 1**. One of the key aspects is that the low melting point of InSb could allow for a CMOS compatible process.

MATERIALS AND METHODS

One of the requirements for electrodeposition of InSb on silicon is to provide a conductive electrode. In the presented work we used highly doped silicon wafer as global working electrode to simplify the fabrication process, while formation of addressable electrodes would require additional processing steps. Silicon wafers (001) n-type for two sets of templates having larger or smaller structures were prepared. For template fabrication, holes were etched in 100 nm thick SiO_x on Si by reactive ion etching

(RIE) to define the electrode/seed area. Then, a 1,350 nm thick bis-benzocyclobutene (BCB, Dow) layer was spin coated and cross-linked at 320°C. Subsequently, the BCB layer was patterned with the layout of template structures, etched using RIE, and coated with a 150 nm thick SiO_x shell by plasma enhanced chemical vapor deposition (PECVD). Finally, openings were patterned on the template structures and etched into the SiO_x shell exposing the BCB layer. The remaining BCB layer was etched using peroxide/sulfuric acid 1:3 solution, resulting in hollow template structures. The as-prepared substrate was dipped for 12–15 s in diluted (2.5%) HF to remove the native oxide on the exposed Si surfaces within the channels before electrodeposition.

All electrochemical syntheses were performed in a water-based electrolyte containing 0.06M InCl₃ (Sigma Aldrich, >98%), 0.045M SbCl₃ (Sigma Aldrich, ≥99%), 0.2M citric acid (Sigma Aldrich, ≥99%), and 0.17M sodium citrate (Sigma Aldrich, ≥99%) at room temperature. Both citric acid and sodium citrate were used as complexing agents to bring reduction potentials of indium and antimony ions closer to each other. The electrodeposition experiments were carried out using the potentiostat (BioLogic SP300) with a three-electrode setup. An Ag/AgCl (3M NaCl) electrode as a reference electrode (Ref) and Pt wire as a counter electrode (CE) were employed. SiO_x template as a working electrode (WE) was installed at a distance of 1.5 cm from the CE electrode. Unless otherwise stated, all potentials refer to the Ref. The fabrication of InSb nano and microstructures was performed using a cathodic pulse with $E_{\text{on}} = -2.3 \text{ V}$ followed by $E_{\text{off}} = -0.1 \text{ V}$. The potentials of “on” and “off” pulses were chosen based on Linear Sweep Voltammetry (LSV) and Open Circuit Potential (OCP) measurements on bare n-Si, respectively. The duration of pulse “on” and “off” were 1 and 5 ms, respectively, based on previous research (Hnida et al., 2015). During pulse “on” the reduction of In and Sb citric complexes occur, while during pulse “off” replenishment of electrolyte near the working electrode surface and dissolution of the top surface of deposit happen (Rajska et al., 2021). Section of the typical electrodeposition pulse sequence is presented in **Figure 2A**. Blue dotted frame marks one cycle. Slight variations in potential and current (red and green lines, respectively, slope especially visible for pulse “off”) are related to the data acquisition. The total deposition times ($(t_{\text{on}} + t_{\text{off}}) \times \text{number of cycles}$) were kept in a range of 12–240 s depending on the size and shape of the



oxide template and overall geometrical area of the working electrode.

For a thin intermediate InSb layer synthesis, MOCVD technique was implemented. Selective epitaxy of InSb was carried out using trimethylindium (TMIIn), and trimethylantimony (TMSb) at V/III ratio 100 at 430°C for 65 s, followed by 25 s of Sb deposition to further suppress the presence of In droplets.

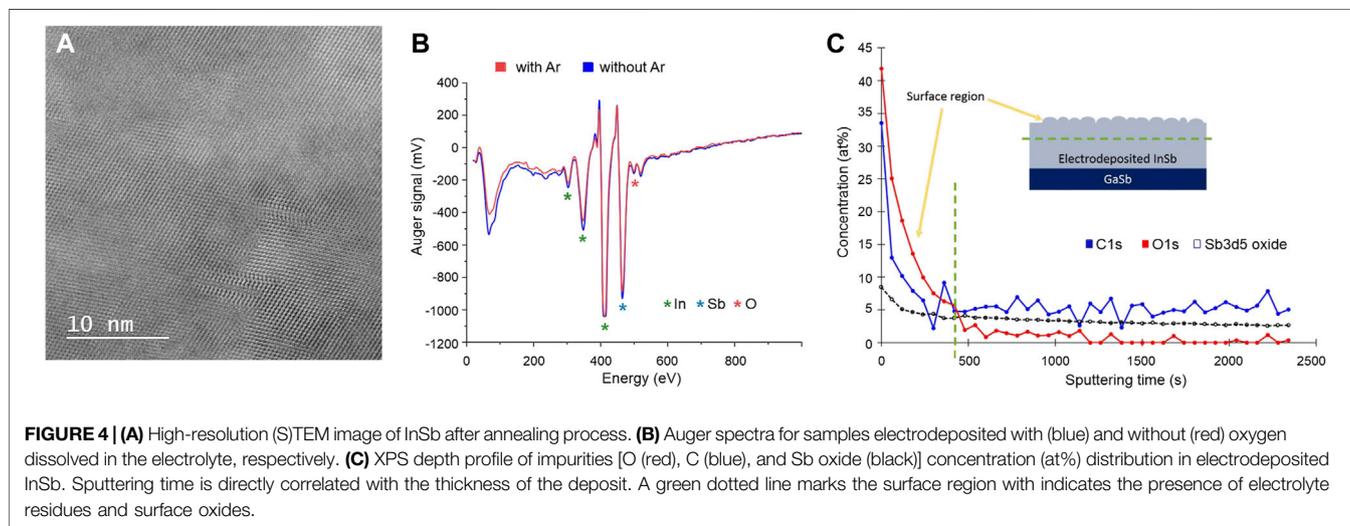
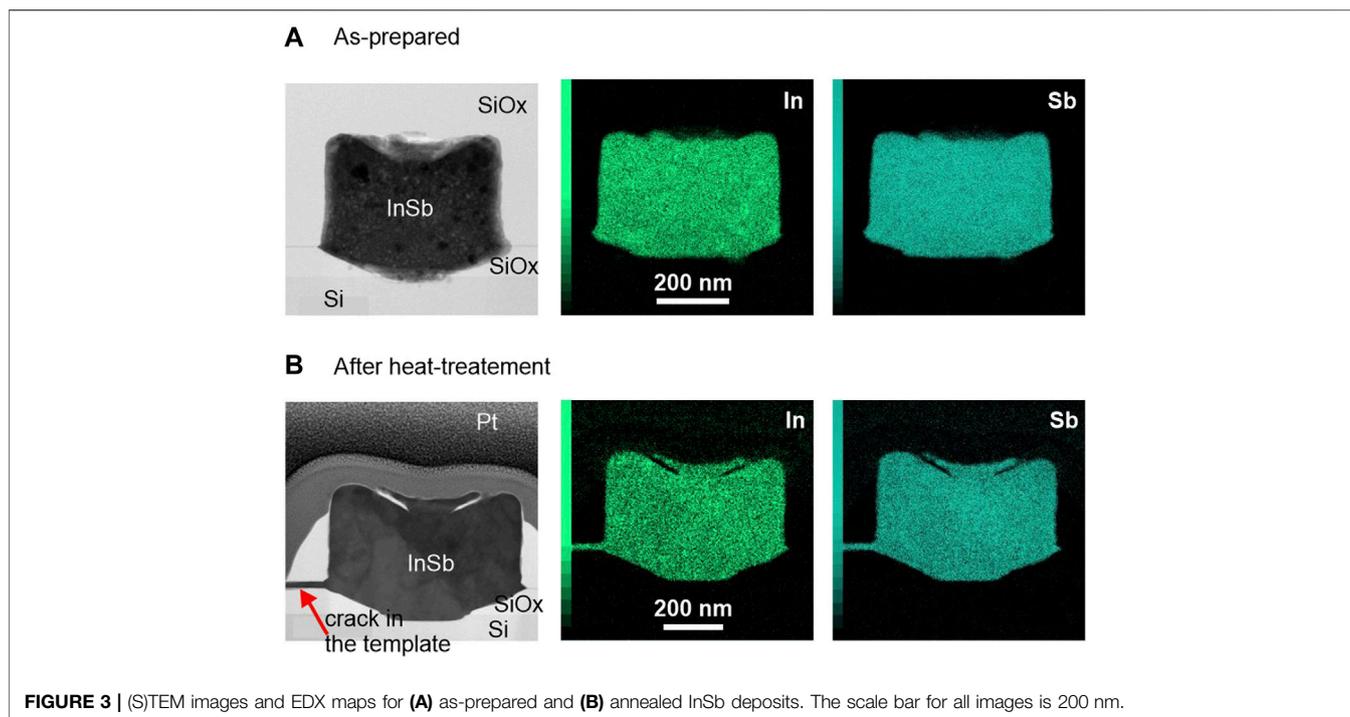
The melting process was performed on SiO_x -capped samples at 535°C , 50 mbar for 2 s. The system was calibrated prior to the process and offset in the measured temperature was considered. After annealing, the SiO_x capping layer was removed using a combination of RIE and HF etching (either wet or vapor), and the morphology, crystallinity, and chemical composition were characterized using scanning electron microscopy (SEM, Hitachi SU8000) and analytical (scanning) transmission electron microscope ((S)TEM, JEOL ARM200F) equipped with energy-dispersive X-ray spectroscopy detector. Lamellas for (S)TEM-EDX analysis were prepared using the focus ion beam technique (Dual beam FIB/SEM, FEI Helios NanoLab 450S). Prior to the lamella preparation samples were covered with 250 nm of SiO_x . The samples have been measured under UHV condition with a Varian Auger system equipped with a TPIS plasma gun.

RESULTS AND DISCUSSION

In preliminary studies, we tested different silicon wafer orientations and doping levels. No change in morphology and composition between deposits was observed as long as ohmic

contacts could be established. InSb deposition on BHF passivated Si showed a high nucleation density and dense film formation. However, the film adhesion was low and with the buildup of mechanical strain in the film, leading to delamination with increasing thickness already in the plating solution (Hnida-Gut et al., 2021). **Figure 2** shows representative SEM images of InSb deposited in the template structures. Here, loss of adhesion and strain as encountered with planer films is not a limiting factor anymore. **Figure 2B** shows two squares composed of four quadrants each with the seed located in the center, and the template opening at the corners. The deposition process is very selective, and the InSb is deposited with high uniformity in each quarter. Templates with up to $10\ \mu\text{m}$ large free-standing structures were successfully filled, while larger ones collapsed due to capillary forces during the fabrication process. The smallest structures fabricated and filled (**Figure 2C**) have line width down to 120 nm. **Figure 2D** illustrates uniform filling of the intended Hall bar structure with the seed area indicated as red point and a dashed circle as reference. **Figure 2E** shows a tilted view image of a sample where the SiO_x was partially removed. The smooth top surface is a result of the replication of the inherently low surface roughness of the spin coated BCB film, while the sidewall roughness originates from the BCB etching process. Cross-sections from several structures are shown in **Figure 2F**, confirming the absence of gaps, voids, and cracks in the InSb.

After demonstrating the successful electrodeposition on InSb on Si, and according to **Figure 1**, step D follows with melting and controlled recrystallization of the InSb from the seed area. First, the chemical composition is accessed before and after the melting step, followed by further chemical and structural analysis. **Figure 3** shows (S)TEM cross-section images of two samples



(as-prepared and annealed, respectively) which were cut across the samples such as to expose seed areas and including the InSb-Si interface. We note that the unexpected roughness of the top surfaces stems from an artefact during the fabrication process. (S)TEM-EDX mapping was performed to investigate the distribution of In and Sb elements (**Figure 3**, center and right-side panels) in the deposited volume before and after annealing for 2 s at 535°C. In both samples the distribution of In and Sb atoms is uniform with no detectable phase separation. The In/Sb ratio for the as-prepared sample was 45/55 ($\pm 10\%$) and remained constant after annealing. In **Figures 3A,B** a small crack is visible on the left (marked with the red arrow) which was created during

the annealing procedure, caused by volume expansion of the melt or thermal stress in the oxide template. Interestingly, the resulting void is completely filled with InSb, thus confirm the melting of the deposit. After the RTA process voids in the InSb structures were frequently detected by SEM inspection, indicating loss of material. This observation was also reported in Menon et al. (2021) and needs further investigation.

Structural analysis using bright field (BF) HR-(S)TEM revealed unexpectedly that both samples remained throughout nanocrystalline with no significant differences in the size of the crystals (**Figure 4A**), despite the fact that the melting was indeed achieved. In addition, the anticipated recrystallization from the Si

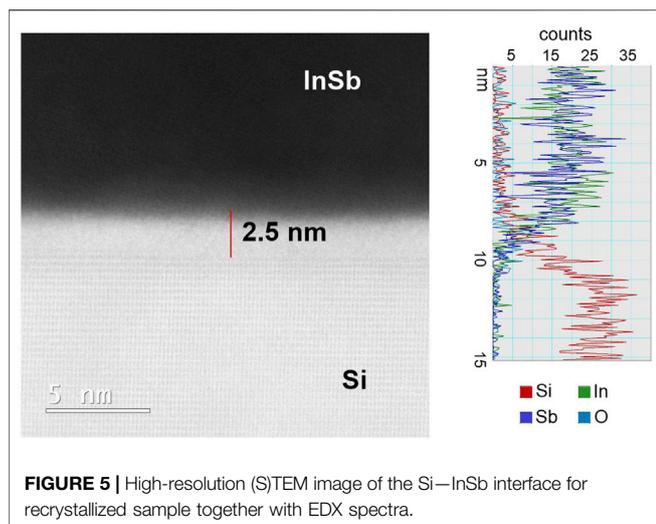


FIGURE 5 | High-resolution (S)TEM image of the Si–InSb interface for recrystallized sample together with EDX spectra.

seed interface did not take place. Regarding the first observation, a possible explanation might be found in the process of diamond crystallization in metal-carbon systems. Palyanov et al. recently reported that oxygen can greatly affect the crystallization (Palyanov et al., 2020). They found that the concentration of O_2 higher than 0.25 wt% can lead to spontaneous nucleation events which hinders crystal growth. As oxygen is present in the water-based electrolyte used for InSb electrodeposition, it is plausible that impurity induced nucleation is limiting the InSb crystallization. The common way of removing oxygen dissolved in the electrolyte is to deoxygenate it with inert gas (such as N_2 or Ar) before and during the synthesis. To explore this hypothesis, two electrodeposition processes were conducted (namely with and without O_2 dissolved in the electrolyte), after which samples were immediately stored in a glove box. Both samples were subjected to Auger electron spectroscopy measurement to determine the influence of O_2 in the electrolyte on its content in the InSb deposits. Both spectra are presented in **Figure 4B** and reveal that regardless of whether the electrolyte used in the synthesis was deoxygenated or not, significant amounts of oxygen are incorporated. To further confirm the intrinsic oxygen and/or carbon contamination in electrodeposited InSb, XPS analysis was performed using a GaSb as substrate for Sb-signal as reference. Due to overlapping spectra for Sb and O, the exact deduction of how much oxygen is dissolved in the InSb deposit is, however, challenging. The XPS depth profile is shown in **Figure 4C** and confirms high concentrations of oxygen, carbon, and antimony oxide on the surface and in the bulk of the electrodeposited InSb. Impurity concentrations are stable around 5.2 at%, 0.8 at%, and 3.1 at% for C, O, and Sb oxide, respectively, which can explain the observed suppression of crystal growth.

As noted, the anticipated recrystallization from the Si interface is not observed, and in addition it is expected that the liquid melt should lead to a dissolution and therefore local etching of the Si surface which is also not observed in **Figure 3B**. A BF HR-(S)TEM of the interface of the annealed sample is presented in **Figure 5** and reveals a 2.5 nm thick amorphous (barrier) layer between Si seed

(bottom bright part) and InSb deposit (dark part), whose presence inhibits epitaxial contact between the Si and the InSb melt and correspondingly also etching of the Si surface. The composition of the barrier was further evaluated using EDX, and together with the (S)TEM data indicates the presence of Si- and metal (In, Sb) oxides. The unhindered effectiveness of the electroplating suggests that the amorphous barrier layer acts mainly as material diffusion barrier and barrier for epitaxy, but not as effective electrical insulator. Despite its 2.5 nm thickness, direct tunneling, and more importantly trap assisted tunneling (TAT) can be significant at $\sim 1 \text{ Vnm}^{-1}$ in low density oxides. In fact, electron tunneling at high cathodic voltages was previously observed during Cu electrodeposition on thin native silicon oxide (Arrington et al., 2008). Moreover, the barrier may contain intrinsically conductive In or Sb oxides. To overcome the formation of a barrier layer, which might itself be intrinsic to the specific electrodeposition process, a modified strategy is demonstrated in the following section.

To demonstrate the overall validity of the concept illustrated in **Figure 1**, the formation of a barrier layer during electrodeposition must be excluded. This small modification is introduced by selectively depositing a thin intermediate layer of InSb using MOCVD in the Si seed areas. This guarantees an oxide free InSb-Si interface which serves in a later step as interface for the electrodeposition of InSb, and the subsequent steps demonstrated above. Instead of complex templates, arrays of vias in a SiO_x mask were patterned on Si (001) and used as a mask for MOCVD growth of small InSb crystals. The conditions of epitaxial growth were chosen to minimize the presence of In droplets on the InSb crystals, with randomly occurring In droplet still detectable (for detailed description please refer to **section 2** Materials and Methods). The resulting InSb seeds crystals are shown in **Figure 6A**. Each hole contains at least one InSb crystal protecting the InSb-Si interface from reoxidation processes. Directly after MOCVD synthesis, the electrodeposition process was performed in which each 100 nm-sized InSb crystallite was further overgrown by InSb, resulting in $>500 \text{ nm}$ sized domes (**Figure 6B**). Finally, the samples were capped with SiO_x . The results of (S)TEM-EDX analysis of as-prepared and melted/crystallized samples are presented in **Figures 6C–F**. The arrows in **Figure 6C** point to the crystalline InSb deposited by MOCVD (for better visibility marked with white dotted line) and to the nanocrystalline InSb deposited by ED. The surface roughness of the ED process is clearly visible around the perimeter of the mushroom. The corresponding EDX map in **Figure 6D** confirms a uniform composition of the ED part, but also a slight In rich area in the InSb seed which might be caused by a In droplet formed during MOCVD growth. The differences of intensities are simply a consequence of the variable lamella thickness, with the stem being thinner compared to the hemisphere. As expected InSb-Si interface is flat.

After melting and crystallization, the morphology changes significantly, as visible in **Figure 6F**. According to the phase diagram, the melted phase gets saturated with Si, leading to a dissolution of Si, confirmed by the presence of the inverted pyramidal structure bound by four Si $\langle 111 \rangle$ planes below the seed region. This melt-back etching is a well documented

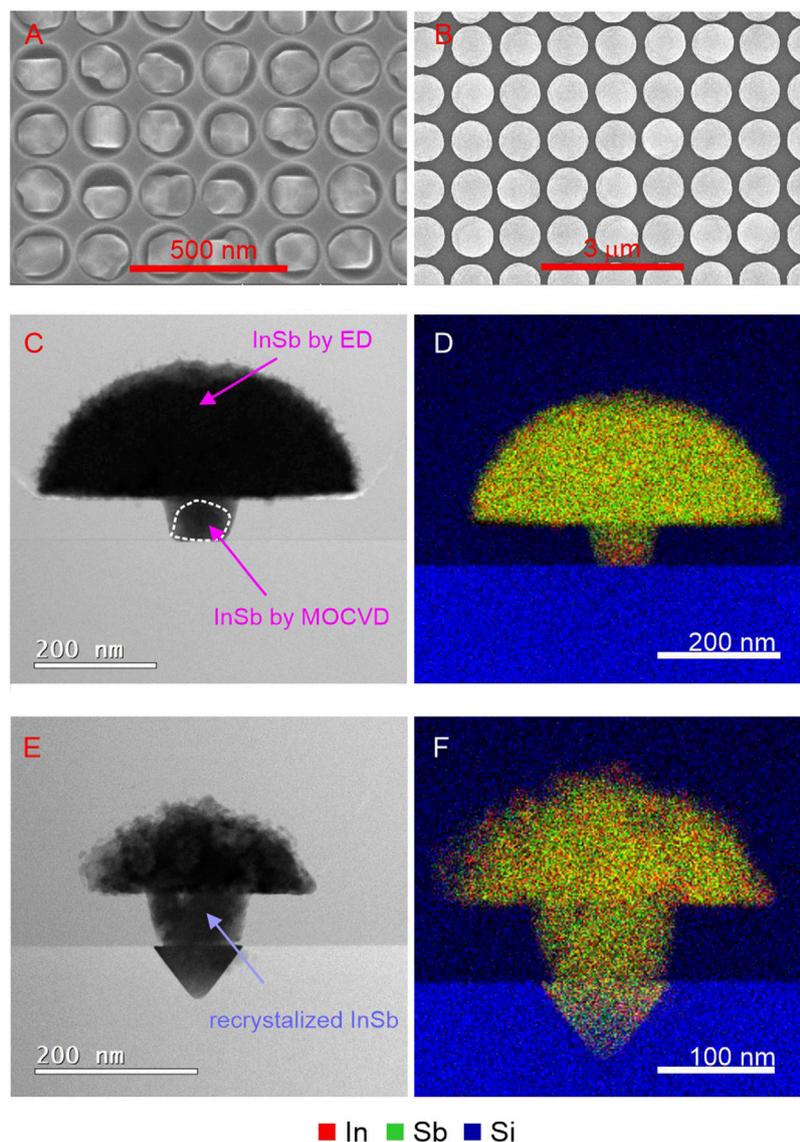


FIGURE 6 | (A) SEM images of dense array of InSb crystallites by MOCVD serving as seeds for later electrodeposition. (B) sparser array similar to (A) with the small InSb seeds after the electrodeposition step resulting in large InSb mushrooms. (C) (S)TEM cross-section image of a representative structure from (B) together with (D) EDX map of In, Sb, and Si elemental distribution. (E) (S)TEM image of (B) after melting and crystallization. (F) EDX map of (E).

phenomenon and is investigated in detail for gallium (Werner et al., 2014) and gallium nitride (Khoury et al., 2017) epitaxial growth on Si, for example. Upon cooling, the dissolved Si precipitates out again until reaching the equilibrium solubility limit. At first surprising is the large volume of Si that is melt-back etched, corresponding to approximately 15% of the entire InSb volume, by several orders exceeding the solid solubility limit of Si in In (Olesinski et al., 1985) and Sb (Olesinski and Abbaschian, 1985). A closer look at the structure after melting and crystallization reveals a much increased surface roughness along the perimeter and a correspondingly decreased radius of the hemisphere. This suggests that dissolved Si was diffusing through the InSb melt and precipitating out again on the opposing interface

during the melt phase. The etching process slows down when the stable $\langle 111 \rangle$ planes are formed, defined by the mask opening, but still continues at reduced speed as is noticeable by the underetching of the mask pattern. EDX measurements (Figure 6F) could not confirm the hypothesis by revealing a distinct Si signal at a periphery, due to the overlap of the Si signal stemming from the SiO_x capping layer, and due to the likelihood of the Si forming a SiO_x compound as well considering the high O level in the InSb.

Finally, structural analysis of the crystallized sample is shown in Figure 7, where an extended monocrystalline area was found (delineated by a dashed line) with the rest remaining nano crystalline. BF HR-(S)TEM revealed that this single crystalline area has the same epitaxial relationship as the Si (001) substrate,

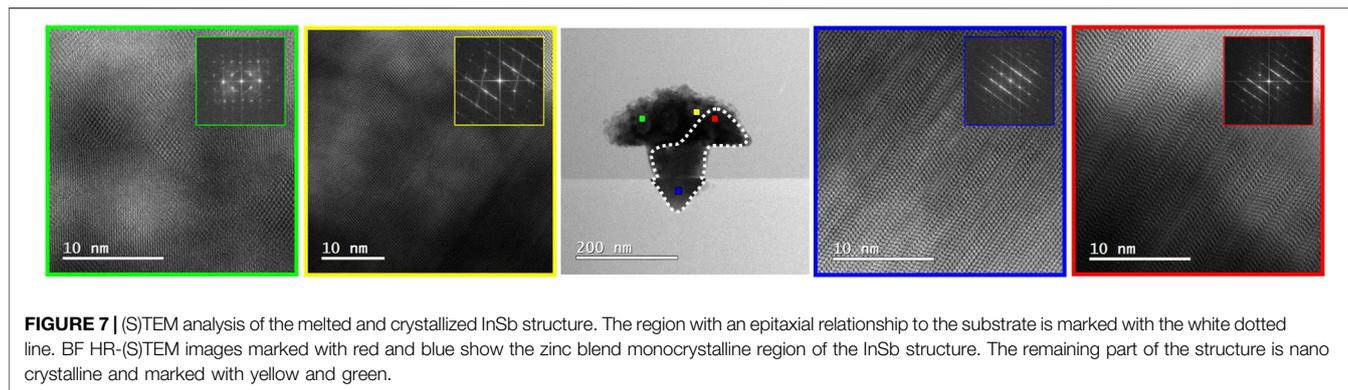


FIGURE 7 | (S)TEM analysis of the melted and crystallized InSb structure. The region with an epitaxial relationship to the substrate is marked with the white dotted line. BF HR-(S)TEM images marked with red and blue show the zinc blend monocrystalline region of the InSb structure. The remaining part of the structure is nano crystalline and marked with yellow and green.

confirming the anticipated process of initial crystallization of the melt from the Si interface. The single crystal has a high density of the stacking faults which run parallel to one of the four possible $\langle 111 \rangle$ planes of the substrate. This is the first demonstration that the proposed concept is indeed feasible, although on a limited scale only due to the limit dictated by the impurity concentration of the InSb melt. It is worth noting that using a higher melting point semiconductor such as InAs in place of the InSb crystal deposited by MOCVD in this work, melt-back etching of the Si and therefore unintentional Si doping of the InSb can be avoided.

CONCLUSION

We have proposed and demonstrated the use of electrodeposition as an alternative approach for monolithic integration of a compound semiconductor on silicon. Arbitrary shaped templates were efficiently filled with nanocrystalline InSb from an aqueous solution using pulsed electrodeposition. The melted and crystallized InSb within the templates were found to remain nanocrystalline, which was ascribed to a high impurity concentration in the InSb. Complexing additives to match the reduction potentials of indium and antimony ions closer together are proposed as a source of the impurities and heterogeneous nucleation during melt cooling. Despite the limitation encountered, InSb plating and epitaxial melt crystallization from a Si surface was demonstrated on a sub-micron scale, validating the proposed integration concept. To improve the current results towards large area epitaxial InSb films on Si, a synthesis path including brightener additives to form high purity deposits will be explored.

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DATA AVAILABILITY STATEMENT

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

AUTHOR CONTRIBUTIONS

KH-G and HS conceived and carried out the experiments. KH-G, SR, and HS contributed to sample preparation. MS performed (S)TEM analysis, MH performed XPS analysis. KH-G and HS processed the experimental data, performed the analysis, drafted the manuscript, and designed the figures. KM and HS supervised the work. All authors provided critical feedback and helped shape the research, analysis, and manuscript.

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Conflict of Interest: Authors KH-G, MS, MH, SR, KM, HS were employed by IBM Research.

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