Review Article

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A review of nanoimprint lithography for high-volume semiconductor device manufacturing

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Abstract: Imprint lithography has been shown to be a promising technique for the replication of nanoscale features. Jet and flash imprint lithography (J-FIL) [jet and flash imprint lithography and J-FIL are trademarks of Molecular Imprints, Inc.] involves the field-by-field deposition and exposure of a low-viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid, which then quickly flows into the relief patterns in the mask by capillary action. After this filling step, the resist is cross-linked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. There are many criteria that determine whether a particular technology is ready for wafer manufacturing. Included on the list are overlay, throughput, and defectivity. The most demanding devices now require an overlay of better than 4 nm, 3σ. Throughput for an imprint tool is generally targeted at 80 wafers/h. Defectivity and mask life play a significant role relative to meeting the cost of ownership (CoO) requirements in the production of semiconductor devices. The purpose of this paper is to report the status of throughput and defectivity work and to describe the progress made in addressing overlay for advanced devices. To address high-order corrections, a high-order distortion correction (HODC) system is introduced. The combination of applying magnification actuation to the mask and temperature correction to the wafer is described in detail. Examples are presented for the correction of K7, K11, and K17 distortions as well as distortions on actual device wafers.

Keywords: defectivity; jet and flash imprint lithography; nanoimprint lithography; overlay; throughput.

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1 Introduction

Nanoimprint lithography (NIL) is a high-throughput, high-resolution parallel patterning method in which the relief images in a template (mask or stamp) are replicated into a material by mechanical contact and material displacement [1–3]. This can be done by shaping a liquid followed by a curing process for hardening. The most common NIL process requires heat input to allow the imprint resist to flow into the relief images of a mask.

Devices that require several lithography steps and precise overlay will need an imprinting process capable of addressing registration issues. A derivative of NIL, ultraviolet NIL (UV-NIL), solves the issue of alignment using a transparent template, thereby facilitating conventional overlay techniques. In addition, the imprint process is performed at low pressures and at room temperature, which minimizes magnification and distortion errors. Two types of approaches are considered for UV-NIL. The first method uses conventional spin-on techniques to coat a wafer with an UV-curable resist [4]. Although it is possible to uniformly coat the wafer, there are concerns that the viscosity of the resist will be too high to facilitate the formation of very thin residual layers. If the residual layer is too thick, the critical dimension (CD) uniformity may suffer as a result of the subsequent pattern transfer process. In addition, a uniform coating of resist cannot account for variations in pattern densities on the template or mask, thereby leading to nonuniform residual layers. This problem is addressed by locally dispensing a low-viscosity resist material. This second approach was first disclosed by Willson et al. in 1999 and is generally referred to today as jet and flash imprint lithography (J-FIL) [5].[1]

J-FIL involves the field-by-field deposition and exposure of a low-viscosity resist deposited by Drop-on-Demand inkjet onto the substrate [6–14]. The patterned mask is lowered into the fluid, which then quickly flows into the relief patterns in the mask by capillary action.

1 Jet and flash imprint lithography and J-FIL are trademarks of Molecular Imprints, Inc.

After this filling step, the resist is cross-linked under UV radiation, and the mask is removed and leaves a patterned resist on the substrate.

Previous studies have demonstrated J-FIL resolution better than 10 nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there is no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single-level processing and zero waste, leads to a cost model that is very compelling for semiconductor memory applications.

There are many other criteria besides resolution that determine whether a particular technology is ready for manufacturing. With respect to the imprint stepper, both CD uniformity and line edge roughness meet the criteria of 2 nm. A collaboration partner has achieved and overlay of 10 nm (with a target of 8 nm) [13] and defect levels ~5/cm^2 across a lot of 25 wafers [14]. In 2015, mix-and-match overlay (MMO) results of less than 5 nm were achieved. Other criteria specific to any lithographic process include throughput, which plays a strong role in determining whether cost of ownership (CoO) requirements can be met. Recently, Takeishi and Sreenivasan reported that a throughput of 40 wafers/h (wph) was achieved on a four-station imprint tool [15]. Further improvements, defining a path toward 60 wph, were reported by Zhang et al. [16].

As the most aggressive features in advanced memory designs continue to shrink below 15 or 16 nm (toward 1Z nm), the cost of fabricating these devices increases because of the large number of additional deposition, etch, and lithographic steps necessary when using immersion lithography [17]. NIL offers a more attractive CoO than competing technologies. Cost benefits can be realized by

- Enabling direct printing of the features of interest without the need for multiple patterning techniques,
- Improving mask life that allows a replica mask to be used for more than 1000 wafers.
- By improving the throughput of the NIL tool, and
- By improving the overlay performance so that the technology can address both NAND Flash and DRAM devices.

Because cost is driven by the items listed above, careful attention is paid to particle generation, patterned defectivity, overlay, and throughput. These metrics are tracked to understand the readiness of the technology for the high-volume manufacturing of advanced semiconductor memory devices, such as NAND Flash and DRAM. A historical overview of these key metrics is shown in Figure 1.

In this review, we focus on the particles generated within the nanoimprint tool, tool throughput, and overlay.

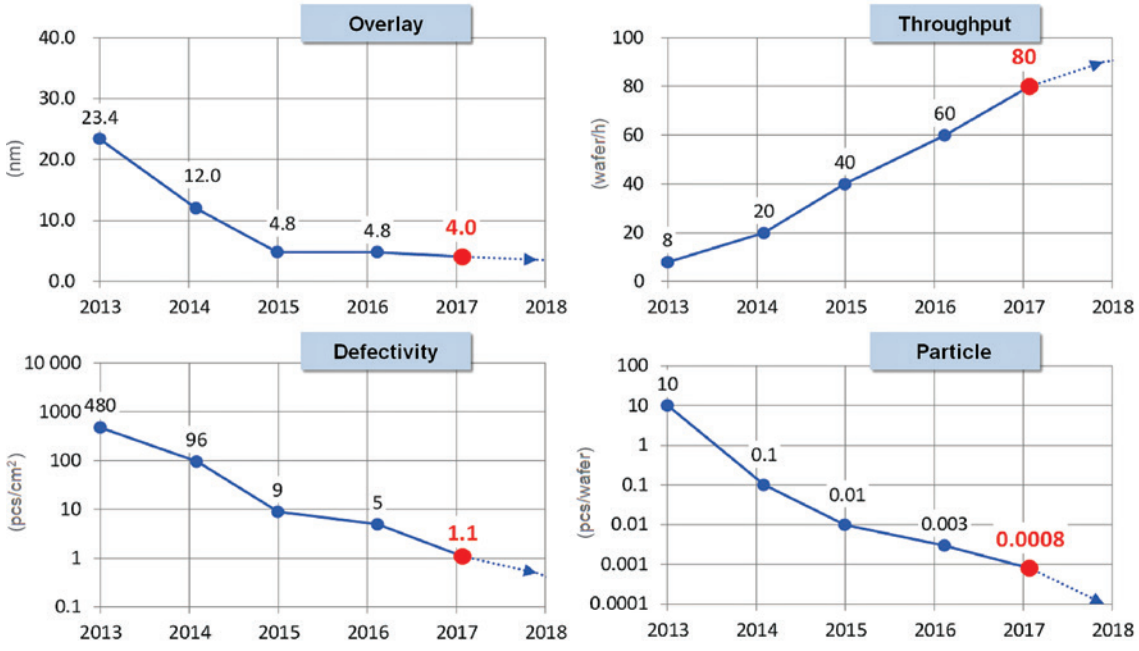


Figure 1: Historical overview of defectivity, particle generation, overlay, and throughput, starting in 2013.

2 Defectivity and particle generation

NIL, like any lithographic approach, requires that defect mechanisms be identified and eliminated to consistently yield a device. NIL has defect mechanisms unique to the technology, and they include liquid-phase defects, solid-phase defects, and particle-related defects. Examples of these types of defects have been discussed previously [15].

Especially, more troublesome are hard particles on either the mask or wafer surface. Hard particles run the chance of creating a permanent defect in the mask, which cannot be corrected through a mask cleaning process.

To put this point in perspective, consider that, to meet the CoO specifications required for memory devices, the replica mask life must be sustained for better than 1000 wafers. If we conservatively, assume that:

- Every hard particle adds a defect to the mask, and
- The mask defectivity limit from hard particles is 0.1 pieces/cm^2.

Then, the number of particle adders per wafer pass must be less than 0.001. As a result, if we are to achieve this particle specification, an aggressive strategy is needed to remove particle adders to the wafer and mask. The methodology for removing particles can be broken down into categories:

- Reduction: The minimization of particle generation from particle sources related to materials within the tool and the surface treatment of these materials.
- Removal: The reduction of particles that could potentially find their way onto the mask and wafer. These can be addressed by optimizing the airflow within the tool and by providing an ionizer source to address charge build up on the mask.
- Rejection: The elimination of particles through an inspection and mask cleaning process flow.
- Tool preparation: Meaning the measures taken to insure tool cleanliness.

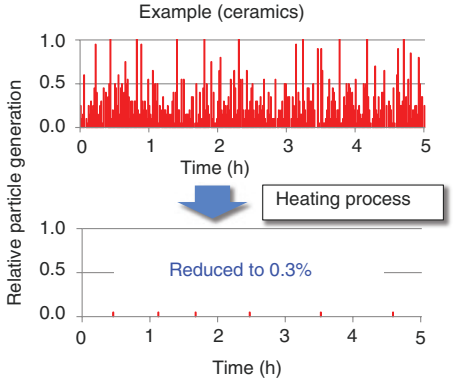
In the next sections, we review some of the previous approaches taken to mitigate particles in the imprint tool.

2.1 Ceramic treatment

In general, lithography tool manufacturers rely on the use of ceramic materials to reduce particle generation. What is not generally appreciated, however, is that even ceramic materials continuously generate particles. As a result, several surface treatment methods have been developed to minimize particle generation. The top left graph in Figure 2 shows an example of a ceramic that generates many particles over the course of several hours. By applying correct polishing, coating, and heating methods, however, particle generation is significantly reduced. As an example, the graph on the bottom left shows particle generation after a special heating process. In this case, the relative particle generation is reduced to only 0.3% after the heat treatment [18]. This type of strategy is applied for all relevant materials within the tool.

2.2 Application of a primary air curtain

A key point to be made is that, even when particles are shed, they do not find their way to the mask and wafer surfaces. This is accomplished by applying airflow optimization methods to the tool, in particular, to the area of the mask and wafer. Figure 3 depicts a simulation of particles



Experimental data for ceramics

Treatment method	Particle generation rate (after treatment)
Polishing	1.4%
Coating	0.4%
Heating	0.3%

Figure 2: Surface treatment methods for ceramic-based materials. Special heat treatment methods can be effective in reducing particle generation from these surfaces to 0.3%.

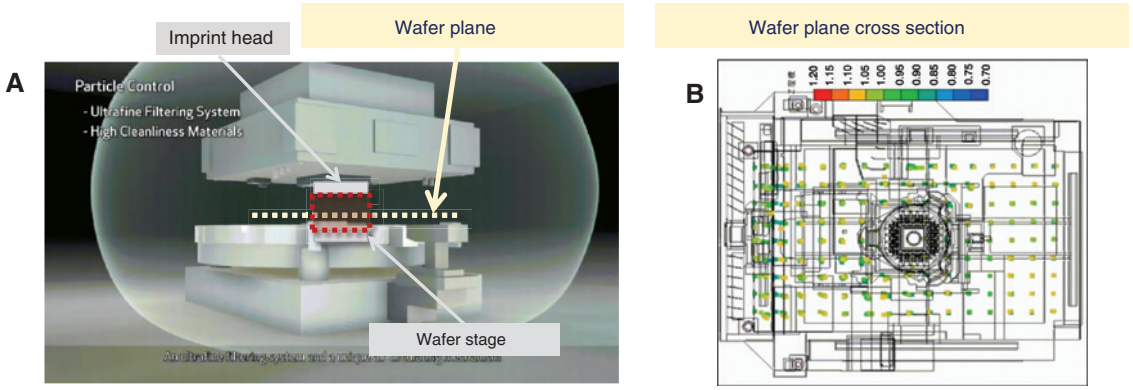


Figure 3: (A) Schematic of the imprint tool and (B) a simulation of particles tracked within the imprint tool.

tracked in the wafer plane. Figure 3A shows a schematic of the tool. Incoming particles can initially be managed through the choice of material and material treatment as well as ultrafine filtration systems. However, these steps alone are not sufficient to meet defectivity goals, and additional countermeasures must be adopted to further reduce particles near the wafer. Figure 3B shows a simulation of particles tracked within the tool. Note that particles located above the wafer are substantially reduced relative to the rest of the tool. How this is accomplished is discussed below.

An environmental test stand was developed specifically to study particle control. This test stand is capable of adjusting the starting environment within the tool. An example of how the system operates is shown in Figure 4. Particle counts were performed at two unique particle settings. The graph below shows the difference between an ISO Class 7 environment, where almost 10^7 particles are generated within a cubic meter, and an ISO Class 0 environment.

To address particles at the wafer plane, a primary air curtain system was introduced into the test stand, as shown in the schematic image in Figure 4B. This air curtain has already been applied to our NIL tools. To predict the effects of an optimized airflow system, an accelerated experiment was performed by setting the test stand for ISO Class 7 conditions.

The accelerated test was done by

- Moving the stage equivalent to a full wafer run and
- Operating the air curtain system in an ISO Class 7 environment and
- Measuring wafer particle counts and
- Then extrapolating the equivalent ISO Class 2 values that are applied to the NIL tool.

The smallest particles measured had a diameter of 80 nm and were measured using a KLA-Tencor Surfscan SP3.

In this experiment, we operated the test stand under three different conditions:

1. Without any air curtain,
2. With the primary curtain, and
3. With an extended primary air curtain.

As shown in Figure 5, without any curtain, almost 3000 particles are generated on the wafer, with an equivalent ISO Class 2 count of 0.03 pieces/wafer pass. By applying the air curtain, we can reduce this number to 0.006 pieces and under optimal conditions further reduce the particle

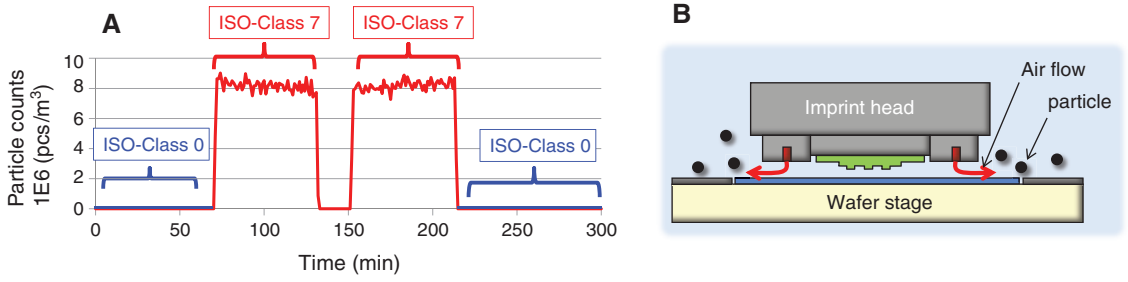


Figure 4: (A) Environmental test stand operating at two different conditions (ISO Class 7 and ISO Class 0) and (B) primary air curtain designed to reduce particulates at the plane of the mask and wafer.

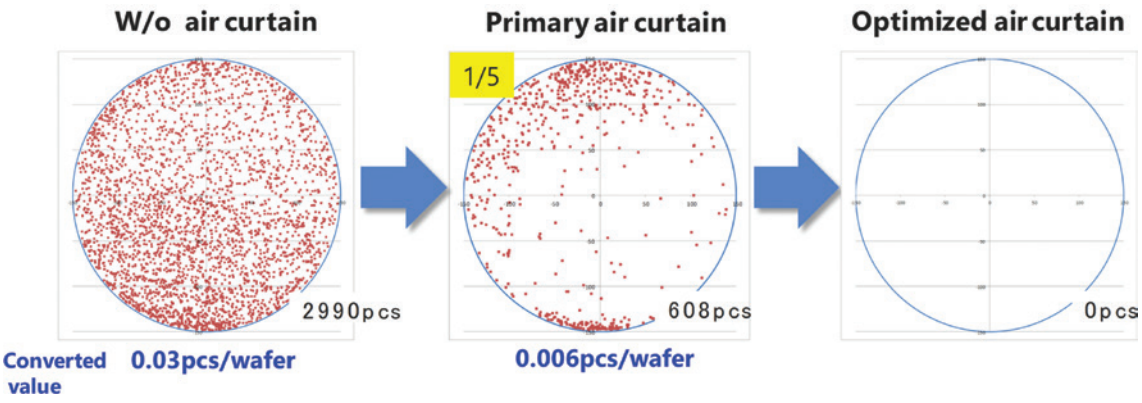


Figure 5: Accelerated particle counts in a test stand with no air curtain, a primary air curtain, and an extended primary air curtain. The extended wafer coverage of the extended curtain was very effective in reducing the number of particles on the surface of a 300 mm wafer.

adders to less than 0.003 [19]. Clearly, the air curtain operation was confirmed to have great potential for meeting the particle adder specification.

The primary air curtain has now been implemented in the nanoimprint tool, and additional polishing and cleaning methods were applied to drive particle reduction down to 0.0008 pieces/wafer or 1 particle every 1250 wafers (as shown in the bottom right graph of Figure 1).

Although successful in reducing particulates, the previous version of the primary air curtain was restricted in its coverage within the imprint tool as shown in Figure 6A. The primary air curtain captured the entire area of the mask chuck but did not include the wafer pick up area. Additionally, when the wafer stage moved beyond the borders of the primary air curtain, the particle environment was not as well controlled.

A redesign and configuration of the air curtain created a more optimized curtain that covered both the mask chuck and the wafer as the stage is moved, as shown in Figure 6B. The result of this optimized design is shown in the rightmost image in Figure 5, which pictures particles captured on a wafer during accelerated testing. In this experiment, no particles were detected when the optimized air curtain equipped with extended coverage was applied. Plans are in place to start on-tool testing and results will be reported in the future.

2.3 Other particle mitigation methods

Polishing methods can also be applied to parts other than ceramics within the tool. As an example, gas nozzles within the system often have rough surfaces that allow particles to shed during the operation of the nozzle. Mechanical and chemical polishing can reduce the roughness and have been shown to reduce particulation by more than two orders of magnitude [20].

Electrostatic charging can also lead to particle formation on the surface of a mask. Electrostatic charge can be generated on the surface of the imprint mask as a result of the separation of the mask and wafer after the exposure of the imprint resist. Charge can be addressed in two ways. One method is to attempt to remove the charge using various neutralization schemes. The second method is to create a charged environment away from the mask to preferentially attract charged particles to the charged environment. The basic concept is shown in Figure 7. An electrostatic cleaning plate (ESCP) is placed

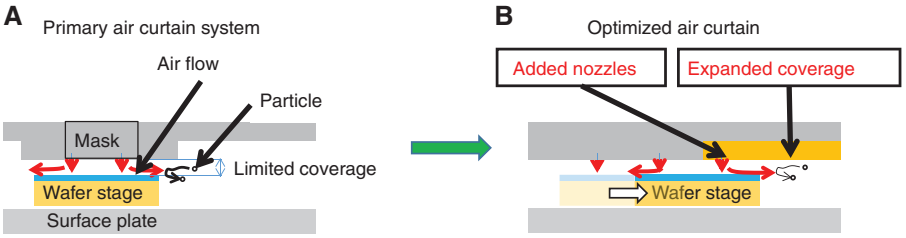


Figure 6: (A) Primary air curtain and (B) optimized air curtain providing extended coverage as the stage is moved.

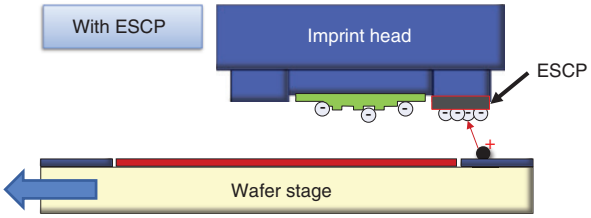


Figure 7: Schematic drawing of an ESCP designed to draw charge particles away from the mask surface.

adjacent to the mask and operated at a voltage greater than the voltage generated on the imprint mask. Initial on-tool results are very promising and will reported in the future [20].

3 Throughput

Throughput for a nanoimprint system is gated by the time it takes to fill the relief images of an imprint mask. There are several parameters that can impact resist filling. Key parameters include

- Resist drop volume (smaller is better),
- Material engineering (to promote wetting between the resist and the underlying adhesion layer),
- Design for imprint or DFI (to accelerate drop spreading and address different pattern types),
- System controls that address drop spreading after jetting for both full fields and partial fields, and
- Drop pattern optimization.

In addition, it is mandatory to maintain fast filling even for edge field imprinting. Previously, we have demonstrated that it is feasible to fill dense line/space patterns in only 1 s.

The resist properties have a large impact on fill time and the engineering of the resist is critical for meeting performance criteria and properties such as surface tension, viscosity, and wetting. Surface wetting has a strong influence on fill time and has been addressed with newer resist formulations that cause resist spreading to increase by a factor of 3 before the mask makes contact to the resist material on the wafer surface [16].

As a rule of thumb, a 1.1 s fill time is necessary to achieve a throughput of 20 wph/imprint station or 80 wph for a fully configured four-station NZ2C cluster tool. In 2016, throughputs of 15 wph with a 1.5 s fill time were achieved. More recently, 17 wph with a fill time of 1.2 s has been demonstrated on the tool and 1.1 s filling on device-like layouts with a test platform. The details are discussed below.

3.1 1.2 s fill time/68 wph

Device levels often consist of unique regions, each having its own particular set of features. As an example, a memory level may have dense feature regions, peripheral circuitry regions, and kerf regions that may include larger features such as align and metrology marks. Figure 8 shows the breakdown for the test mask used for this study.

Each region of the layer has its own specific filling characteristics. The second column describes the filling times achieved for the 1.2 s/60 wph process demonstrated at the end of 2015. For this work (final column), fill times of 1.0 s were targeted in all regions, with the exception of the kerf regions containing various metrology marks.

It is interesting to note that the longest fill times are often located in the kerf regions, as resist typically fills from the center of a field out toward the edge. In addition, larger features, such as metrology marks located in the kerf, are the most difficult to fill. For the other regions, it was sufficient to achieve the faster filling times by applying new resist systems designed to promote faster resist spreading and to fine-tune system controls.

Filling area	Fill time (end of 2015)	Fill time targets (mid 2016)
FF: Core area 30 nm L/S	1.2 s	≤1.0 s
FF: Peripheral circuitry	1.5 s	≤1.0 s
PF: Core area 30 nm L/S	1.5 s	≤1.0 s
FF & PF: Marks in kerf	1.5 s	≤1.2 s
Tput (wph)	**60***	**68***

FF: Full field
PF: Partial field

Inspection is based on KT2800 and KT2905
- Random mode inspection for full imprint field
- Array mode inspection for L/S.

* Based on a 4-station NZ2C imprint tool.

Figure 8: Test mask layout and targeted fill times for both 60 and 68 wph processes.

For the kerf area, however, some marks needed to be redesigned (without impacting their functionality). This redesign represents one implementation of DFI. Quite often, this meant segmenting the larger features as shown in Figure 9 below.

After performing the necessary optimization, a 25-wafer run was done at a filling time of 1.2 s on the FPA1200-NZ2C using a test mask with a minimum half-pitch of 30 nm. The results of this run are shown in Figure 10.

The test mask started with a baseline defectivity of ~3 defects/cm^2. After the completion of the run, the defectivity increased by 1.5 defects/cm^2. This increase was anticipated, as wafers were prepared in one site and then shipped overseas for imprint testing. This was confirmed by inspecting all fields and performing a defect analysis. This analysis is shown in Figure 11. In the analysis, 61% of all defects were traceable to the previous layer on the wafer. Most importantly, however, was the confirmation of the fill time process. Only 0.8% of the defects were nonfill defects that can be attributed to resist filling issues.

3.2 1.1 s fill time/80 wph

To achieve an 80 wph throughput, both fill time and overhead needed to be reduced. The targeted fill time for this work was 1.1 s. Again, the greatest challenges were in the kerf regions and were addressed with the following methods [13]:

- Resist drop volume: sub-1.0 pL
- Smaller drops means decreased distances between drops.
- Drop pattern optimization based on imprint feature type:
- Dense lines, contact holes, peripheral circuitry, and metrology marks.
- System hardware and controls
- To address mask/wafer initial contact after jetting and drop spreading after contact.

Fill time was tested by patterning both full fields and partial fields and the results are shown in Figure 12A and B, respectively. Figure 12A describes full-field nonfill defect density as a function of fill time. The nonfill defectivity

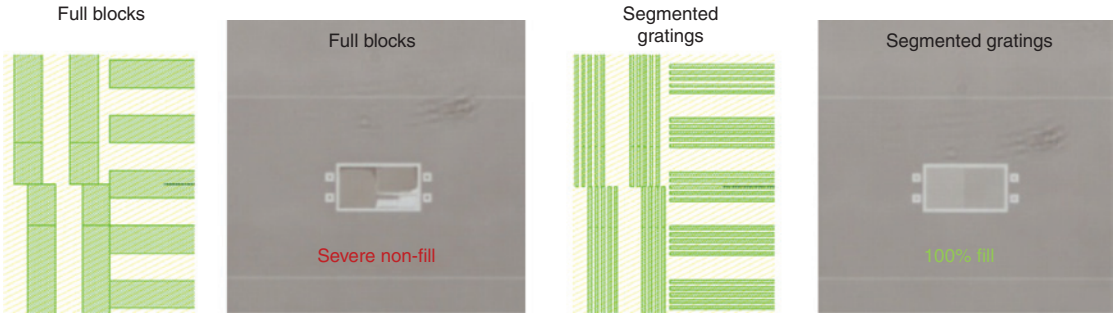


Figure 9: Example of DFI in which large features are broken into segments to promote faster resist filling.

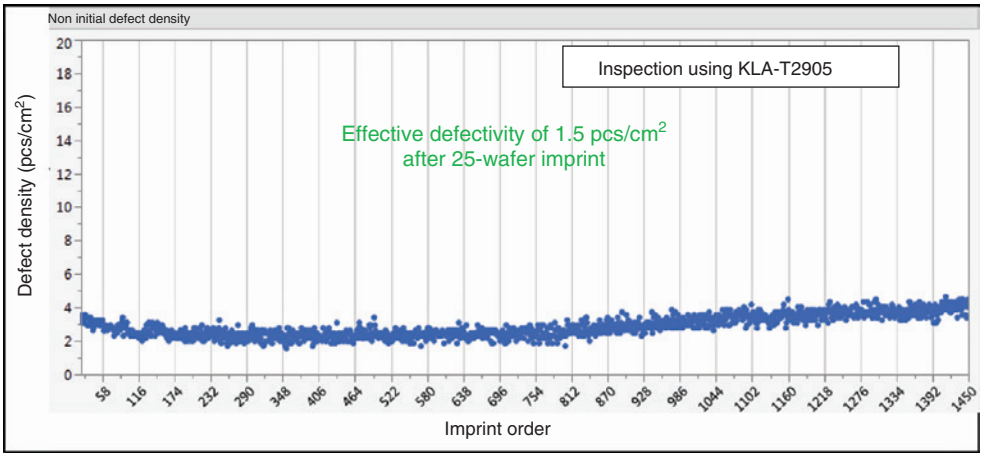


Figure 10: Defect density across a 25 wafer run. Overall defectivity increased by 1.5 defects/cm^2.

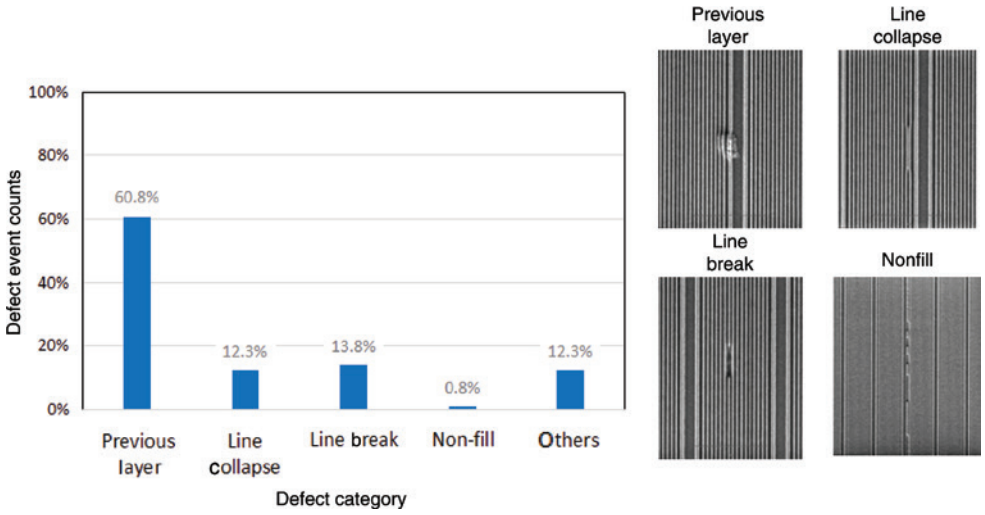


Figure 11: Defect breakdown across a 25 wafer run. Only 0.8% of the defects were fill time related.

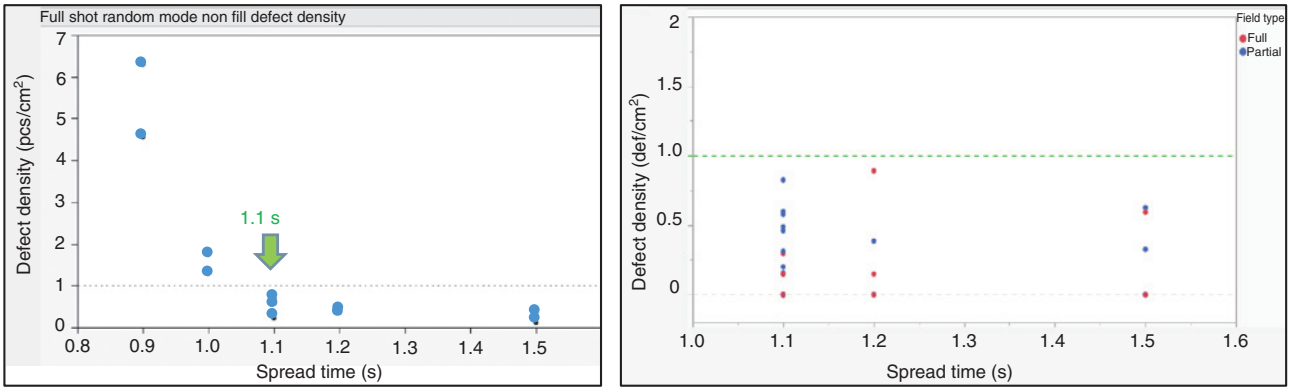


Figure 12: (A) Full-field nonfill defect density as a function of fill time (the nonfill defectivity remains constant until the fill time decreases to 1.0 s) and (B) full- and partial-field nonfill defectivity showing similar behavior.

remains constant until the fill time decreases to 1.0 s. In Figure 12B, nonfill defectivity is tracked for both full fields and partial fields. It is important to note that several partial field locations require testing as the system controls need to be adjusted depending on the size of the partial field area. It should also be mentioned that the nonfill defectivity observed in this study was mainly confined to larger features in the kerf areas that have not yet been segmented into smaller features, as described in Figure 9. Future studies will apply the needed DFI, and the new control processes will be ported to the NZ2C four-station tool.

4 Overlay

The alignment and overlay system consists of various factors, which can be categorized generally as alignment and distortion. In a multistation system, such as the NZ2C, it is important to recognize that overlay and distortion must be controlled within a station and from station to station. Additionally, the magnification actuator system initially employed for overlay is limited in its ability to correct for high-order distortion signatures present on previously pattern levels of a device. Thus a method for correcting these distortions is required. In the following sections, we address all three subjects.

4.1 Through the mask (TTM) alignment system

Using a TTM Moiré-based alignment system [21], 1 nm repeatability has been demonstrated and the data collected by the TTM system correlate very closely with an

Archer measurement tool. Canon has studied both single-machine overlay (SMO) and MMO, and the results are reported below.

SMO measurements are not done in the same way as an optical projection system, as it is not possible to print a second time over the existing resist. As a result, the wafer must be removed after a first imprint, etched, and placed back in the tool for the subsequent imprinting. Shown in Figure 13 are the SMO results across a full wafer and within a single field. Within a single field, an SMO of less than 1.2 nm, 3σ was observed. Across wafer, the SMO was less than 2.2 nm.

The best MMO data are presented in Figure 14. Across the wafer, 4.0 nm, 3σ was observed.

In a follow-up experiment, system stability was examined over a 3-day period. The average +3σ MMO achieved

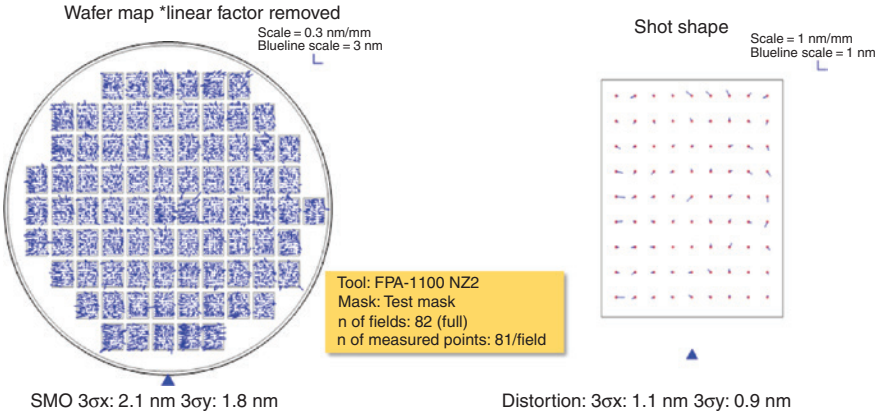
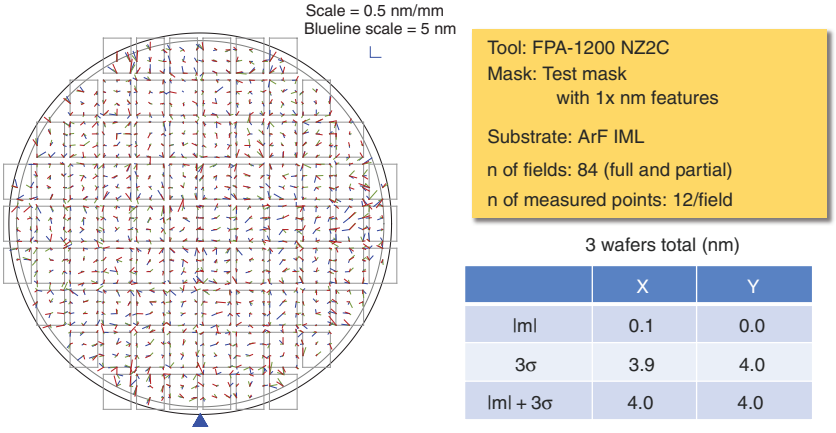


Figure 13: SMO measurements using the NZ2C imprint system. Within a single field, an SMO of less than 1.2 nm was observed. Across wafer, SMO was less than 2.2 nm.



3 wafers total (nm)

	X	Y
|m|	0.1	0.0
3σ	3.9	4.0
|m| + 3σ	4.0	4.0

Figure 14: MMO to an ArF immersion scanner. The three-wafer average and 3σ values in x and y were 4.0 and 4.0 nm, respectively.

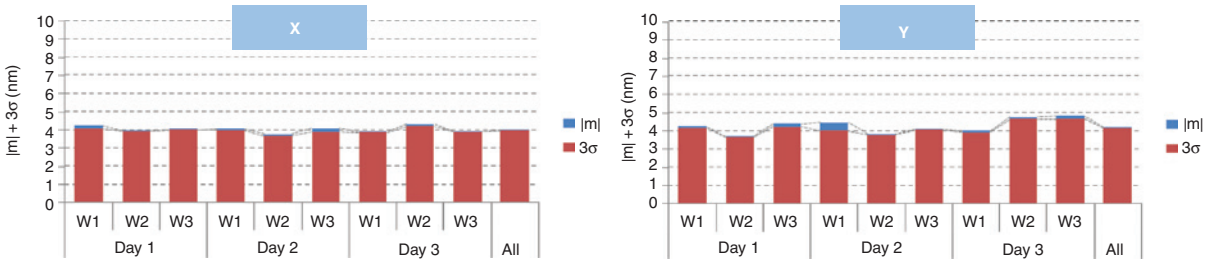


Figure 15: MMO stability over a 3-day period. The mean + 3σ values in x and y were 4.0 and 4.2 nm, respectively.

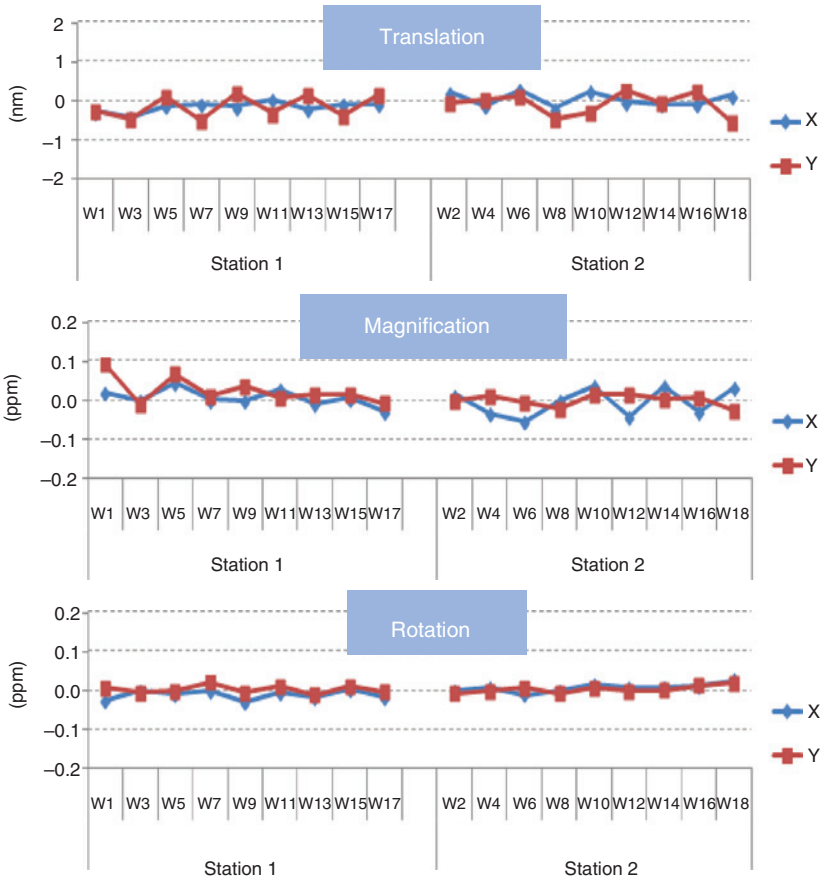


Figure 16: Translation, magnification, and rotation variability between two imprint stations in the NZ2C.

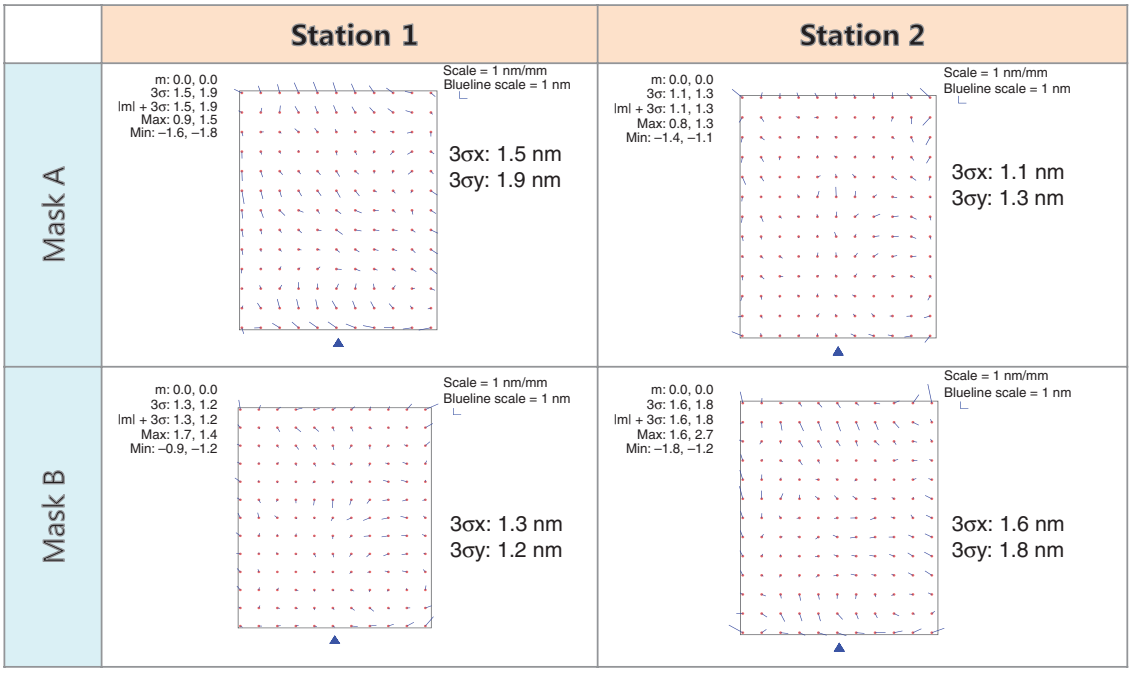


Figure 17: Residual distortion errors between two imprint stations using two different masks.

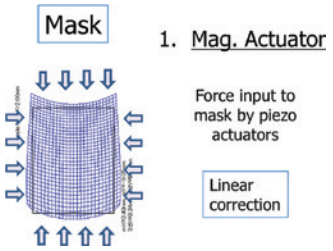


Figure 18: Correction using an array of piezo actuators.

over the 3-day period was 4.0 nm in x and 4.2 nm in y, as shown in Figure 15.

4.2 Station-to-station stability

Initial tests have also been performed to understand the variability between stations in the NZ2C cluster tool. The first experiment examined variability between two stations across an 18-wafer run. Measured were the translation, magnification, and rotation residuals. As shown in Figure 16, the translation variability is well under 1 nm and the magnification and rotation residuals were less than 0.10 ppm.

Figure 17 reports the average distortion residuals between two stations using two different masks. Data were collected across 58 fields of a wafer and the residual value was calculated by subtracting out the average distortion. The difference between stations and masks is less than 0.70 nm.

4.3 High-order distortion correction (HODC)

It is important to note the difference in overlay approaches between an optical scanner and an imprint step and repeat tool. In an optical scanner, shot shape high-order compensation (SSHOC) is done by manipulating both the stage and lens during the exposure process. A different approach is required for the imprint tool to do HODC. HODC for NIL can be enabled by combining two approaches:

- Magnification actuator, which applies force using an array of piezo actuators, and
- Heat input to correct distortion on a field by field basis

Both approaches are described below.

With respect to the magnification actuator, a larger array of piezo-based actuators can be applied to do linear corrections. A simple schematic is shown in Figure 18.

Heat input on a field-by-field basis is also possible using a digital multimirror device (DMD) and defines a potential path for achieving overlay results of better than 3 nm. An example of this method is depicted in Figure 19. Figure 19A describes the heat input, temperature, and initial shot distortion at time $T=0$. Figure 19B shows the final heat input, temperature, and distortion after 500 ms,

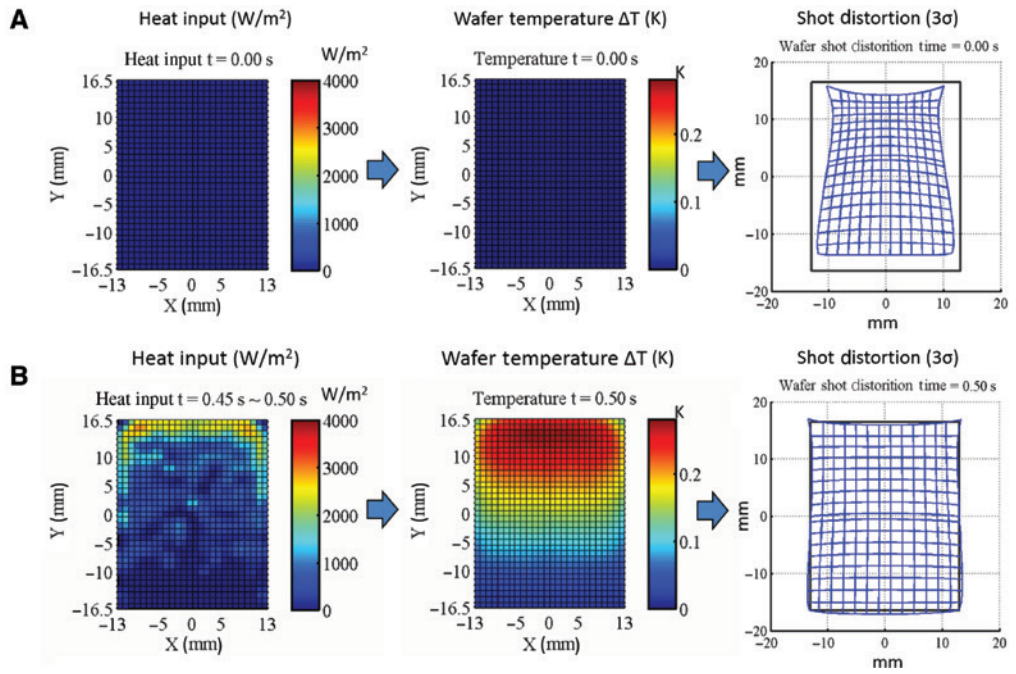


Figure 19: (A) Shot distortion at time $T=0$ and (B) distortion after a heat input of 500 ms.

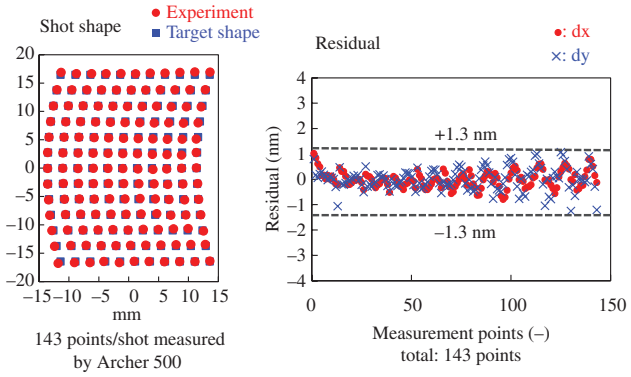


Figure 20: (A) Targeted and experimental results for a K11 high-order correction and (B) residual errors were less than 3 nm.

which is well within the resist fill time budget of 1100 ms to achieve throughputs of 20 wph/imprint station.

Initial heat input experiments have now been performed and the results are very promising. Simulation and experimental results are in excellent agreement, and a reproducibility across a four-wafer set of ~1 nm was demonstrated. Testing has now started on the NZ2C tool, first looking at the ability to correct known high-order terms such as K7 (second magnification), K11 (bow), and K17 (pincushion).

Figure 20 describes the results of the experiment designed to address bow within a field. In the experiment, bow was targeted at 0.02 ppm/mm. To obtain the data, a first reference wafer was patterned by imprinting 58 full-field shots with a –2 ppm magnification offset. A second wafer was then patterned by imprinting 58 full-field shots with the same magnification offset and the heat input required to generate the desired bow. Average placement across each wafer was then calculated and the two field maps were subtracted. The results in Figure 20A show the difference between the targeted shape (in blue) and the shape obtained experimentally (in red). The residuals are shown in Figure 20B for each of 143 measurement points. Very good agreement was observed, with maximum residual errors of less than 1.3 nm.

Similar experiments were also done to look at K7 and K17 high-order corrections, as shown in Figure 21. Again, the targeted and experimental values are in good agreement.

HODC was next applied to a device wafer that required a bow correction. The results are reported in Figure 22. Again, excellent correction was confirmed, with residual errors less than 1.3 nm as measured using an Archer 500 tool. Other high-order terms can be corrected as well, but the thrust going forward will be targeted at device wafers.

5 Conclusions

Great progress has been made in the field of NIL over the last 4 years. In this paper, to meet CoO requirements and to address yield issues, the progress on particle reduction, throughput, and overlay was reported. The continued reduction of particle adders extends both the life of the master mask and the replica mask. In this work, an air curtain system was tested both on a test stand and on the imprint tool. In an optimized configuration in a test stand, the air curtain showed potential for enabling a particle adder count greater than 1000 wafers. Optimization

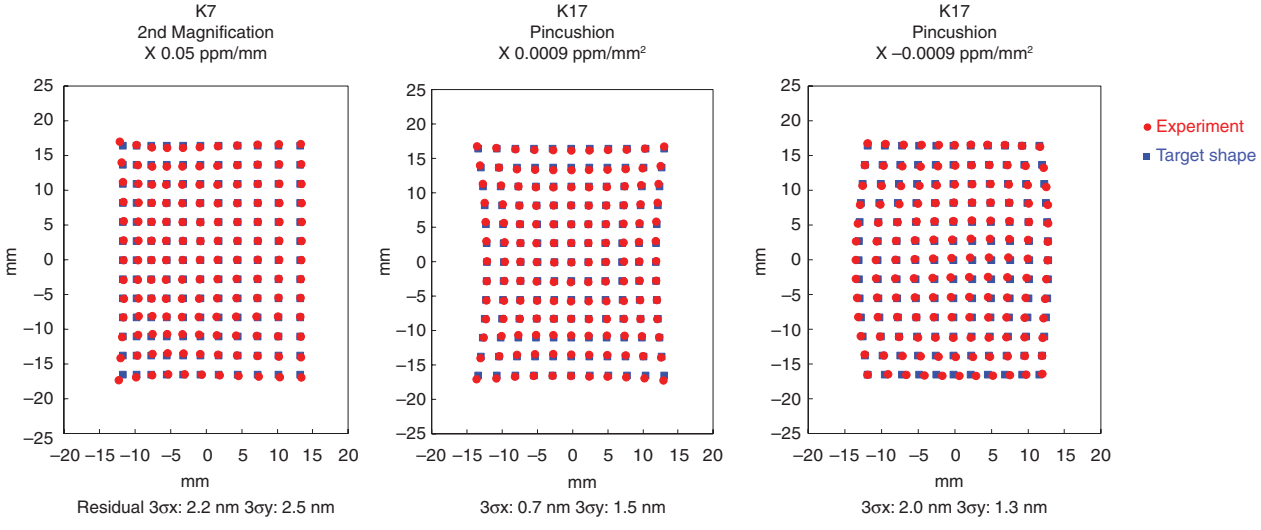


Figure 21: Good HODC obtained for K7 (second magnification) and K17 (positive and negative pincushion).

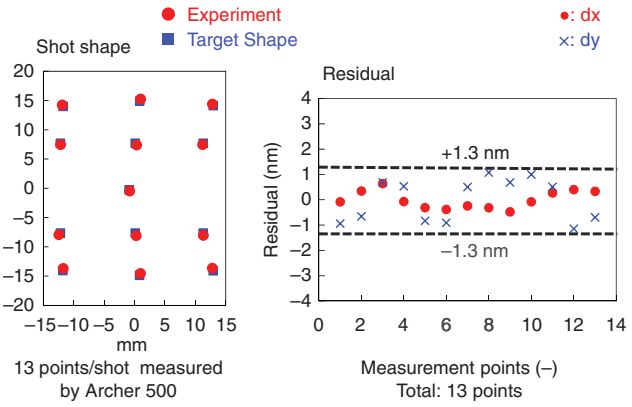


Figure 22: Corrected bow on a device wafer using the HODC system. Residual errors were again less than 1.3 nm.

of this new scheme as well as enhancements to the existing particle control systems will aid in the further reduction of imprint defectivity to meet the levels required for device manufacturing. Recently, a mask lifetime of 13 boxes or 325 wafers was reported at a defectivity of 1.1 defects/cm^2 [22].

Throughputs of up to 20 wph/imprint station have also been achieved. This translates to 80 wph for a four-station cluster tool and is considered sufficient for high-volume manufacturing.

Finally, an MMO of 4.0 nm has been demonstrated and methods for reducing overlay error using heat input through a HODC system were introduced. The HODC system has successfully corrected bow, pincushion, and second magnification distortions and was also successful in doing corrections on device wafers. An overlay of 4.0 nm is already considered sufficient for the manufacturing of NAND Flash devices. For DRAM, however, tighter overlay controls are typically required (usually on the order of 15%–20% of the half-pitch for the most critical levels), and it is anticipated that the HODC system implementation will be needed to meet the more stringent targets.

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