Views

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ITRS lithography roadmap: 2015 challenges

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Abstract: In the past few years, novel methods of patterning have made considerable progress. In 2011, extreme ultraviolet (EUV) lithography was the front runner to succeed optical lithography. However, although EUV tools for pilot production capability have been installed, its high volume manufacturing (HVM) readiness continues to be gated by productivity and availability improvements taking longer than expected. In the same time frame, alternative and/or complementary technologies to EUV have made progress. Directed self-assembly (DSA) has demonstrated improved defectivity and progress in integration with design and pattern process flows. Nanoimprint improved performance considerably and is pilot production capable for memory products. Maskless lithography has made progress in tool development and could have an α tool ready in the late 2015 or early 2016. But they all have to compete with multiple patterning. Quadruple patterning is already demonstrated and can pattern lines and spaces down to close to 10-nm half pitch. The other techniques have to do something better than quadruple patterning does to be chosen for implementation. DSA and NIL promise a lower cost. EUV promises a simpler and shorter process and the creation of 2-D patterns more easily with much reduced complexity compared to multiple patterning. Maskless lithography promises to make chip personalization easy and to be particularly cost effective for low-volume chip designs. Decision dates for all of the technologies are this year or next year.

Keywords: directed self assembly (DSA); EUV lithography; ITRS roadmap; lithography; maskless lithography; multiple patterning; nanoimprint; semiconductor patterning.

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1 Introduction

In 2012, we published a letter describing the current lithography challenges as outlined by the International Technology Roadmap for Semiconductors (ITRS) roadmap [1]. At the time, the 2011 roadmap was the latest published full roadmap. It showed a key decision point coming up at the end of 2012: What patterning choice would be used for the 22-nm logic node and for 22-nm half pitch DRAM production? The choices were ArF immersion lithography with double patterning, and four next-generation lithography (NGL) techniques, extreme ultraviolet (EUV) lithography, directed self-assembly (DSA), imprint lithography, and maskless lithography (E-beam direct write). Every NGL technique had its own challenges, but EUV lithography appeared to be the nearest to commercialization.

Now, we know that the 22-nm node was manufactured with ArF lithography and double patterning [2, shows 60 nm pitch fin geometries for 22 nm logic node chips]. Multiple patterning is also being used to produce the 14-nm logic node, which started production in 2014[1] and is expected to be used for the 10-nm logic node, too,[2] which will involve quadruple patterning for at least the fin layer A 10 nm node chip with a 24 nm metal half pitch is described in [3]. Extrapolation of fin geometries suggests they are sub 20 nm half pitch and require quadruple patterning. So where does this leave the next-generation lithography options listed above, and what are the current patterning challenges facing the semiconductor industry?

As shown in Figure 1 below that was published in the 2013 ITRS roadmap (see figure 3A from the 2013 ITRS lithography roadmap at http://www.itrs.net) multiple patterning and all of the NGL techniques have enough resolution to do 10-nm half pitch or better. Better

1 See page 43 of http://www.intel.com/content/dam/www/public/us/en/documents/pdf/foundry/mark-bohr-2014-idf-presentation.pdf, for start dates of 14 nm node logic production.

2 See, e.g. the report in EETimes, http://www.eetimes.com/document.asp?doc_id=1324165 for the 14 nm node and http://www.eetimes.com/document.asp?doc_id=1326670 for the 10 nm node.

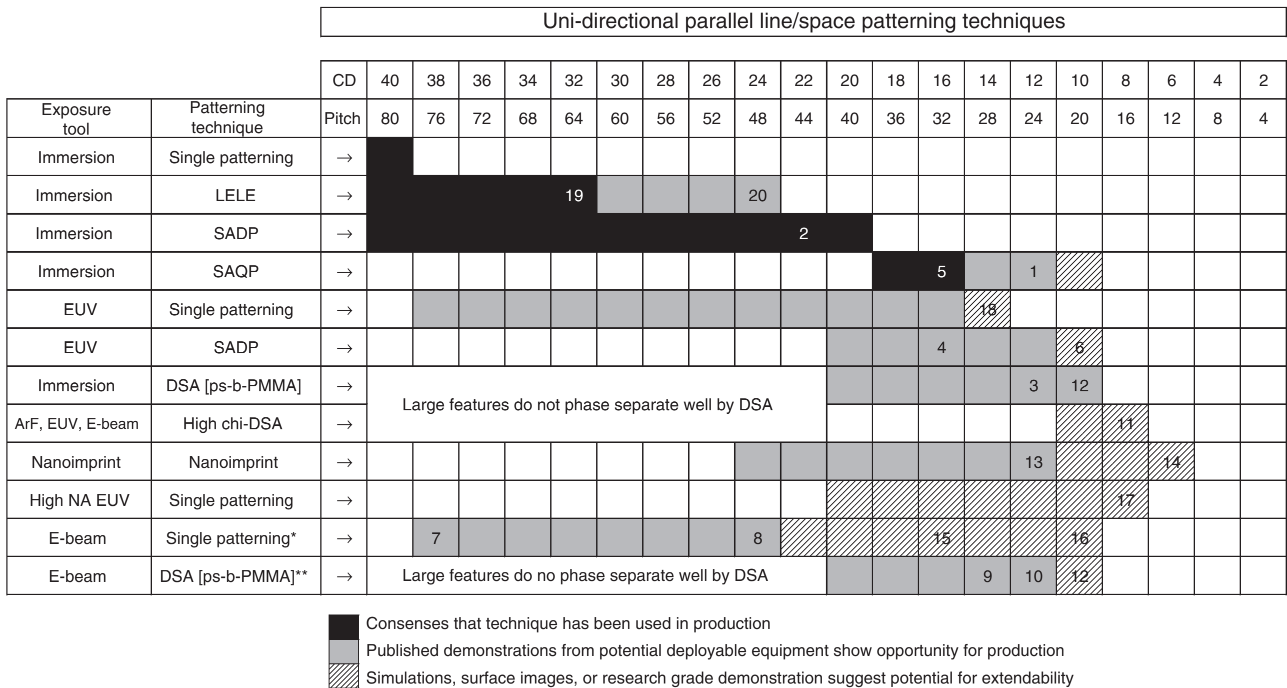

Figure 1: Line and space potential solutions by pitch and half pitch. Numbers indicate literature references available in the full roadmap published at www.itrs.net.

resolution than this will not be needed in manufacturing until at least 2020. The 2013 ITRS roadmap shows this minimum half pitch first being reached in 2022 or 2023 by fins in logic finFETs. However, the industry typically exceeds the roadmap. Assuming a 2 year cycle extending from recent product announcements and descriptions, 2020 seems a possible year to be doing this half pitch in logic device production. Given that quadruple patterning is already a demonstrated technique, any NGL has to demonstrate some advantage over quadruple patterning in order to be adopted in manufacturing before 2021. Once sub-10-nm half pitch dimensions are needed in manufacturing, these same NGLs will then be competing with extensions of multiple patterning such as octuple patterning. In the sections below, we discuss the progress of each of the NGL techniques since 2011, along with their status, challenges, and possible driving forces for implementation.

2 Extreme ultraviolet lithography (EUVL)

A key issue in 2011 was the exposure tool light sources, which were not powerful enough to even be used for pilot development. There has been a lot of progress in the past several years [4]. It is fair to say that EUV scanners now have sufficient productivity to be used for pilot line development of chip making processes. Companies have now started to order enough tools for pilot production. Two multiple EUV scanner orders have been reported recently, and at least one of these orders is clearly destined for logic pilot production.[3]

The most likely first manufacturing node possible for EUV use is the 7-nm logic node, given that processes for the 10-nm node seem already to be fixed with manufacturing production planned for 2016 [2, see 10 nm node references]. However, throughput and uptime suitable for manufacturing use still has not been demonstrated. In 2014, it was reported that a wafer throughput of 75 wafers per hour would be needed to provide a cost benefit over multiple patterning with ArF immersion for 7-nm logic node metal levels [5]. ASML roadmaps show that approximately 125 W EUV power at the intermediate focus together with a resist sensitivity of 20 mJ/cm^2 will be needed to reach this throughput. This compares with the 2015 report of 80 W and 51% uptime [4]. Resist photospeed

3 See EETimes report of December 8, 2014, http://www.eetimes.com/document.asp?doc_id=1324906, that TSMC will buy two TSMC report and ASML's press release of April 22, 2015 that a US customer had ordered fifteen EUV scanners purchase order http://www.asml.com/asml/show.do?lang=JA&ctx=5869&rid=51765.

was not specified in this report, but other work suggests that typical resist photospeeds for high-performing EUV resists are currently around 40 mJ/cm^2 or higher and still do not meet targets for line width and line edge roughness (LWR and LER) [6]. Given that source power still has to be almost doubled to reach 125 W and resist photospeed is roughly twice the scanner manufacturer's target, throughput still has to improve by a factor of 3–4 in order to make EUV cost effective for the 7-nm logic node.

Next to EUV source power, enabling defect-free EUV masks and keeping them defect free has been the most critical challenge for EUV over the past decade. A major industry milestone was achieved in 2014 when SEMATECH announced it had achieved EUV mask blanks with zero killer defects larger than 50 nm in size [7]. This was the culmination of a 10-year industry development program to enable defect-free mask blanks. The expectation is that further developments to keep pace with the more stringent defect requirements of smaller technology nodes will be led by the mask blank suppliers. In addition to mask blank defect reduction, improved mask cleans and repair technologies as well as defect mitigation schemes using smart pattern placement to make defects nonprintable have brought the defect-free mask goal within reach. However, the industry has come to the consensus that eventually an EUV pellicle will be needed [4]. Over the past 2 years, pellicle membranes with EUV transmission >80% have been developed [8], and the 90% transmission may ultimately be achieved reducing the pellicle-induced light loss to 20%. However, commercializing EUV pellicle technology will likely take a few years so that EUV will have to be introduced into manufacturing as a pellicle-less technology.

In addition to mask materials, the critical mask tool infrastructure has been enabled over the past years with both an EUV AIMS review tool and an actinic mask blank defect inspection tool becoming commercially available through development programs led by SEMATECH/Carl Zeiss (EUV AIMS) [9] and EIDEC/Lasertec (AIT) [10], respectively. However, it is not yet clear when an actinic patterned inspection tool will become available. Overall, the EUV mask infrastructure is expected to be ready to fully support EUV at the 7 nm. For earlier use of the EUV bridge, tools may have to be used, e.g. patterned defect inspection.

The 7-nm logic node patterning technology will probably have to be selected sometime in 2016 for production in 2018. (This assumes the 10 nm node meets its planned manufacturing date of 2016, and a two year cycle for the 7 nm node.) Improvement of scanner throughput, mask defects and scanner uptime are preconditions for successful EUV use in manufacturing. EUV offers substantial benefits in process simplicity compared to multiple patterning by reducing mask counts and allowing more two-dimensional designs to be printed [11]. These benefits will be the driving force for change from multiple patterning.

3 Nanoimprint (NIL)

NIL is a technology of creating a patterned template like a stamp that is pressed onto a thin film of liquid on a wafer. The template is transparent, and a brief flash of light polymerizes the liquid so that when the template is lifted off, a relief pattern of polymeric material is left behind. The features in the template need to be the same size as the final features (unlike current lithographic techniques where the mask is 4× the final feature size). NIL can deliver excellent resolution and good line edge roughness, but as a 1× technology where the patterning media (the template) actually touches the wafer, the major challenges for NIL are defects, contamination, and overlay issues.

Up until spring of 2015, there were few recent publications on the progress of this technique; but there was a company, Molecular Imprints, that was developing tools and techniques in conjunction with unnamed partners. In April of 2014, Canon Inc., a manufacturer of lithographic exposure tools acquired the semiconductor division of Molecular Imprints and renamed it Canon Nanotechnologies. This was a clear vote of confidence by Canon in the future of NIL. In February of 2015, a NIL development alliance of Canon with two major flash memory manufacturers, Toshiba and SK Hynix, was announced. Later at the 2015 SPIE Microlithography conference, a series of papers was given showing substantial progress in NIL, with improvements in throughput, overlay, and defectivity demonstrated. Overlay improved by a factor of eight in 2 years, and sub-5-nm 3 σ overlay was demonstrated. Throughput per imprint station improved fivefold to 10 wafers per hour. Overall process defectivity was reduced by two orders of magnitude to 9 defects per cm^2. The defectivity is not at the level desired for manufacturing flash memory yet, but progress is occurring at a rate that suggested it could get there by 2016 or 2017 [12]. Template (the NIL equivalent of a mask) improvement was also described [13]. Very low defectivity is achieved by making a master template, then inspecting and repairing it. The master template is used to make replica templates, which are in turn used to print the wafers. The replica templates are discarded after a certain number of uses. The replica templates were reported to meet targets for HVM.

Cost of ownership calculations suggested that a four-imprint tool system running 15 wafers per hour per imprint station would have a substantially lower cost than ArF self-aligned quadruple patterning (H. Takeishi and S. Sreenivasan, Op. Cit.). This cost advantage would drive implementation in cost sensitive products such as flash memory. This cost advantage was calculated for printing 15-nm half pitch. Printing larger features would give lower defects, easier template manufacture, and possibly faster throughput, which would lower the cost further. If this improvement in cost is enough, it could make nanoimprint a cost saving method for non-critical levels, too. If the cost benefit is enough, it would lower the cost of flash memory chips without shrinking the bit size. This could drive implementation of NIL because the alternative, shrinking the cell size, worsens the performance of planar flash memory.

4 Maskless lithography (ML2)

Maskless lithography involves using an e-beam writer to expose resist and write the desired pattern. It completely avoids any mask-related issues. E-beam-based patterning can provide excellent resolution but at the same time faces a pixel scaling challenge, which limits its productivity. Unlike optical lithography, pixel throughput gets slower as features get smaller. To overcome this, multi-e-beam column approaches are being pursued, where the tool will use many e-beams writing at once. Maskless tools are under development currently for both mask writing and for e-beam direct write of wafers. A multibeam tool designed for mask making has been shipped to a customer for field testing in 2014.[4] Such a tool is planned to take 10–15 h to write one 11-nm half pitch mask [14]. Substantial throughput improvements will be needed to make direct write for wafers feasible. The latest published report for e-beam direct write on wafers was provided by the MAPPER project in early 2015. Imaging results were reported for imaging with a 110 beam 'pre-α' MAPPER tool [15]. Mapper Lithography's published roadmap shows the development of a unit with a 10-wafer per hour throughput using 13,260 beams targeted at various layers for the 14-nm, 10-nm, and 7-nm logic nodes [16]. Given that 'α' tool was not ready for imaging in early 2015, substantial progress is needed in the next year in order for it to be under consideration for 2018 7-nm node volume production. At a minimum, a working α tool early in 2016 seems to be necessary.

4 http://semiengineering.com/executive-insight-elmar-platzgummer/, November 13, 2014.

5 Directed self-assembly (DSA)

Certain types of polymers can separate into different phases when annealing. If the polymer consists of two blocks of dissimilar materials, the size of the blocks will determine the size of the regions of different phase. This is called 'self assembly', and, in the absence of constraints or directing forces, will provide random patterns of the different phases. If some sort of constraint can be applied, the patterns can be made much more regular. For example, if the self-assembly is constrained between parallel linear walls, a pattern of lines can be assembled, or if there is a pattern of holes, self-assembly may give smaller holes within those holes. This directing of the patterns formed by applying constraints is called 'directed self assembly' or 'DSA'. DSA is not a stand-alone lithography, though it is sometimes referred to as lithography in a bottle. If DSA can meet placement and defect requirements, and DSA-friendly designs can be integrated with existing CMOS technology, it can make multiple patterning less expensive or make individual patterns better in quality or smaller in size, no matter what sort of patterning is used to print the guide patterns.

There has been much progress in the past few years for directed self-assembly. Reported defect levels have been reduced, and recent reports have suggested that defectivity is now at a level where it is not stopping manufacturing [17, 18]. New materials have been reported that show extendibility to smaller dimensions [19–21], and new process integration schemes have been demonstrated that enable easier cutting of the repeated arrays that DSA is good at preparing [22]. In 2014, IBM described the electrical properties of chips where DSA was used to pattern the fin arrays [23]. But implementation of DSA in manufacturing is still not a sure thing. As reported by Tokyo Electron, the current issues are related to design and process integration (M. Somervell, Op. Cit.). Micron reported that DSA gave somewhat worse LWR than the plan of record process for 16-nm NAND flash manufacturing. As a 16-nm half pitch requires quadruple patterning, this suggests that the LER of quadruple patterning is very good and that DSA LWR also has to be improved for line space implementation [24, 25].

6 Summary

In our 2011 article, when EUV lithography was the leading option after ArF immersion patterning, we suggested that it could start with manufacturing implementation in 2012 and be in production in 2014. However,

Table 1: Key targets and challenges for implementation of new patterning options.

Next-generation technology	First possible use in mfg	Feature type	Device type	Key challenges	Required date for decision making
Multiple patterning extension	2019	Sub-l0-nm hp fins in finFETs	'5-nm' node logic	– Printing and overlay of cut levels – Cost due to many masks	2017
EUV	2017 2018	22 nm to 26 nm hp CH/cut levels 16 nm to 20 nm hp LS	'10=nm' node logic extension, '7-nm' node logic, 19-nm DRAM	– Enough throughput – Defects from mask – Resist sensitivity and roughness	2015
Nanoimprint	2016	14-nm hp LS	Flash memory	– Detectivity – Overlay – Throughput – Template infrastructure	2015
DSA (for pitch multiplication)	2017 2018	Contact holes/ cut levels	DRAM logic	– Detectivity – Pattern placement – Design	2015
Maskless lithography (ML)	2018	Contact holes/ cut levels	'7-nm' node logic	– Throughput – Demonstrated – Multibeam tool	2016

delays in ramping EUV source power and tool availability have meant that only now are EUV tools mature enough for pilot line use. In the interim, much progress has been made in other next-generation technologies. In particular, Nanoimprint and DSA are much closer to manufacturing implementation than they were. But multiple patterning has also progressed, and quadruple patterning is clearly feasible. In 2014, the ITRS lithography roadmap published an update with the following Table 1 (Moore white paper from 2014 at http://www.itrs.net.) that showed the status as of 2014 of all the NGL techniques competing with multiple patterning, their implementation targets, and their key decision dates. Despite being 6–12 months old, Table 1 still is mostly accurate. One change we see is that EUV is likely to be used for a 7-nm logic node because competitive pressures are forcing fast roll outs of 10-nm node technology, which will have to use multiple patterning. We also see a probable 1-year slip in the earliest possible NIL implementation for memory manufacturing.

As quadruple patterning is known to work and is extendable to close to 10-nm half pitch, NGL techniques cannot just demonstrate resolution capability to be chosen for implementation. They have to also do something better than quadruple patterning does. DSA and NIL promise a lower cost. EUV promises a simpler and shorter process, the creation of 2-D patterns more easily with reduced complexity. Maskless lithography promises to make chip personalization easy and to be particularly cost effective for low volume chip designs. Decision dates for all of the technologies are this year or next year. We look forward to seeing how the industry progresses with all of these technologies.

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