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Research Article

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Computational metrology and inspection (CMI) in mask inspection, metrology, review, and repair

Abstract: Mask manufacturers will be impacted by two significant technology requirements at 22 nm and below: the first is the more extensive use of resolution enhancement technologies (RET), such as aggressive optical proximity correction (OPC), inverse lithography technology (ILT), and source mask optimization (SMO); the second is the extreme ultraviolet (EUV) technology. Both will create difficulties for mask inspection, defect disposition, metrology, review, and repair. For example, the use of ILT and SMO significantly increases mask complexity, making mask defect disposition more challenging than ever. The EUV actinic inspection and AIMS™ will not be available for at least a few years, which make the EUV defect inspection and disposition more difficult, particularly regarding multilayer defects. Computational metrology and inspection (CMI), which has broad applications in mask inspection, metrology, review, and repair, has become essential to fill this technology gap. In this paper, several such CMI applications are presented and discussed.

Keywords: computation lithography; computational inspection; computational metrology; computational metrology and inspection; mask pattern recovery.

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1 Introduction

As semiconductor manufacturing processes advance in step with Moore's law, the photomask industry has been increasingly challenged, especially as it entered the subwavelength era. When imaging subwavelength patterns, resolution enhancement technologies (RET) such as OPC, phase shift masks (PSM), subresolution assist features (SRAFs), source mask optimization (SMO), and inverse lithography technology (ILT), are often required, adding complexity to the mask [1–8]. The multilayer structure of mask blanks adds complexity in the case of extreme ultraviolet (EUV) lithography. How to inspect the EUV masks with multilayer defects, predict the impact of multilayer defects on wafer prints, and repair or compensate the impact of multilayer defects are challenging questions to answer. Computational lithography, which was developed primarily to address the lithography technology gap, can be borrowed, extended, and used for many operations that mask houses depend on to deliver quality, including inspection, metrology, review, and repair for both the advanced DUV lithography and EUV lithography. We call all such computational techniques computational metrology and inspection (CMI). CMI are mathematical approaches designed to improve the resolution, throughput, and accuracy of defect inspection, review, and repair in mask shops and wafer fabs. Using proprietary algorithms, defect images are processed and automatically analyzed in order to identify and provide advanced warning of wafer print errors that would adversely affect the final device functionality. This process eliminates wafer loss due to misclassified defects and can dramatically improve metrology and inspection cycle times in mask shops and wafer fabs.

Once a mask has been written in a typical mask house back-end flow it must go through CD metrology, mask inspection, repair, and the AIMS™ review. The AIMS review is also used before mask repair in some mask houses. Each step of the flow has a significant number of challenges and needs.

For example, customers are requesting many more CD measurements than before, and they are asking for the measurements to be made on real patterns instead of CD bars. In addition, wafer fabs are requesting wafer CD maps predicted from mask CD maps, so that they can feed

necessary information into the scanner to correct for CD bias.

Currently, disposition and classification during the mask inspection step are done by operators. An automatic defect classification (ADC) would help streamline this task and reduce variability from the operators' judgment. The situation gets worse when moving to the most advanced nodes, as aggressive OPC, ILT, and SMO make masks more and more complicated, and the resulting tiny jogs and features on the masks cause high-resolution inspection systems to flag many more nuisance defects, which must be reviewed and dispositioned by an operator. The other side of this 'coin' is that the operator may choose to reduce the sensitivity of the inspection system in order to reduce the number of defects for review to a reasonable level and thereby increase the chances that 'killer' defects will be missed.

In the AIMS review step, as the AIMS only provides the aerial image and not the wafer CD contour, the defect analysis is currently done by operators with the help of analysis software. This procedure is tedious. The result is subjective and may vary from operator to operator and even for the same operator from day-to-day. Furthermore, it is necessary to capture a reference image from another die or another identical pattern in the same die in order to calculate the relative CD error (CDE). Therefore, a die-to-database (D2DB) capability would be helpful, as it is often difficult to find a reference pattern on ILT/SMO type masks. Finally, because the AIMS only emulates the scanner aerial image, resist development is not emulated. This was never a problem in the past because of the good linear correlation between the AIMS aerial image CDE and wafer CDE; however, the high MEEF on more advanced masks unfortunately eliminates this simple linear correlation. Therefore, an AIMS to wafer capability is now seen as desirable by wafer fabs and mask houses.

Mask repair tools need a reference image in order to determine the repair area. A reference pattern generator (RPG) is needed for the same reason as described above for the AIMS D2DB capability. In addition, having a way to judge the repair quality before the mask leaves the repair tool would significantly improve the repair cycle time, compared to the alternative of sending the repaired mask back to the AIMS tool, possibly determining the repair quality to be inadequate and returning the mask back to the repair tool.

All of the challenges described above can be addressed by CMI, by applying technologies and modeling capabilities that have been developed for computational lithography. As shown in Figure 1, the basic idea is to simulate aerial or wafer images from data (mainly the images from all of the equipment used in the mask house back-end flow) and then classify and disposition defects based on their impact on wafer printability. As the data

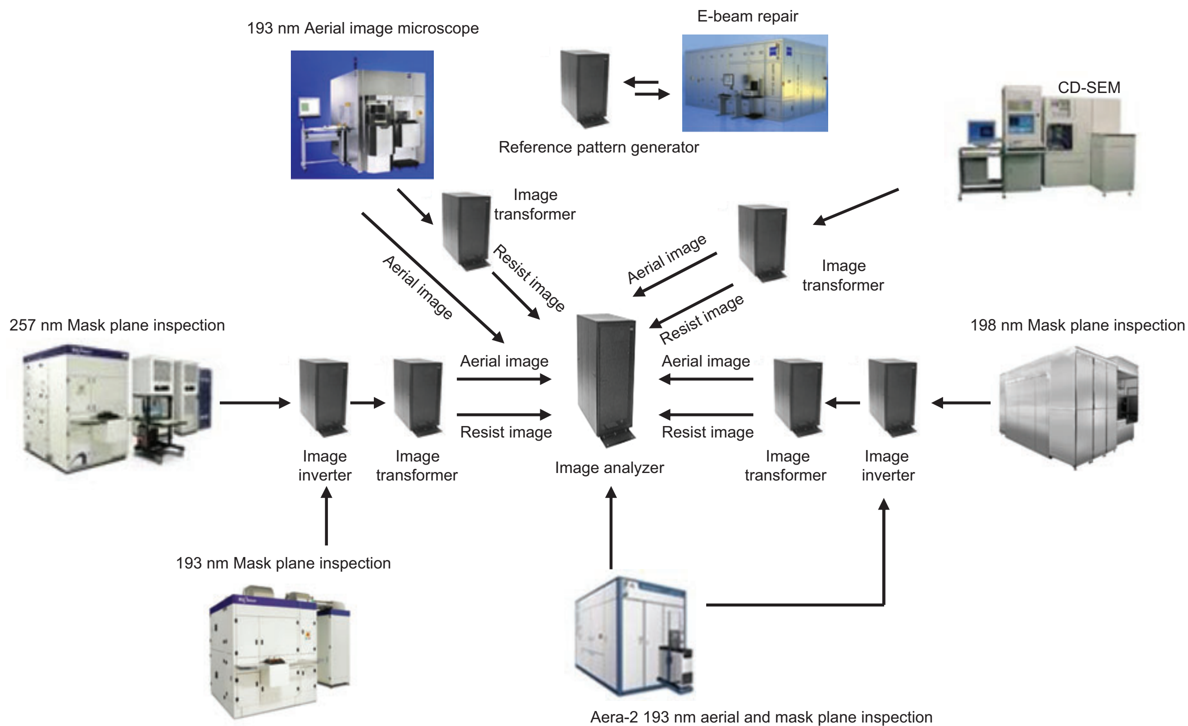

Figure 1 Diagram illustrating the general flow of CMI by LAIPH™ products for DUV masks.

are affected by the imaging systems of the equipment used to obtain them, a mask pattern recovery or reconstruction is needed before any litho simulation can be performed. In this paper, these applications of CMI in mask inspection, defect review, metrology, and repair are presented and discussed. The application for the AIMS review will be presented and discussed first. As AIMS is a hardware emulation that provides scanner aerial images, the mask recovery step is not needed, and it is directly linked to the aerial image analyzer (AIA), which serves as the central and common module of all of these applications.

2 Applications of computational metrology and inspection (CMI) in AIMS review

2.1 Aerial image analyzer (AIA): die-to-die (D2D) mode

The AIMS generates aerial images under a specific scanner setting, and such images are used to evaluate a mask defect's printability. Currently, such analysis is performed by an operator, with some help from software. For example, Figure 2 shows the manual flow performed by operators at the Taiwan Semiconductor Manufacturing Company (TSMC) mask shop [9]. First, the defect location is obtained from the inspection system. Second, the coordinates are passed to the AIMS, the stage is moved to the corresponding location on the mask, and the defect aerial image is taken. The reference image is also taken from the same location on another die by the AIMS. Third, using the AIMS software, one can determine the threshold to print the target CD on the reference aerial image. Fourth, using the same software, a defect CD can be calculated by applying the same threshold to the defect aerial image. In the final step, the CD error is calculated and reported to the TSMC E-Beam Operation's (EBO's, TSMC's mask production department) manufacturing system.

This complicated procedure must be repeated for each defect because a single threshold is not accurate enough to be applied to all features on the mask (similar to applying a variable threshold resist (VTR) model in OPC). Because this procedure is so complicated and tedious, and considering the TSMC's EBO output of more than 5000 masks per month, it is easy to see that the opportunity for operator error during this manual disposition is significant. In the new flow enabled by the AIA application on the Luminescent's Automated Image Processor Hub (LAIPH™, pronounced 'life') platform, the disposition of mask defects is fully automated [9].

Figure 3 shows the flowchart for both D2D and D2DB modes of AIA. Basically, the flow follows the operator manual flow: in the D2D model, both defect image and reference image are captured by the AIMS, and an aerial image to a wafer model (in this case, a local variable threshold model) is applied to generate the wafer contour. A relative CD error (CDE) is then calculated, and the defect disposition is done based on CDE. The actual software workflow is more complicated. For example, as the defect image and reference image are not guaranteed to be aligned, image alignment has to be performed. In addition, the AIMS image has also to be aligned with design target (in GDS or OASIS format) in order to obtain the target CD for the defect location, which is not trivial, as one is a grey-scale intensity map,

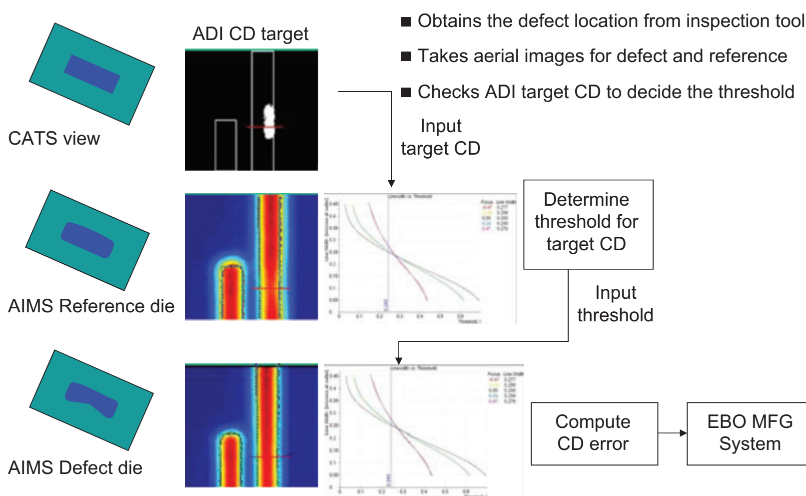

Figure 2 A typical defect disposition flow on AIMS.

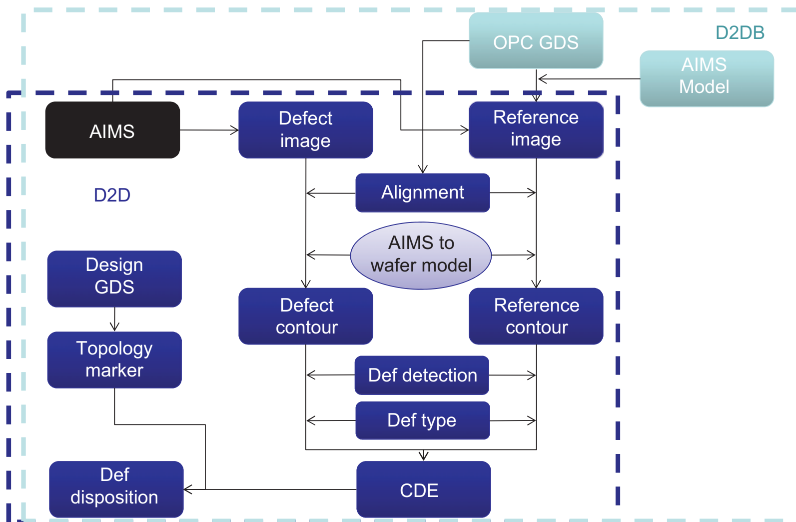

Figure 3 Workflow of the LAIPH AIA D2D and D2DB modes for AIMS.

and the other is a set of binary polygons. Defect detection must also be performed because defects may not be centered in image fields, and a single defect may actually affect the multiple features and spaces nearby. The software also classifies defects according to the types of patterns they affect, with categories such as line, space, corner, end-to-end, end-to-line, etc. In addition to mimicking what the operator is doing, AIA also automatically classifies the design target polygon into different topologies, so that different specifications and multiple level of tolerances can be set based on lithographic significance and to make it consistent with the specifications used in OPC and OPC verification. In the D2DB mode, the reference image is generated from OPC data (in GDS or OASIS format), so they no longer have to be captured by the AIMS, thereby reducing the machine time by 50%.

Figure 4 shows an example of topology on typical patterns. In AIA, the patterns are automatically classified into different topologies, such as smooth region, corners, end-to-end, and end-to-smooth regions. Different CD tolerances for defects falling into those different regions are then applied. In addition, the system can also read cutline locations and CD tolerances from the OPC and OPC verification database. This enables different sensitivity levels for different patterns and structures; for example, as also shown in Figure 4, contact coverage regions have higher sensitivity than other regions on metal, while metal lines have higher sensitivity than dummy contacts.

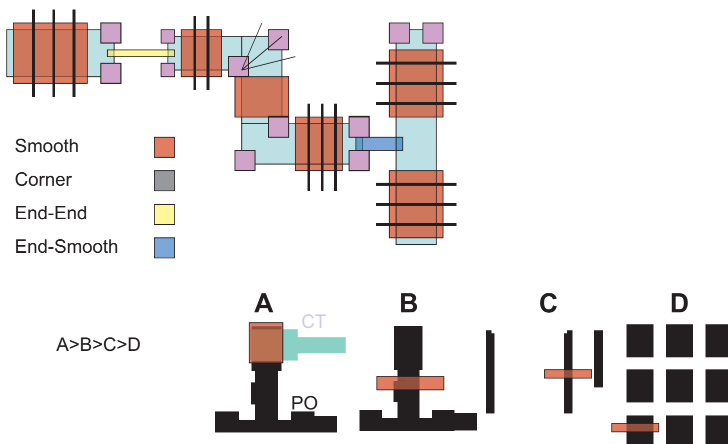

Figure 4 Topology marking in AIA – enables consistent lithography-based specs as OPC and OPC verification.

All of the calculations are done automatically without human intervention. Once all the defects are processed, AIA also provides an intuitive graphical user interface (GUI) in both native Linux/Windows and Web Browser for operators and engineers to review the final results. For example, as shown in Figure 5 (left panel), the GUI shows the defect list, including the disposition decision, defect coordinates, defect type, CD changes, etc. Also in Figure 5 (right panel), the GUI shows the aligned defect and reference AIMS images, the difference between them, the defect map (where multiple defects and multiple cutlines are shown), the aerial image intensity along a selected cutline location, and a zoomed image with design GDS and simulation contours. On the right bottom of the page, the user can write comments, change the disposition decision, and/or go to the next/previous defect. In general the operator is not required to make a decision; however, they do have the power to override the automated disposition decision (i.e., pass, waive, and fail) within the GUI and may also add additional cutlines for further simulations and calculations.

The LAIPH AIA has been used in production at all the TSMC EBO locations – one in Hsinchu and two in Tainan [9]. Figure 6 shows the pilot run results of the LAIPH at the TSMC. In Figure 6A, the manual measurements performed by the operator and auto measurements performed by the LAIPH are compared for both a contact mask and a line/space (L/S) type of mask. A line of matching slope 1.0 is drawn in each plot of Figure 6A, which represents perfect linearity between the manual and auto measurements. The fitted slope contact and L/S is 0.98 and R^2 is 0.99, indicating excellent matching. After reviewing outlying data points, it was found that errors mainly resulted from inadequate manual measurements. For example, as shown in Figure 6B, the major error on the contact layer was caused by not being sensitive to shift error in the manual operation, so the cutline was always drawn on the center of the defective contact. For the L/S pattern, the errors occurred mainly on 2D patterns, where it is difficult for operators to draw cutline exactly on the centers of rounded features. Throughput improvement using the LAIPH AIA auto measurements is significant. As shown in Figure 6C, it took an operator 40 min to perform the X/Y measurements on 17 blind or missized defects, while it only took the LAIPH AIA 1 min to have the entire mask checked and sizes measured along both axes. In addition, AIA also detects the contact shifts that the manual operation cannot.

2.2 Aerial image analyzer (AIA): die-to-database (D2DB) mode

Figure 7 shows an example of the LAIPH AIA D2DB mode. In D2DB mode, the reference image is simulated from post OPC mask database using a calibrated AIMS optics model. Although AIMS optics were designed to emulate the scanner optics, there are some significant differences; for example,

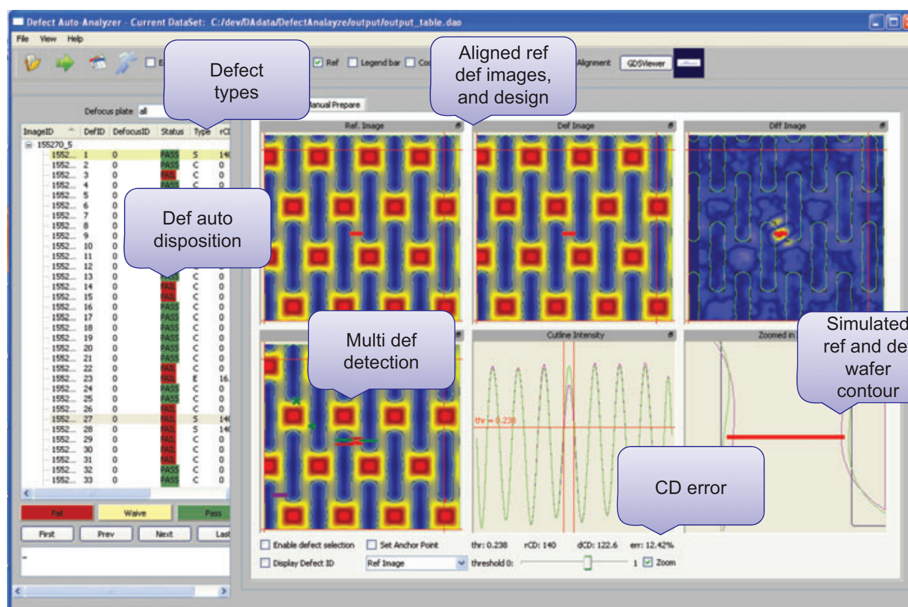

Figure 5 The LAIPH AIA GUI to review the defect disposition result.

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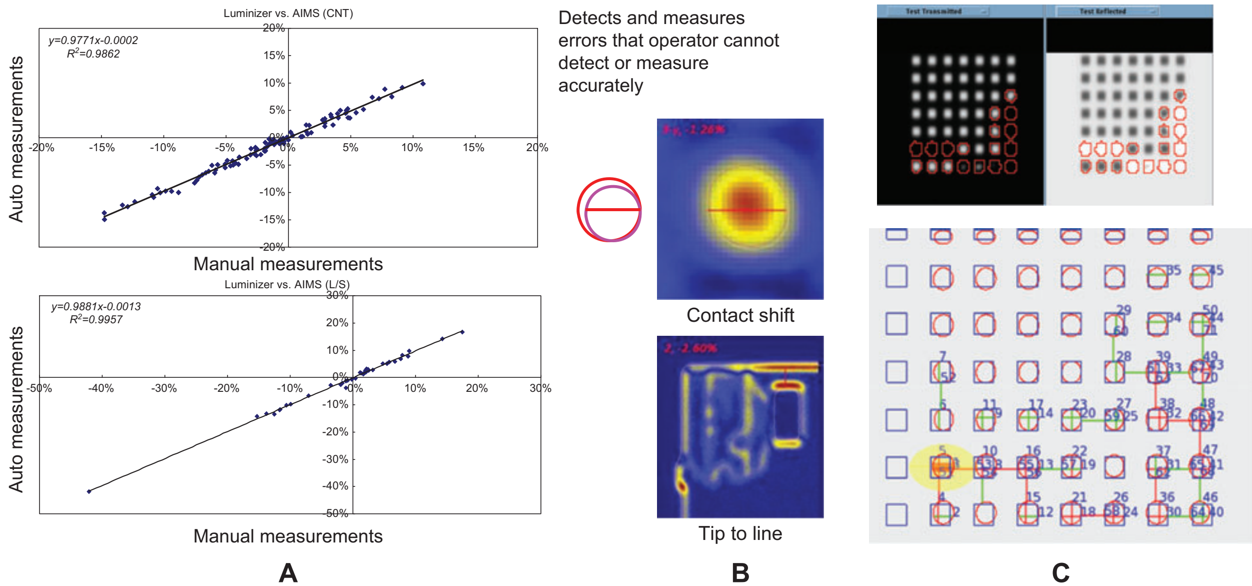

Figure 6 The LAIPH AIA production run result at the TSMC: (A) D2D accuracy, (B) examples showing AIA can detect and measure certain type defects that operators cannot detect or measure accurately; (C) an example of contact measurement coverage and speed.

AIMS systems operate at large magnification to capture images with a CCD sensor whereas scanners operate at 4:1 reduction. This difference is covered by the AIMS model, which is calibrated off-line for each node to ensure the accuracy of the simulated AIMS reference images. The details of the AIMS optics modeling was discussed in our EMLC 2012 paper [10].

Accurate AIMS modeling alone still cannot solve the problem. Each AIMS system has its own signature, requiring a customized model fit to its own images. Such model calibration is crucial in order to replace the AIMS D2D mode by the AIMS D2DB mode. AIMS model calibration is different from the OPC model calibration. The objective of OPC models is to predict CDs, either at specified cutlines, or along contours of pattern edges. A good OPC model does not necessarily have to calculate the intensity accurately to predict correct CDs. On the other hand, an AIMS model must calculate the intensity accurately everywhere to match each pixel of real AIMS images. For a given layout, this may involve fitting about an order of magnitude more data than that of the corresponding OPC model. Figure 8 shows an example of side-by-side comparison of the actual AIMS image and simulated the AIMS image using the calibrated AIMS model, where the intensity across the image is matched.

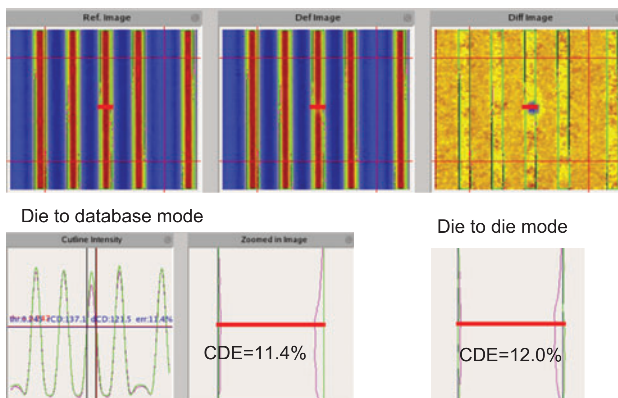

Figure 7 An example of the LAIPH AIA D2D, while the CDE is compared with D2DB mode.

2.3 Aerial image to wafer (A2W) – close the gap of AIMS aerial image CD and wafer CD

As AIMS is an optical emulator, the resist development is not included. This was not a problem for high k1 imaging using older technology because the image contrast is very high; therefore, the wafer CD and contour obtained by applying a simple constant threshold model or local threshold mode has an almost linear correlation to the real wafer CD and contours. However, such a simple correlation no longer exists for low k1 imaging due to the low image contrast; therefore, accurate resist modeling is desired by wafer fabs to predict wafer CDs from AIMS CDs.

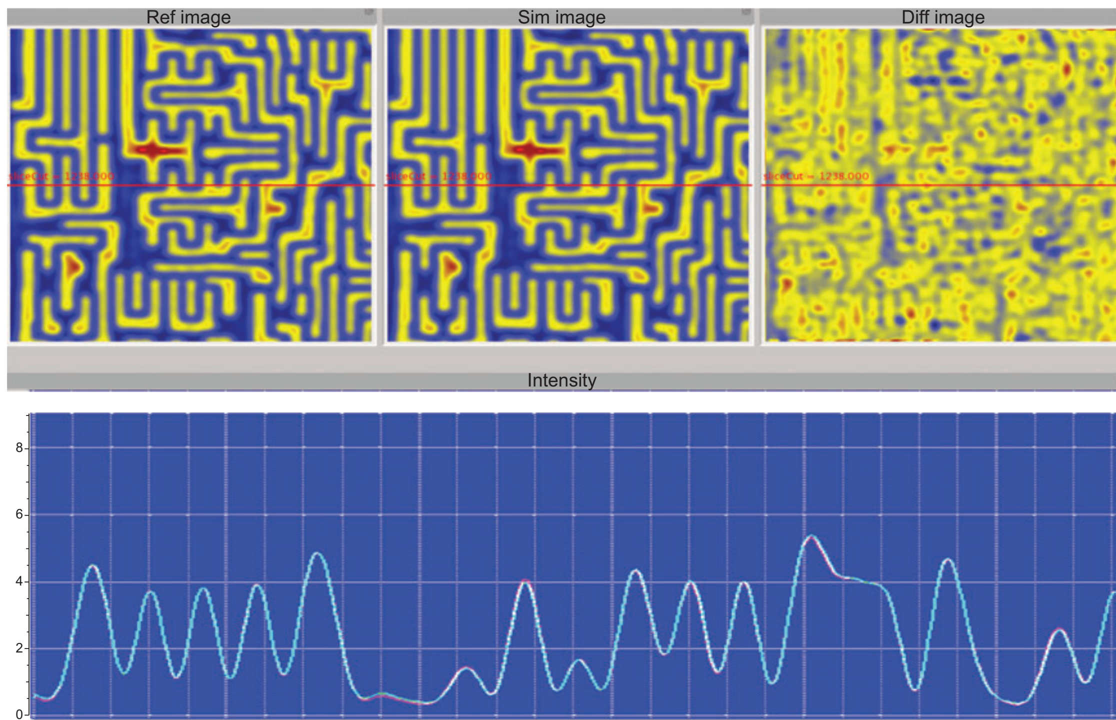

Figure 8 An example of the LAIPH AIA D2D, while the top row are actual AIMS image, simulated AIMS image, and the difference between those two (the scale is normalized against the maximum difference), the bottom graph show the intensity along the cutline for both the actual AIMS image and the simulated one. The range of Y axis is from 0 to 1, where 0 is for totally opaque region, and 1 is for totally transparent region.

Such tasks can be accomplished by computational metrology and inspection technologies as well. A resist model [either an empirical variable threshold resist (VTR) model or a physical resist model] can be built to simulate resist contours from the AIMS aerial images. Such a resist model needs to be calibrated to achieve the required accuracy. Just like calibrating an OPC model, such a resist model can be calibrated against real wafer data. Figure 9 shows the AIMS to wafer model calibration flow and an example of using a calibrated resist models, where the difference in simulated contours between using the local VTR model that was used in D2D mode and the calibrated physical resist model are clearly seen at the line end, where the image contrast is low. The threshold of the local VTR model is calibrated using the wafer line/space CD near the line-end, while the calibrated physical resist model is calibrated using wafer resist contours.

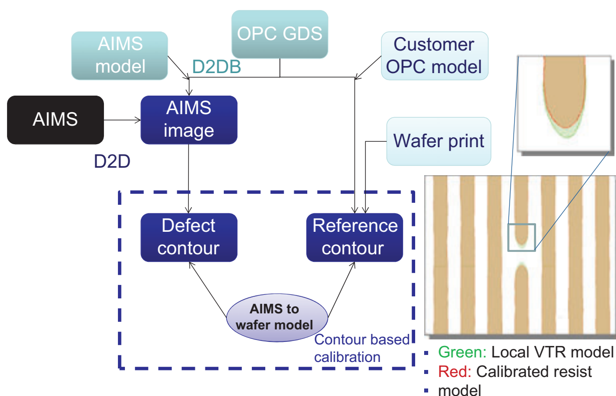

Figure 9 AIMS to wafer resist model calibration flow and an example showing the simulated wafer contour using local variable threshold model and calibrated resist model.

Figure 10 shows an example of the A2W result. To evaluate the resist model effect, for each CD group, a number of patterns with biases are created. For every bias, the simulated wafer critical dimension error (CDE) using A2W and the AIMS CDE are plotted against the wafer CDE. A slope is fitted among the data to obtain a matching slope. The closer the matching slope is to 1, the better is the prediction of the wafer CDE. As shown in Figure 10, the matching slope using A2W (the blue curve on the right plot) is much closer to 1 for through-pitch patterns, demonstrating that the A2W brings a closer match than the AIMS.

It should be noticed, although all of the above applications were developed for the AIMS, they can be adopted by mask inspection systems using aerial images, such as the AERA2 aerial image mask inspection systems.

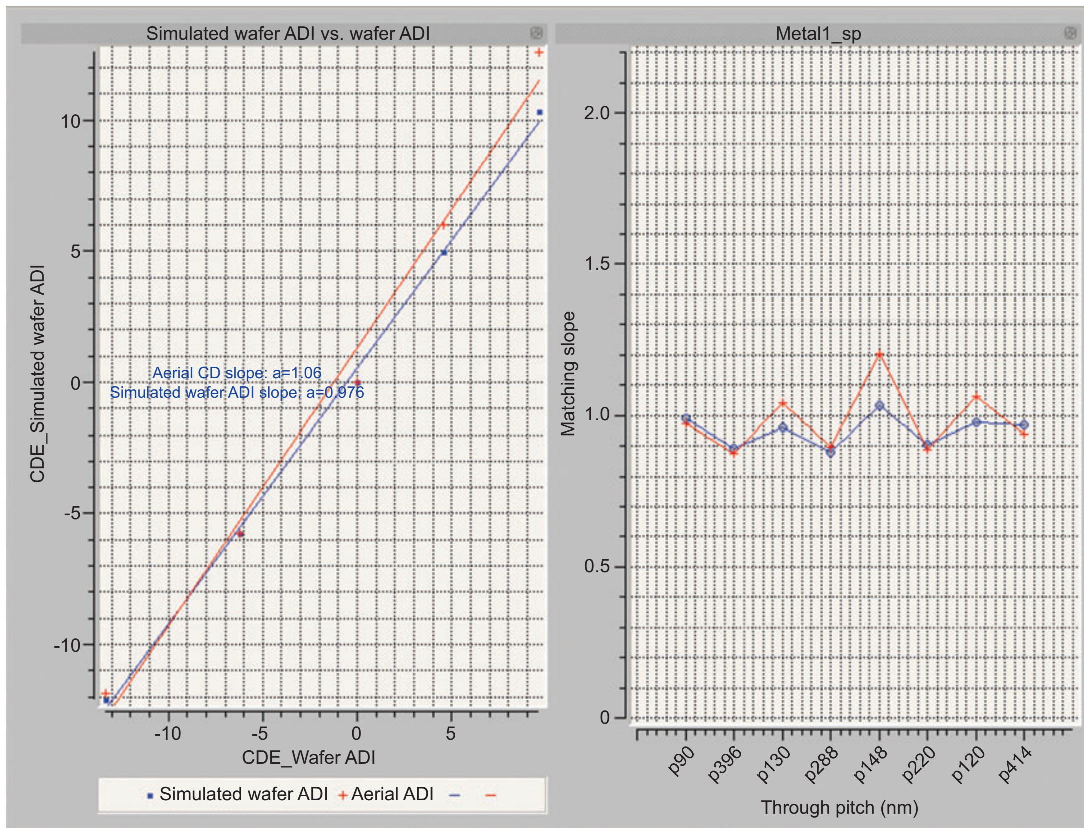

Figure 10 Example of the results of A2W. The subplot on the left shows the CDE between AIMS and the A2W for one CD group with different biases. The subplot on the right shows the matching slope for through pitch patterns.

3 Applications of computational metrology and inspection (CMI) in mask inspection

3.1 Automate defect review and dispositioning by automatic defect classification (ADC) and litho plane review (LPR)

Figure 11 shows an example of how ILT can be used to substantially increase the litho process windows. However, the resulting mask geometries and assist features, which play a crucial role in increasing the process window, also make the mask patterns more complicated and difficult to inspect, especially in high resolution [8].

Traditionally, mask inspection is performed at the highest resolution imaging mode. The mask inspection system is trying to capture the mask image as clearly as possible. This approach has been used for many generations of semiconductor design, but has become less straightforward after the 45-nm node. First, approaching the resolution limit in lithography necessitates more aggressive RET techniques being applied to the mask, resulting in mask patterns that deviate significantly from the design targets. A defect seen on the mask may or may not be indicative of its printing impact on the wafer (as shown in Figure 12A [11]) because of the varying MEEF factors between the different geometries and designs of the mask. For example, similarly sized defects could have a very different wafer printability impact depending on whether it is on the main feature or a SRAF, on a line/space or a hole pattern. Second, many tiny OPC decorations and defects are small, and due to the optical proximity effects, their signals are blended into the surrounding area. For example, as shown in Figure 12B, the pin-hole defect looks more like an intrusion or CD type of defect. This creates a dilemma for the inspection system of either flagging too many nuisance defects or lowering the detection threshold and missing some real defects. Such misclassification could also result in errors in dispositioning or repair.

Again, computational metrology and inspection can address the challenges discussed above. The end goal is to have an automated flow that allows the mask defect to

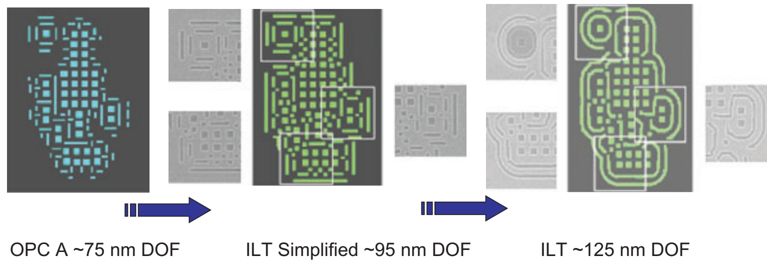

Figure 11 Example of the lithography performance gained by using ILT masks with different mask complexity.

be dispositioned without missing any killer defects and with a low false alarm rate, while at the same time, considering their wafer printability. One approach would be automating what the operator is currently doing manually – basically, to create rules and classify the defect based on those rules, just like what was done for the AIMS AIA. This is the safe approach for the mask houses, because the process is automated without changing any disposition rules. It may take months to build and fine tune the rules, especially rules that determine printability on the wafers. Another approach would be a (litho) model-based approach, where the defects are simulated at the aerial or wafer plane for review; in other words, LPR. The benefit of such an approach is that rules are unnecessary, and the mask defect disposition is directly linked to defect printability. Still, the computation and model accuracy requirement is high compared with the rule-based approach. Combining these two approaches into one hybrid approach makes it is easier for the mask houses to adopt it. This can solve the over detection problem with less stringent requirements on model accuracy.

Figure 13 shows the LAIPH mask defect autodisposition flow (start from left to right). The defects are first classified on the mask plane into defect types, such as MoSi extension, clear intrusion, chrome-on-shifter, etc., followed by location identification (on-edge, near edge, or isolated). Then all or part of the selected defects is run through the LPR to check their impact on the aerial/wafer CD. Finally, the ADC and LPR results are combined together, and a customized defect code is assigned to each defect (for example, both MoSi extensions, one affecting the CD for more than 8% and the other one affecting the CD for <8% have different codes).

Details of the LAIPH ADC results and accuracy can be found from the TSMC/Luminescent joint papers presented at photomask technology (BACUS) 2011 [12]. Figure 14 shows the ADC results on the 40-nm mask mass production at the TSMC. Basically, defects can be differentiated into two categories. One category includes defects that need post AIMS check or defect repair. The other category includes defects that do not need the AIMS check or defect repair, for example, false defects and nuisance defects. Here, we define defect 'classification efficiency' for a single mask product as the number of total false and nuisance defect counts classified by the ADC divided by the total number of false and nuisance defect counts classified by operators. A higher classification efficiency with no error in classification (especially

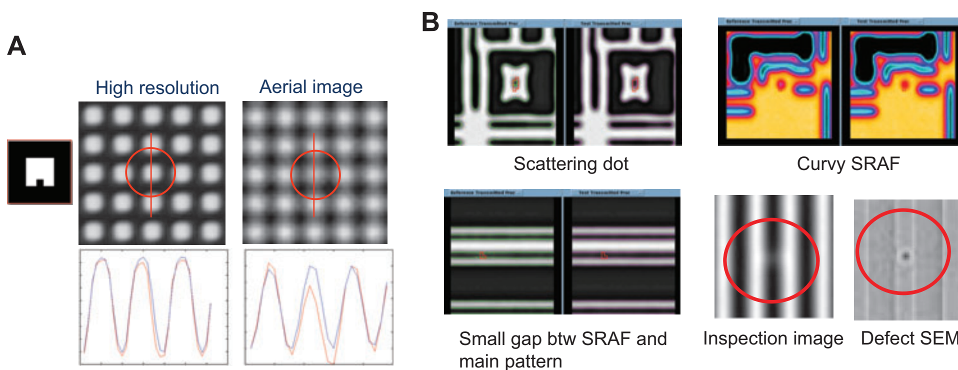

Figure 12 Challenges in high-resolution mask inspection: (A) the defect size on the mask does not reflect its impact on the wafer; (B) some small defects cannot be 'seen' even in high-resolution image mode.

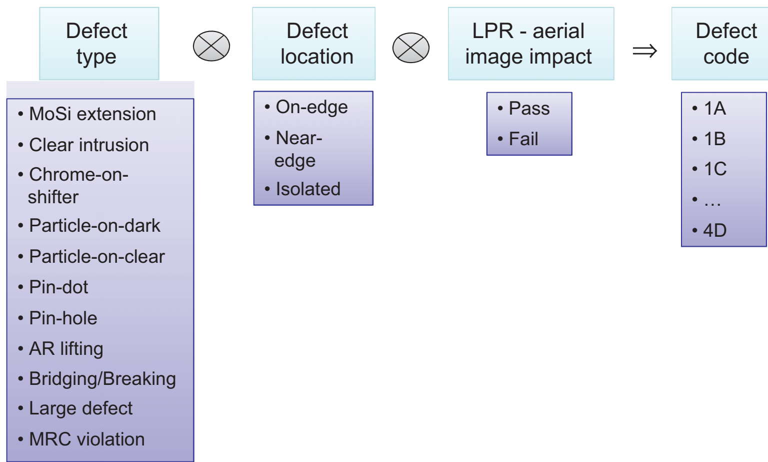

Figure 13 The LAIPH mask defect autodisposition flow for mask inspection off-line review.

for cases needing the AIMS check or defect repair) is required.

In Figure 15, the summarized results of 250+ plates of the mask products reveal that defect classification efficiency of over 95% has been achieved when comparing the ADC final classifications to the operator defect classifications. Moreover, no critical defect has been missed. In particular, classification efficiency for contact/via layer is higher than 100%, that is because operators tend to be conservative – they classified some false and nuisance defects as real, while ADC classified those defects as false and nuisance, and AIMS results verified ADC results are correct. Therefore, the ADC performance was proven to be qualified for the application of mass production.

Figure 16 shows the details of the LAIPH LPR flow. For the high-resolution imaging mode, the aerial image must first be simulated, and the rest of the flow is the same as the AIA used for the AIMS aerial image. In order to simulate the aerial image, the 'true' mask pattern must be recovered, followed by a scanner aerial image simulation. The key technology in such a flow is the mask pattern recovery, as without an accurate mask pattern, the aerial image simulation will not be accurate either. Details of the mask pattern recovery will be explained in section 6.

Details of the LAIPH LPR results and accuracy can be found from the Luminescent joint papers with the TSMC [12], Samsung [13], and Applied materials [11]. Figure 17

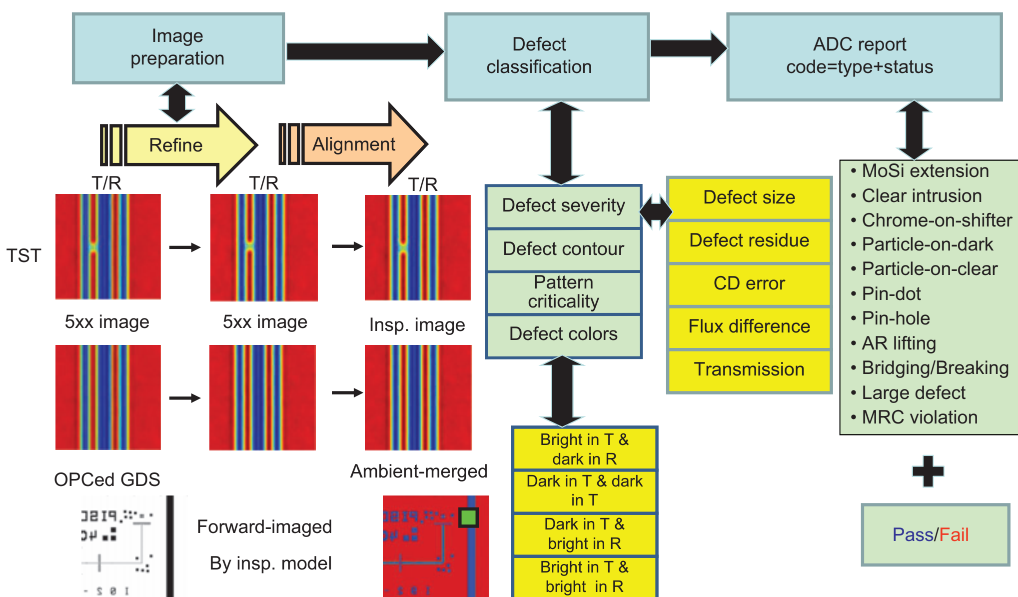

Figure 14 The LAIPH ADC workflow.

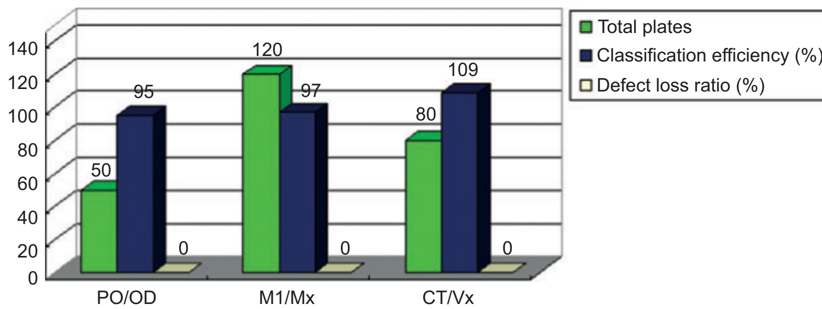

Figure 15 Overall ADC accuracy and efficiency at TSMC's 40-nm mass production.

shows four examples on the contact layer from the joint papers with the TSMC [12] – one MoSi extension on the corner, one pin-dot in the center, one clear intrusion on the corner, and one over-sized contact. One can notice that all of these defects are recovered from the high-resolution inspection image, in particular, the pin-dot defect, while it is not seen in the inspection image. Again, the accuracy of the inspection system optical model, the scanner aerial image, and the mask pattern recovery are demonstrated – the difference between the simulated reference aerial image and the defect aerial image at non-defect locations is very small.

Once the whole flow is running, it can replace the operator's manual defect disposition process. For a contact layer of the 45-nm node, the automated flow of the LAIPH system matched operator's disposition on 958 out of 969 defects, while the false alarm rate was 1.14%. The improvement in turnaround time is also significant. For example, the LAIPH system can disposition 250 defects per minute under the worst-case assumption that all defects have to go through the LPR, which is the most time-consuming operation because it requires mask pattern recovery and litho simulation.

4 Applications of computational metrology and inspection (CMI) in mask metrology

4.1 Wafer CD (WCD) metrology using mask CD SEM data

Mask manufacturers are limited to measuring CDs on masks, but their customers would prefer to know the CDs

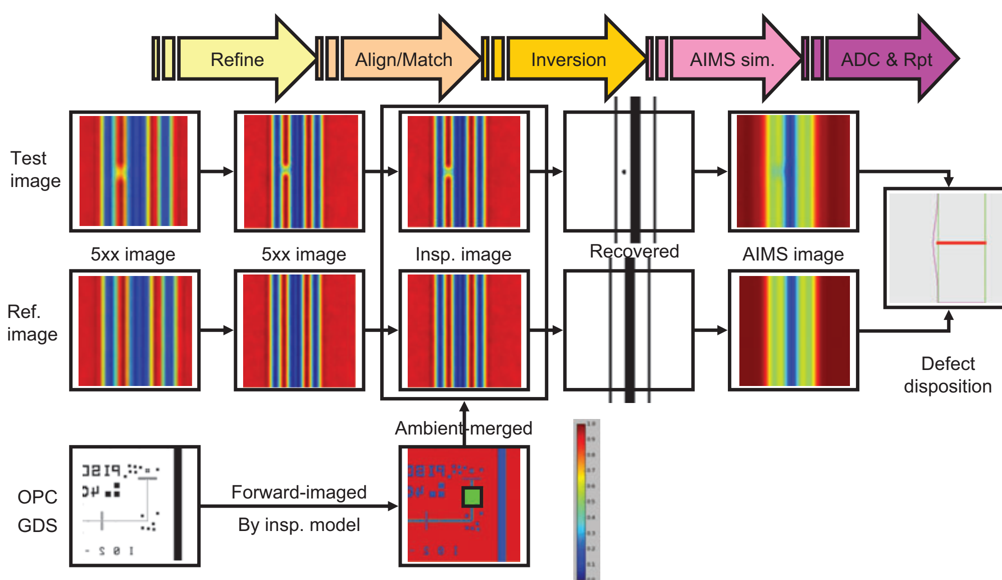

Figure 16 The LAIPH LPR workflow.

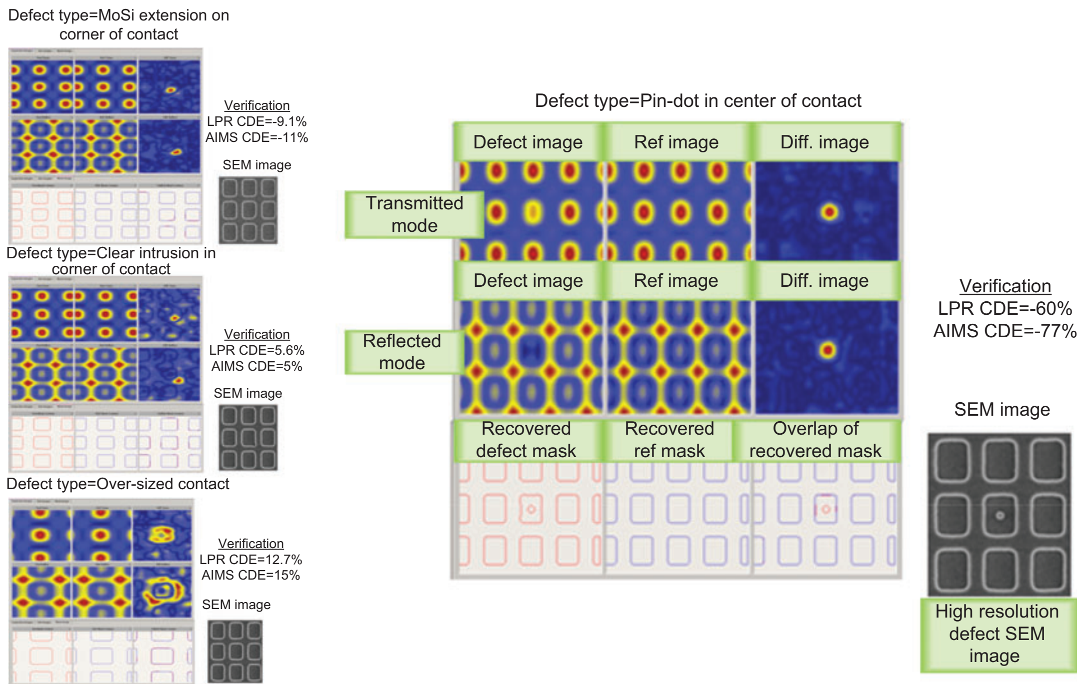

Figure 17 The LAIPH LPR results on a programmed contact mask, where the defect images, recovered mask patterns, its corresponding CD SEM image, simulated AIMS CDE, and real AIMS CDE are shown [12].

that the masks will produce on wafers. These can be predicted by applying CMI to data from the mask CD SEM. In the LAIPH wafer CD (WCD) metrology application, the first step is to extract CD contours from the CD SEM images as shown in Figure 18. Once the mask contours are available, one can use the fab OPC model to simulate the wafer pattern and CDs. However, there is trick here: the fab OPC model is calibrated using the wafer CD measurement against the design data (in GDS or OASIS format); in other words, the mask corner rounding and the mask bias that are introduced in mask making have been built into and considered in the model. Therefore, when the model is applied directly on the extracted mask contour, which already has the effect of corner rounding and mask bias, it is not accurate. Therefore, the trick is to remove such corner rounding and mask bias – convert the real mask contour back to 'post-OPC-like' pattern so that the OPC model can be applied (Figure 18). Such a

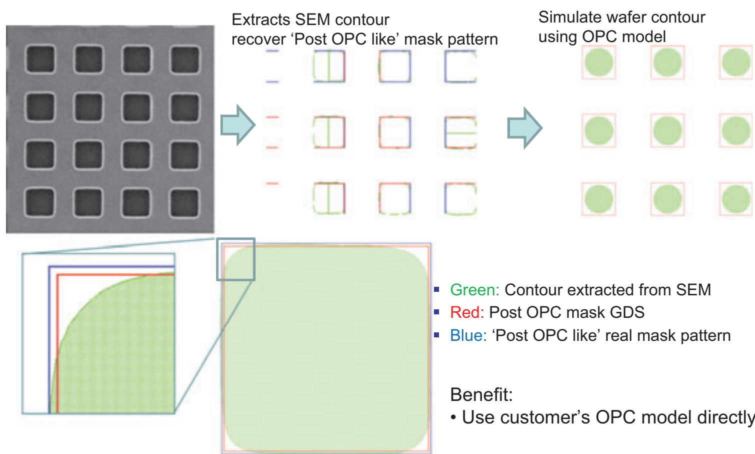

Figure 18 WCD metrology using mask CD SEM flow.

process is just another type of image inversion and can be solved as a constrained optimization, therefore, we call such process Inverse Pattern Recovery (IPR). As shown in Figure 19, the CD accuracy that has been achieved on such a reconstructed 'POST-OPC-like' pattern is ±1 nm for the 1D pattern and ±2 nm for the 2D pattern. More details about WCD can be found in the Photomask Technology (BACUS) 2011 paper [14].

5 Applications of computational lithography and inspection (ILT) in mask repair

5.1 Reference pattern generator (RPG) for mask repair systems

In order to repair a mask, one must know what the perfect pattern looks like. This perfect pattern is called the reference pattern. On the advanced mask repair system, once the reference image is obtained, the system can overlap the defect and reference the image (assuming they are perfectly aligned) and calculate the difference, which is the repair area. In the old days, such a reference pattern could be easily found in the nearby region or from another die. This becomes more difficult for the ILT and SMO types of masks, where the patterns may look similar but are actually different. Therefore, there is a need to have a RPG for the mask repair systems.

Figure 20 shows the workflow of the LAIPH RPG. The mask defect coordinate is passed from mask inspection or the AIMS review to the database server to clip the post OPC mask design. Such a clip is then run through a calibrated RPG model to simulate the reference SEM image of the mask pattern. Once the reference image is generated, it is uploaded to the repair system to calculate the repair area. The RPG model includes three parts: the mask process model for the mask corner rounding and bias, the SEM image profile model to render the SEM image, and the geometry distortion model to match the design to the real defect image. This includes rotation, scaling, and skew that are caused by stage and SEM scanning.

The key to deploying such an RPG application in production is simulation accuracy. The LAIPH RPG has achieved a very high accuracy – when comparing the simulated reference image with customer's real reference images the total number of pixel differences highlighted by the repair tools is <0.05% of the total number of pixels in the entire image. Figure 21 shows an example of this,

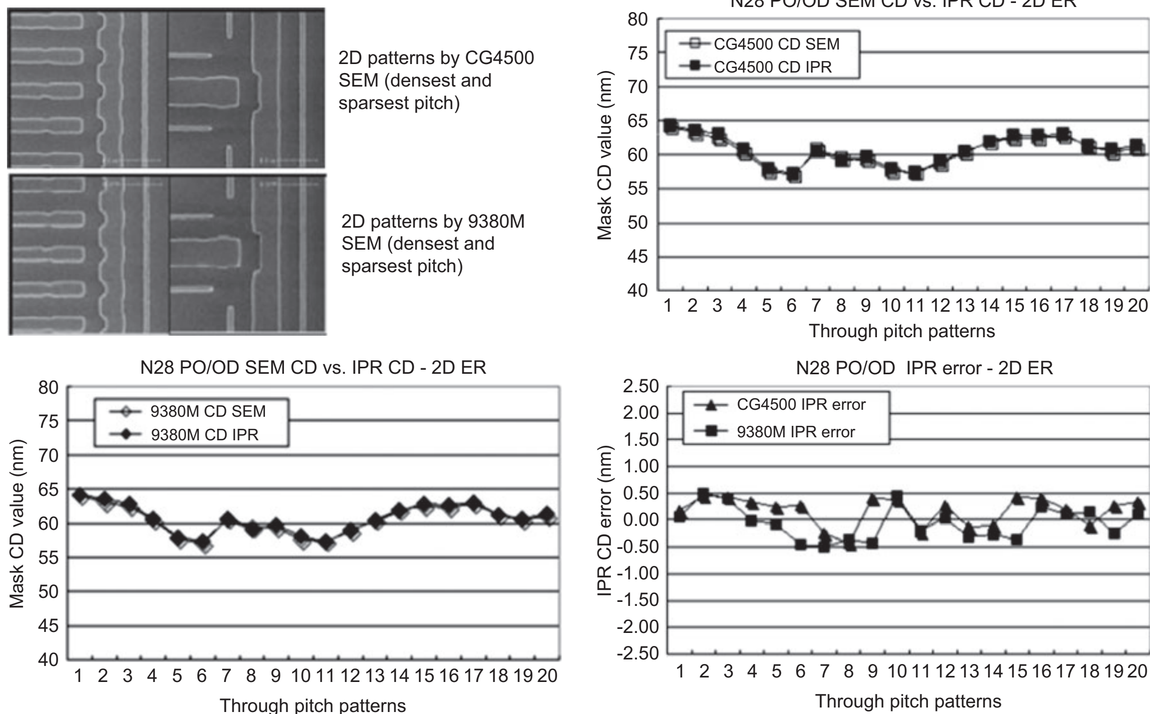

Figure 19 Example showing the CD measured on reconstructed 'Post OPC like' pattern from real mask and actual mask SEM CD.

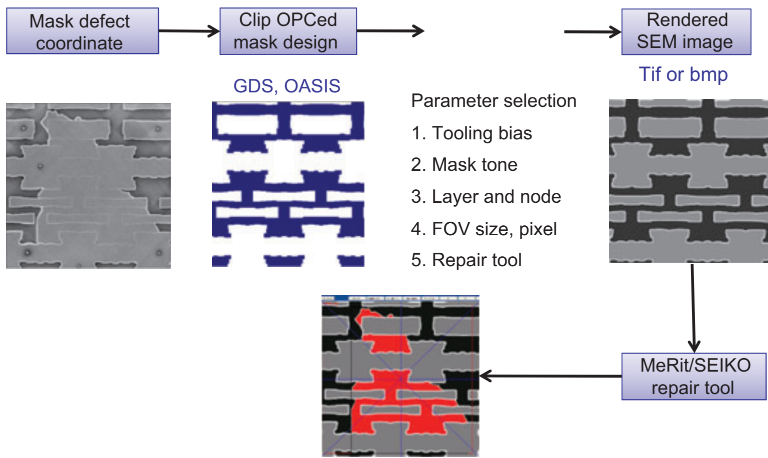

Figure 20 The LAIPH RPG for mask repair flow.

where pixel differences are highlighted in blue by the repair tool.

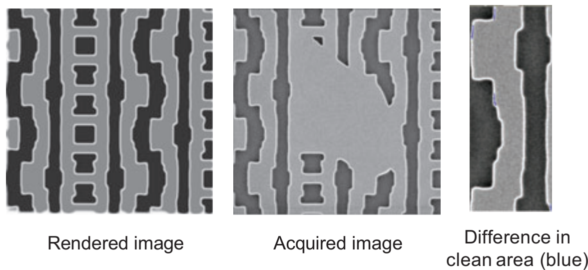

Figure 21 Example of the LAIPH RPG rendered reference image, the defect image, the real reference image, and the difference between the rendered and real reference image.

6 Inverse method in computational metrology and inspection

One of the key components of computational metrology and inspection is recovery of mask patterns from images obtained with various mask imaging systems. As illustrated in Figure 22, the data that are available at the mask houses are images of masks. For mask inspection, images are collected by a high-resolution optical imaging system. For the AIMS, images are collected by a microscope emulating the scanner optics; and for the CD measurement, images are collected by scanning electron microscopy. Owing to different imaging mechanisms mask data are captured, with some characteristics being amplified, some are filtered out, and others hidden by noise or limited

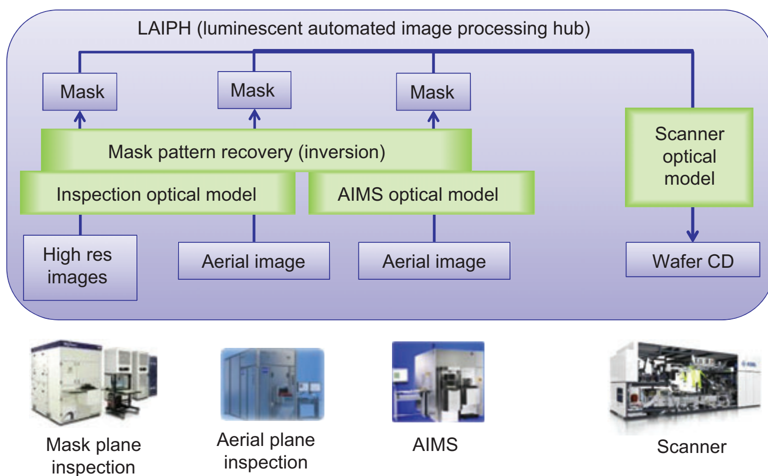

Figure 22 Diagram showing the mask litho simulation by using images from different mask imaging equipments must have to go through the mask pattern recovery step.

resolution. The first step is to recover the mask pattern, so that it may serve as input to an accurate simulation. The general inverse problem of retrieving an object from its image has been treated extensively in the literature. For the CMI applications, we can take advantage of the fact that the non-defective portion of the mask is essentially a two-dimensional binary object. This permits us to use inverse methods developed specifically for mask optimization, avoiding much of the ambiguity and difficulty of retrieving a three-dimensional, gray-scale object with more general methods.

The methods chosen for CMI are based on the same level set-based algorithms developed at Luminescent that are used in inverse lithography technology (ILT) to optimize the mask patterns from the intended wafer target [1] and to do SMO [15].

In this approach, the problem is treated as an image inversion problem and solved with optimization algorithms. As shown in Figure 23, the mask image system can be defined as the forward transformation operator f. Once we have a mask function ψ, the mask image obtained after the inspection system optics, ω, can be expressed as

$$\omega = f(\psi)$$

Now, we know ω, and we seek to find

$$\psi^{*} = f^{-1}(\omega)$$

where ψ^{*} is the recovered mask function.

This problem can be addressed by recasting the inverse problem as an optimization problem. We define a merit function, also called a cost function, energy function, or Hamiltonian (by analogy to quantum mechanics), and label it $H(\psi)$. This function is indicative of the quality of the solution, or the 'goodness' of the mask. A simple example would be

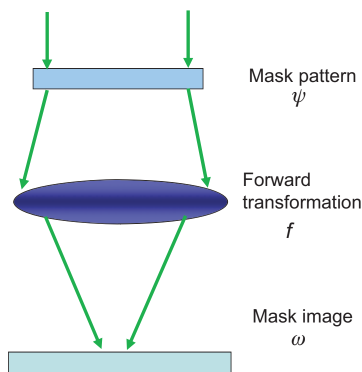

Figure 23 Illustration of mask imaging systems as a forward transformation.

$$H = \iint \left| f(\psi) - \omega \right|^{n}$$

In other words, this Hamiltonian is the absolute value of the difference between the simulated mask image and the real mask image, integrated over the area of the mask. The recovered mask solution minimizes the Hamiltonian subject to support constraints that the mask is a two-dimensional binary object with known transmission properties.

Now, the mask pattern recovery problem is formulated as a general multi-variate optimization, it can be solved using standard optimization algorithms, such as the conjugate gradient method. The challenges of such optimization problem have to do mainly with the scale of the optimization. which scales with the number of pixels used to represent the object.

One important aspect of the inversion problem is multiplicity of solutions. Aggressive OPC requires masks to be written with addresses much smaller than the pixels of inspection systems, so any inspection image can be fitted with many mask patterns that are indistinguishable within background noise limits. In these circumstances, solutions found by iterative optimization algorithms depend on their starting points. We take advantage of this by starting from something close to the solution (for example, a contour generated by thresholding the image). Because the goal of mask pattern reconstruction is to simulate its image with band-limited scanner optics, it is not necessary that the reconstruction be exact.

Our approach is to solve such problems by using the level set method. The level set method is a branch of applied mathematics that was invented by Professor Stan Osher (Luminescent's cofounder) and James Sethian in the 1980s. It has been applied in many engineering fields and is regarded as one of the most efficient mathematical methods in solving problems involving the dynamic change of 2D patterns with topology changes. The level set method-based ILT [1] was developed by Luminescent Technologies, Inc. from 2003 to improve the mask optimization efficiency and reduce complexity. Now the same mathematical framework can be applied to the mask pattern recovery.

The enabling technology in the level set method-based ILT is the level set representation of the design, mask pattern, and mask image. Representing the 2D design pattern, mask pattern, and mask image by level sets is mathematically efficient and gives the mask pattern practically infinite degrees of freedom to change shapes during optimization. It also solves the discontinuity

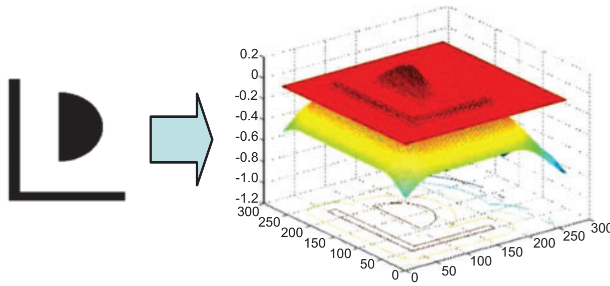

Figure 24 How to represent a 2D mask pattern by level set.

problem in the mathematical formulation when isolated defects are on the mask.

In the level set approach, the idea is to solve the problem in a higher dimension. One can take the original 2D curve and build it into a 3D surface by adding a mathematical function in the 3rd dimension. For example, as shown in Figure 24, one can define a distance function where the value (z) of this function for any point (x, y) is the shortest distance between the point to the nearest edge of the 2D curve. The surface representation will intersect the xy plane in a 2D shape, and the 2D shape on the xy plane (zero level set) is actually the original 2D curve.

The level set method also offers very efficient computational methods for optimization problems if the gradient of the function can be expressed in closed form instead of having to be calculated numerically. Many choices are available for the cost function. One can use the transmitted image, reflected image, both transmitted and reflected image, or through-focus images. There is no need to build an inverse model; it just uses the forward optical simulation model, which is well understood and studied in lithography modeling. For example, in terms of the inspection optics model, there is no need to know the exact parameters of the inspection system optics because, just like OPC, one can build a very accurate model by running the model calibration on a collection of test patterns (in this case, programmed defect masks). Most importantly, it can recover phase information from the same transmitted and reflected image. The details of mask pattern recovery using the level set method can be found in the reference [11].

7 Extension of CMI to EUV lithography

The EUV lithography is the leading candidate to replace optical lithography for semiconductor patterning. However, many issues are delaying implementation of the technology and may prevent its implementation altogether. One of the most critical problems is mask defects, specifically buried multilayer defects, which are unique to the EUV masks.

Buried defects in mask multilayers are major problems, which must be solved before EUV can be implemented. As Figure 25 shows, a substrate defect causing a very small multilayer surface bump can have an unacceptable effect on the wafer image. It is unlikely that defect-free EUV multilayers will be available for the production of the EUV lithography. A number of methods have been proposed to deal with this problem. One of the most popular takes advantage of the degrees of freedom wherein the pattern is located on a blank, shifting it so that the multilayer defects are covered by the absorber to minimize their effects on the image. This method works if the number of multilayer defects is sufficiently small, and the mask pattern has large absorber regions that may be suitably placed to cover them. It is therefore best suited to sparse, darkfield patterns. The probability that a solution exists decreases as the number of multilayer defects increases or the density of absorber in the mask pattern decreases. Whether a solution exists for a particular blank-pattern combination depends on specific coordinates of the defects and absorbers. Therefore, a better approach is required to relax or eliminate those limitations.

7.1 Full defect printability simulator (DPS) algorithm

In order to make any simulation-based compensation work, computation of the EUV images affected by the multilayer defects must be fast and accurate. There have been many proposals for producing high-quality masks from defective multilayers, and each requires accurate simulation of the mask image due to the pattern and buried defect. Rigorous methods, such as the finite difference time domain (FDTD), are accurate, but are too slow to be useful for most applications. Therefore, a new multilayer model has been developed and integrated into a new simulator for the EUV masks with buried defects. This new model is 4–5 orders of magnitude faster than the FDTD method, but has comparable accuracy.

The overall simulation flow for the Luminescent defect printability simulator (DPS) is based on that of the simulator RADICAL developed at the University of California, Berkeley [16, 17]. DPS is designed specifically to simulate the EUV masks with buried defects. Speed and accuracy of algorithms used to compute the EUV images are optimized for this particular application. Figure 26

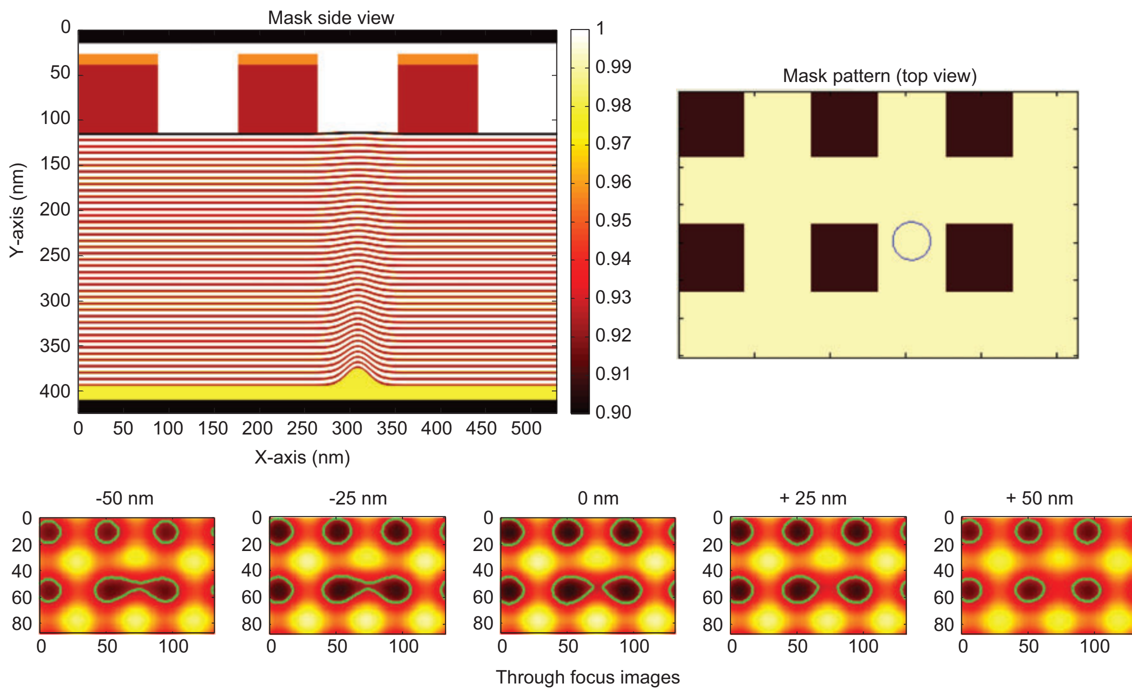

Figure 25 Example of defective EUV multilayer geometry, mask pattern, and resulting through focus wafer images.

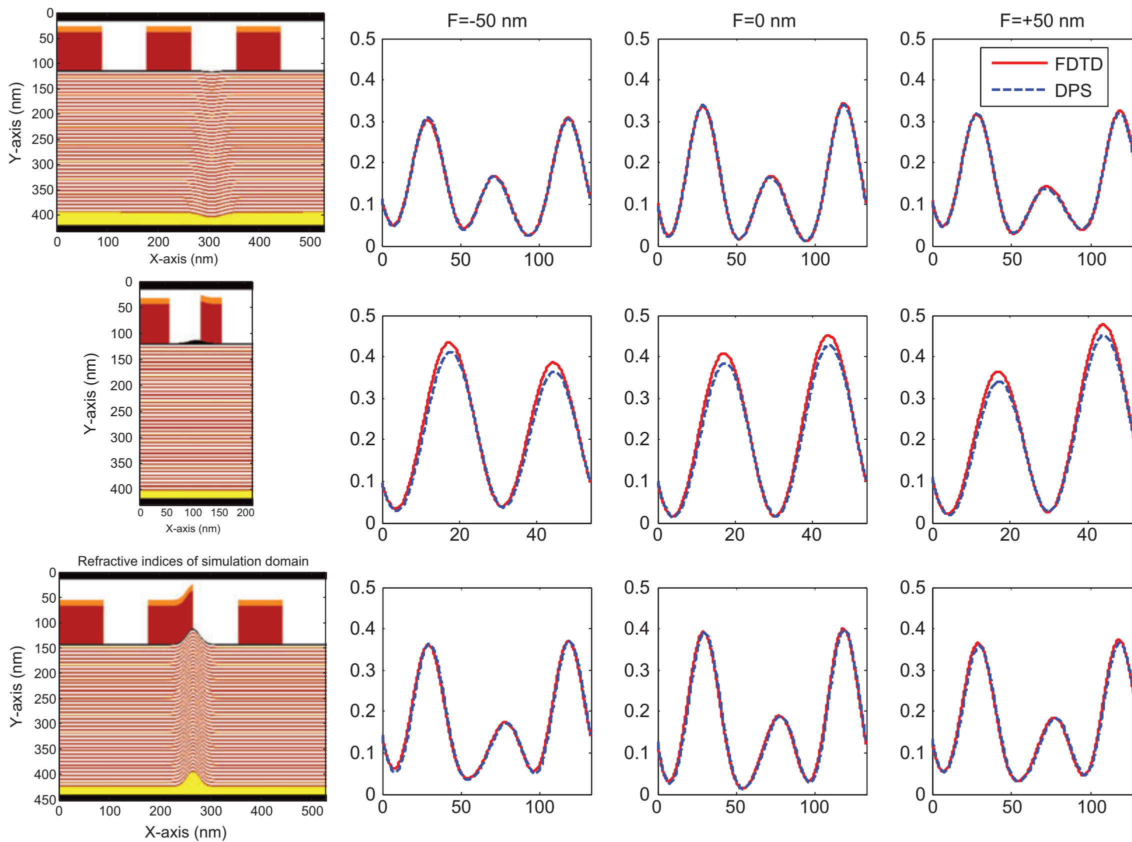

Figure 26 Aerial image cutline comparison for the three geometries. (A) Pit defect on the substrate. (B) Bump defect on the top of multilayer. (C) Large bump defect with conformal multilayer growth model.

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shows the comparison between a three-dimensional FDTD simulation and a three-dimensional DPS simulation. Because the FDTD is so computationally intensive, only a small EUV mask area could be simulated. As one can see from the result, the differences between the FDTD and the DPS are very small and within the uncertainty range of the FDTD simulations. Therefore, the conclusion of this accuracy analysis is that DPS has comparable accuracy to FDTD [18].

The DPS was created because the conventional simulation methods were too slow for the defective EUV mask simulation. The increase in the DPS runtime as a function of the mask area is summarized in Figure 27 along with an approximation of the corresponding FDTD runtime. It shows that the DPS is consistently 4–5 orders of magnitude faster than FDTD [19].

7.2 EUV multilayer defect compensation (MDC)

It is unlikely that the EUV multilayer blank that meets the defect specifications will be available when the EUV goes into production. Therefore, some method is required to create a useable mask from a multilayer with buried defects. One possible method is to reduce the EUV defect printability by changing the absorber pattern to compensate for the buried defect.

Figure 28 shows the MDC flow that can be integrated into an e-beam mask repair tool [19]. First, an absorber pattern contour is extracted using the SEM image module in the repair tool. It is then aligned with the 3D profile of the top layer obtained from the atomic force microscope (AFM) module to accurately identify the relative location

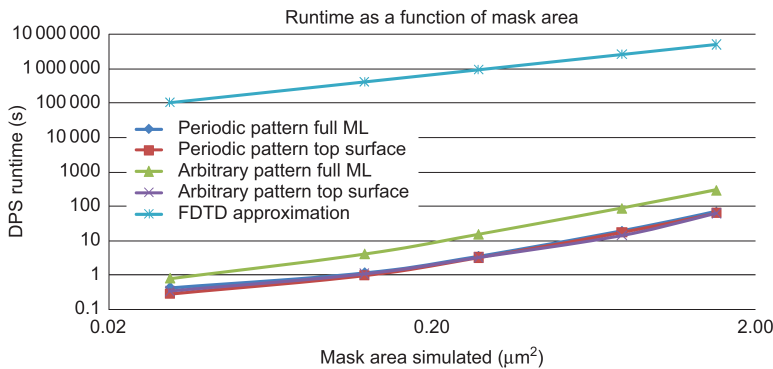

Figure 27 Comparison of runtimes for four of the DPS scenarios and the predicted runtime of FDTD.

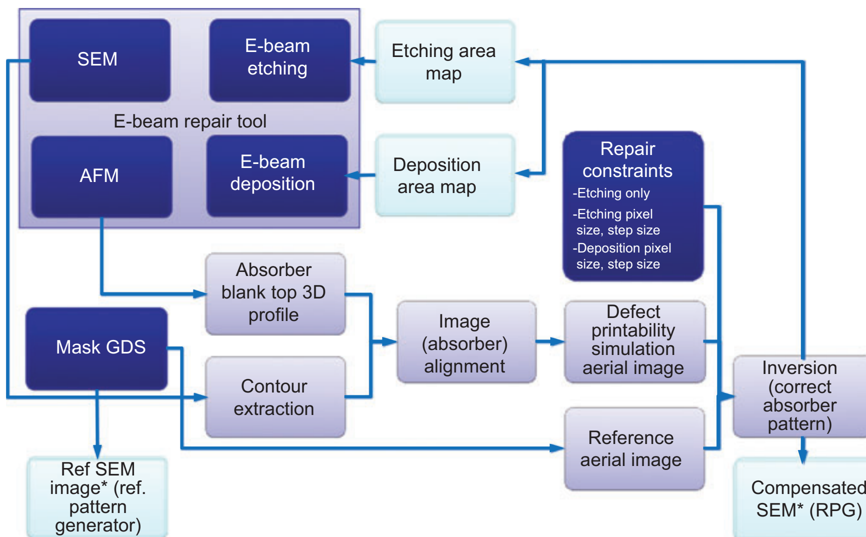

Figure 28 EUV multilayer defect compensation flow.

of the multilayer top layer profile with the SEM image. The multilayer defect location is accurately shown on the AFM 3D profile, but not on the SEM image, as the SEM image only has signals on the sharp edges. Therefore, this alignment step is very important because, later on, the compensated absorber pattern will be rendered on the SEM image, and the repair tool will use that SEM image to perform repair. The aerial image is then simulated using either the Single Surface Approximation (SSA) model or full multilayer model combined with a multilayer growth model. This provides the aerial image to be corrected during compensation. The reference aerial image is simulated from the mask target in GDS format, also using DPS. This becomes the target aerial image that the compensation attempts to achieve. An 'inversion' (optimization) is then run to make the aerial image with the multilayer defect approach the reference aerial image by modifying the absorber pattern. Such 'inversion' is a constrained optimization; in other words, the repair tool constraints are used to guide the solution to produce the absorber patterns that the repair tool is able to make. For example, an etching-only optimization is run first, searching for a solution by removing the absorber pattern only, as etching is easier to perform, and it has higher accuracy on the repair tool. If that does not work, etching and deposition are both allowed in the optimization. In either case, the etching pixel size, step size, the deposition pixel size, and step size are specified and used as constraints. Once the inversion converges, the etching area map and the deposition area map can be extracted, generated, and sent to the etching and deposition modules of the repair tool to perform the absorber pattern repair. E-beam mask repair tool is used here just as an example to illustrate how MDC works; MDC works, with other repair scheme as well, such as nano-machining.

Once again, the level set method was used here to calculate the compensated absorber pattern shapes. Simulations show that this method works for all the situations as long as the wafer CDE impact from multilayer defects is within a certain range. It can compensate both bump and pit multilayer defects, regardless of their locations. Figure 29 shows bump defects with different sizes. Figure 30 shows pit defects at different locations. All are nicely compensated [19].

7.3 Multilayer defect reconstruction (MDR) and calibrating multilayer defect growth model

DPS can simulate printability of the multilayer defect knowing the dimension and deformation of the multilayer. It is a useful tool to understand the behavior of the multilayer defect; however, in real applications like MDC, that information is, in general, not available. Therefore, how to reconstruct the multilayer deformation from limited information and how to calibrate the multilayer growth model are very critical.

Borrowing ideas from computational lithography, particularly OPC model calibration, the multilayer growth model can be calibrated using the data collected from the programmed multilayer defects. Instead relying on CD SEM to measure wafer CDs, AFM is used to measure the top layer profile, and TEM is used to measure the multilayer cross-section deformation. A multilayer growth model calibration engine was

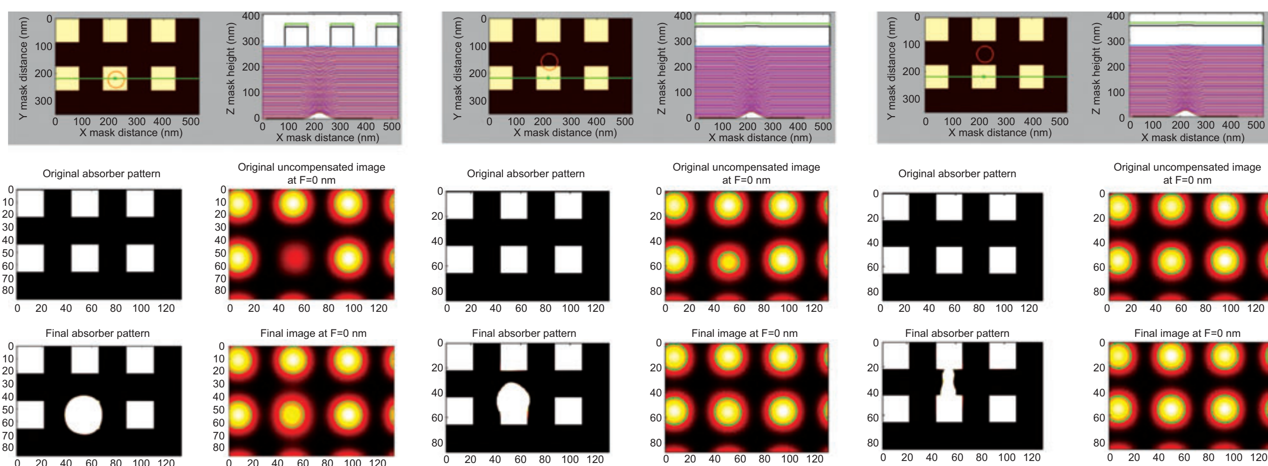

Figure 29 Examples of bump defects located at the center, edge, and between contacts that can be compensated.

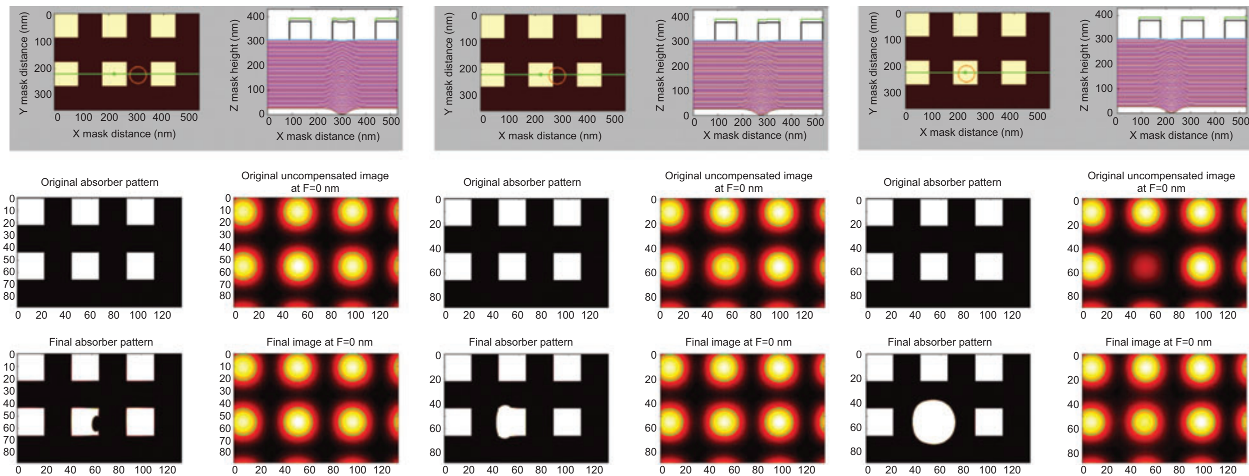

Figure 30 Examples of pit defect located between contacts, on the edge, and at the center of contact that can be compensated.

developed to calibrate the multilayer growth model using those real measurements.

Once the multilayer defect growth model is calibrated, it can be applied to multilayer defects in real applications, such as MDC, to reconstruct multilayer defects from the limited information that can be obtained from the measurements. This process is called the MDR. Figure 31 shows an example of the MDR [20]. Blue lines are predicted multilayer profiles obtained from the MDR, and the predicted multilayer profiles were overlaid on the actual TEM images. The multilayer profile obtained from the MDR using only the top surface AFM data is well matched with the actual TEM images.

The multilayer structure regenerated from the MDR was used for the inputs of the DPS as shown in Figure 32 [20]. Through-focus images of the multilayer phase defects were obtained at Actinic Inspection Tool (AIT) using 0.2 sigma and 0.35 NA. The DPS aerial intensities were calculated at the same illumination condition as the AIT, and the DPS aerial intensities were compared with the AIT intensities. The AIT intensities and the DPS aerial intensities were obtained from the multilayer phase defects without the absorber layers. The DPS aerial intensity profiles were well matched with the AIT intensity profiles.

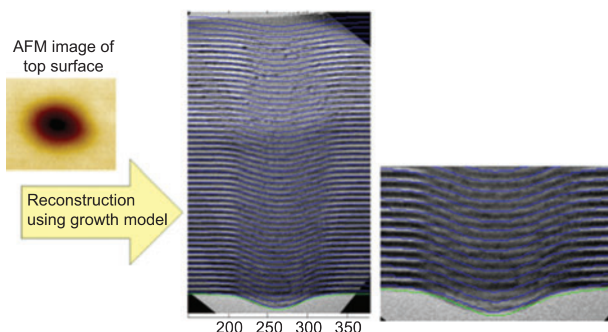

Figure 31 Examples of reconstructed multilayer profile. Blue lines are reconstructed multilayer profiles overlaid on actual TEM images.

8 Conclusions

As technology advances to 32 nm, 22 nm, and beyond, the methods used to inspect the masks and disposition defects require significant changes. The basis of accurate disposition should be the wafer images affected by defects, rather than raw images of the defects themselves. Computational lithography provides the necessary simulated images. CMI provides the means to perform disposition on the simulated images without relying on subjective judgment.

CMI addresses the challenges and requirements of the mask house back-end process. The WCD SEM using the mask CD SEM data provides wafer fabs with predicted wafer CDs so that they can improve CD uniformity even before the wafer is printed. Mask ADC with Litho Plane Review (LPR) reduces noise, prefilters the defects, and eliminates the missing killer defect problem. The AIA automates defect disposition for both the AIMS™ and the AERA2™ inspection systems. The AIA D2DB reduces the AIMS machine time by half and provides a consistent reference for high MEEF mask patterns. A2W bridges the gap of aerial image and wafer CD by adding a calibrated resist model. The RPG provides the reference image to mask the repair tools, making automated repair a reality. Its

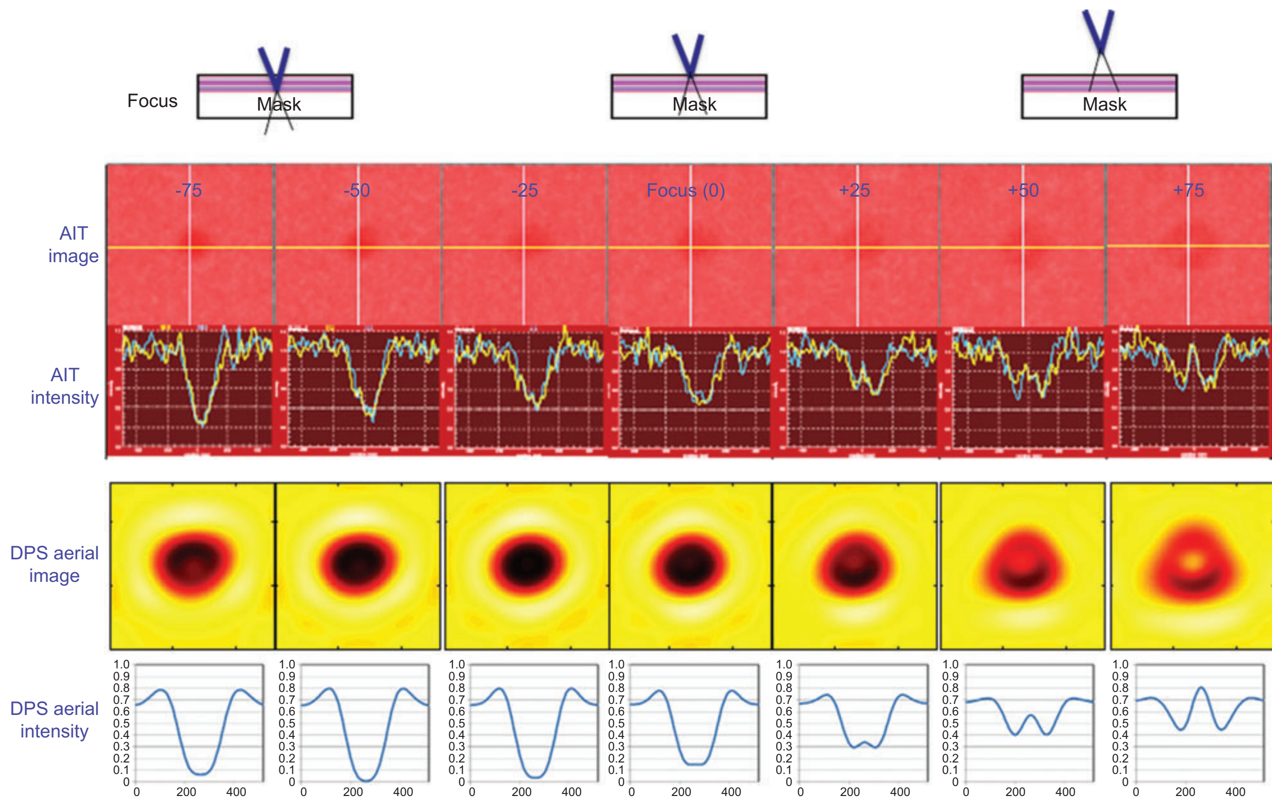

Figure 32 Examples of intensity comparison between AIT and DPS.

extension can also be used to evaluate the repair quality before the mask leaves the repair tool.

CMI is also extended into the EUV lithography to address the key challenges of the EUV mask defect inspection and repair. First, a new EUV DPS, which is 4–5 orders faster than rigorous FDTD is developed to simulate the aerial image with the multilayer defects present. With such a fast EUV multilayer defect simulation, the multilayer defect compensation calculation becomes possible. The MDC by the absorber modification is a promising method for reducing the impact of the multilayer defects. Simulations show that this method works for all situations as long as the wafer CDE from multilayer defects is within a certain range. It can compensate both bump and pit multilayer defects, regardless of their locations. Calibrating an accurate multilayer growth model and reconstructing a multilayer profiles based on available limited information is crucial for MDC.

To achieve an accurate lithography simulation, an accurate mask pattern is essential. Mask pattern recovery based on the level set methods can accurately recover the mask patterns from their images obtained with standard equipment in use by mask manufacturers.

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Dr. Lin He is currently the Senior Research and Development Engineer at Luminescent Technologies. Dr. He joined the Luminescent in 2008 and has played a critical role in developing many cutting edge products in the photomask inspection area and the wafer image inspection area. Some of the products are the industry's first off-line computational inspection products and have brought multi-million dollars to the Luminescent. Prior to joining Luminescent, Dr. He received a PhD Degree in Applied Mathematics from the University of California, Los Angeles and a BS Degree in Mathematics from Peking University.

Dr. Ying Li is currently a key developer in lithography model team at Luminescent Technologies. Dr. Li joined Luminescent in 2009, she's been working on building and improving DUV optical models in the most advanced technology nodes. Dr. Li also pioneers in EUV optical model development and buried defect printability analysis. Prior to joining Luminescent, Dr. Li obtained a PhD degree in Physics from Georgia Institute of Technology, USA and a BS degree in Physics from Peking University, China. Her research focus on large scale quantum simulation of fermionic clusters.

Masaki Satake is currently Senior Application Engineer, Computational Defect Management Group at Luminescent Technologies. He joined Luminescent in 2010 and has been working for application engineering and development of products. Prior to joining Luminescent, he worked at lithography process R&D division in Toshiba. He has 2 issued patents and 11 pending patents. He received a BS in applied chemistry and a MS in material science and engineering from the Nagoya University in Japan.

Vikram Tolani is currently the Director of Applications Engineering at Luminescent Technologies. He joined Luminescent in 2007 focusing on product management, and, application development using novel computational inspection and metrology technologies. Prior to Luminescent, Vikram worked at Intel Corporation's mask shop as a Sr. Process Engineer in the inspection and repair areas.