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Research Article

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Global shutter pixels with correlated double sampling for CMOS image sensors

Abstract: This article describes the operation and performance of global shutter pixels with correlated double sampling for CMOS image sensors. Correlated double sampling is required to keep the read noise at a level comparable to interline transfer CCDs. A pixel with voltage domain in-pixel sampling of the floating diffusion reset and signal levels is explained and its noise performance is modeled. The saturation level of this pixel is analyzed and parasitic light sensitivity is discussed. The pixel is benchmarked against other global shutter pixels that allow correlated double sampling, based upon charge domain in-pixel storage.

Keywords: CMOS image sensor; global shutter; pixel.

OCIS codes: 040.1240; 040.1520.

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1 Introduction

Industrial vision cameras require global shutter pixels and good image quality. A global shutter is available in interlined transfer (IT) CCD devices for a long time. The signal in an IT CCD is synchronously transferred from the pinned photodiodes into the vertical CCD shift register, and correlated double sampling (CDS) of the output stage ensures slow readout noise. Higher frame rate requirements and integration of on-chip logic and analog-to-digital conversion (ADC) have pushed the machine vision market to CMOS image sensors (CIS). The implementation of global shutter pixels in CIS was limited by read noise and parasitic light sensitivity of the in-pixel storage node(s). Recently, progress has been reported on global shutter pixels in CMOS. Two strategies are followed. Both reduce the read noise through correlated double sampling. A first set of global shutter pixels have been developed with in-pixel charge domain storage and multiple charge transfers [1–3]. The charge domain storage in combination with CDS offers the lowest readout noise, but the shutter parasitic light sensitivity is limited. A second type of pixels have been developed with in-pixel voltage sampling of the pixel reset and signal levels, offering good noise performance in combination with good shutter efficiency [4–6].

In this paper, we will describe the operation and architecture of global shutter pixels with in-pixel voltage sampling. The read noise of the pixel will be modeled in detail and validated against characterization results on developed image sensors. The saturation level of the pixels is analyzed and parasitic light sensitivity is discussed. An overview of various devices that have been developed with these pixels is given. The results obtained are then compared against pixels with in-pixel charge sampling and some conclusions are made.

2 Global shutter pixel with correlated double sampling and in-pixel voltage sampling

2.1 Pixel architecture

The schematic of a global shutter pixel with CDS and in-pixel voltage sampling is shown in Figure 1. It counts eight transistors and two capacitors, hence we will refer to it as the ‘8T pixel’. Charges are collected on a pinned photodiode. At the end of exposure time, these charges are transferred to a floating diffusion FD. The floating diffusion can be reset through a reset transistor controlled by a reset signal RST. The signal of the floating diffusion is buffered by a source follower SF1, with its current load PC. The switches S1 and S2, and the storage capacitors C1 and C2 are used to sample the signal and reset levels of the floating diffusion. C2 samples the reset level before charge transfer and C1 samples the signal level. For best noise performance, as will be shown in this article, C1 and C2 are of

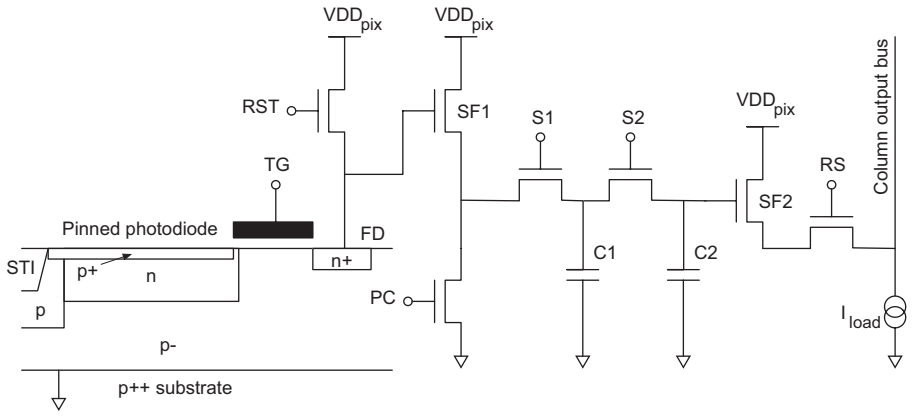

Figure 1 Schematic of an 8T global shutter pixel.

equal size. Source follower SF2 buffers the sampled signal levels for readout using the column bus. The row selection transistor, controlled by a row select line RS, selects the pixel for readout. A pulsed or permanent current source is connected to the column bus to load the source followers SF2 of all pixels.

Figure 2 shows the timing of the pixel and Figure 3 shows the potential profiles of the pinned diode and transfer gate at the start of the exposure, integration and readout. The exposure starts with a fully depleted photodiode. During integration time, photocharges are collected on the photodiode. Floating diffusion is typically kept in reset during exposure. At the end of exposure time, the floating diffusion reset line drops, and the FD reset level is sampled on C2 using switches S1 and S2. Then the charge is transferred to the floating diffusion, and the signal is sampled on C1 using switch S1. These actions happen synchronously in all pixels of the image sensor. The charges stored on the in-pixel capacitors after the signal sampling are:

$$Q2=C2\cdot V_{reset} \tag{1}$$

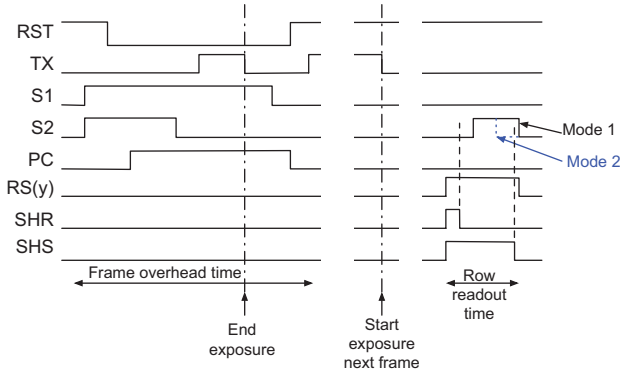

Figure 2 Timing diagram of the 8T global shutter pixel during frame capture and readout.

$$Q1=C1\cdot V_{signal} \tag{2}$$

The pixel array is read out row-by-row by pulsing the RS(y) line on row y. This switches on the row selection transistor. The reset level, which was sampled on C2, is put on the column output bus and is sampled in the column amplifier as $V_a=V_{reset}$ by the SHR pulse. Then switch S2 is closed and the charge of C1 and C2 is added together on the combined capacitance C1+C2. The resulting signal sampled into the column amplifier by the SHS pulse is:

$$V_b=\frac{Q1+Q2}{C1+C2}=\frac{C1\times V_{signal}+C2\times V_{reset}}{C1+C2} \tag{3}$$

The CDS subtraction circuit in the readout chain calculates V_b-V_a:

$$\Delta V=V_b-V_a=\frac{C1}{C1+C2}\left(V_{signal}-V_{reset}\right) \tag{4}$$

The subtraction cancels any common temporal and fixed pattern noise sources on the reset and signal levels. This includes the kTC noise of the floating diffusion, and low frequency noise sources, supply ripple or interferences.

For switch S2 there are two operational options. To start this analysis, we assume that S2 remains closed during row sampling (mode 1). We will analyze later what happens when S2 is opened again before the sampling of the signal level in the column amplifier (shown as mode 2 as indicated in Figure 2).

2.2 Temporal noise analysis

Several noise sources in the pixel can be identified:

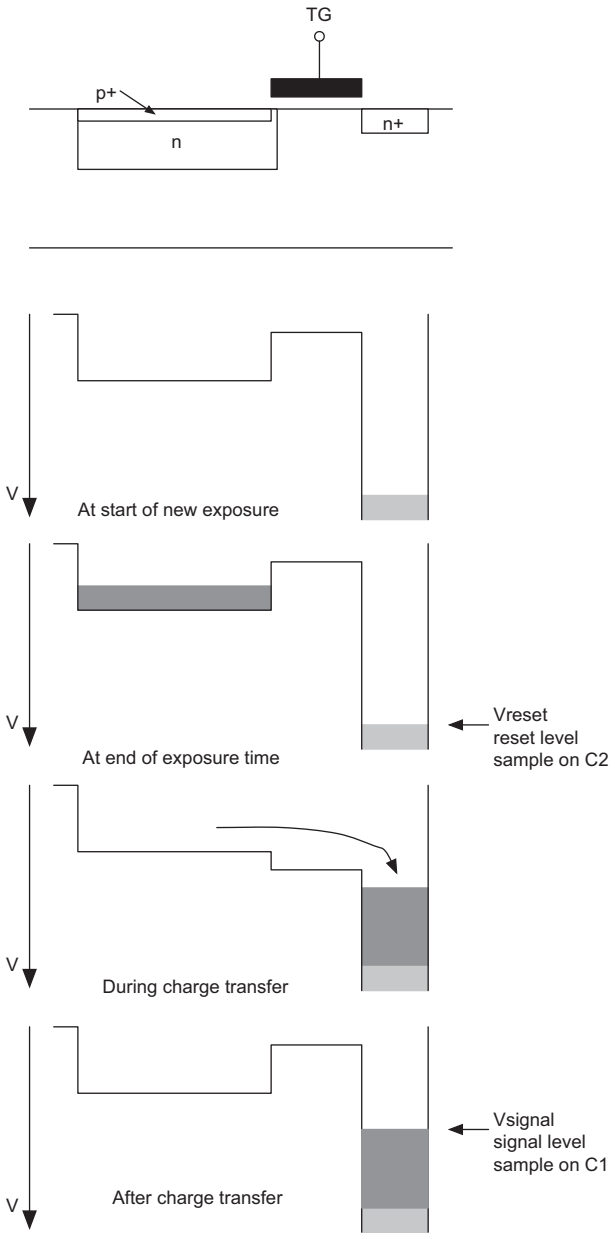

Figure 3 Potential profiles of the 8T global shutter pixel during its various operating modes.

- photon shot noise and dark current shot noise,
- thermal noise, including kTC noise,
- flicker noise.

Photon shot noise is unavoidable and caused by the quantized nature of the photons and the electron charge. Its magnitude equals the square root of the mean number of the generated electrons. It is not present for dark conditions. Dark current shot noise is the shot noise on the charges generated by dark current. It can contribute at moderate exposure times and higher temperatures. For example, a realistic dark current of 1000 e-/s at 45°C creates a signal of 10 e- and a shot noise of 3.3 e- RMS. The shot noise and dark current shot noise are not further considered in this article. The pixel read noise which is present under all exposure and temperature conditions is further studied in detail, because this shows the lowest noise limit that can be met by the pixel.

Figure 4 shows the noise model for the 8T global shutter pixel. The random motion of the electrons inside the transistors generates thermal noise in the two source followers SF1 and SF2 of the pixel. The thermal noise also results in kTC noise on the floating diffusion and the C1 and C2 sample capacitors. We can consider the following noise sources:

- kTC noise integrated on the floating diffusion:

$$\overline{v_{kTC,FD}^2}=\frac{kT}{C_{fd}} \tag{5}$$

- kTC noise integrated on sample capacitors C1 and C2:

$$\overline{v_{kTC,C1}^2}=\frac{kT}{C1} \tag{6}$$

$$\overline{v_{kTC,C2}^2}=\frac{kT}{C2} \tag{7}$$

- Input-referred noise power spectral density (PSD) of the thermal and 1/f noise on source follower 1, active during the global shutter pixel sampling [7]:

$$S_{sf1}=\frac{8}{3}\frac{kT}{g_{m,sf1}}\left(1+\frac{g_{m,pc}}{g_{m,sf1}}\right)+\left\{N_{f,sf1}+\left(\frac{g_{m,pc}}{g_{m,sf1}}\right)^2 N_{f,pc}\right\}\frac{1}{f} \tag{8}$$

- Input-referred noise PSD on source follower 2, active during readout:

$$S_{sf2}=\frac{8}{3}\frac{kT}{g_{m,sf2}}\left(1+\frac{g_{m,col}}{g_{m,sf2}}\right)+\left\{N_{f,sf2}+\left(\frac{g_{m,col}}{g_{m,sf2}}\right)^2 N_{f,col}\right\}\frac{1}{f} \tag{9}$$

where $g_{m,sf1}$, $g_{m,sf2}$, $g_{m,pc}$ and $g_{m,col}$ are the transconductance of the source followers SF1 and SF2, the in-pixel current source PC and the column load current source, respectively. $N_{f,sf1}$, $N_{f,sf2}$, $N_{f,pc}$ and $N_{f,col}$ are the respective flicker noise parameters for these transistors.

The noise contribution of the second source follower SF2 can be reduced by appropriate design measures. The load current can be set high enough to increase $g_{m,sf2}$ and the bandwidth of the source follower is limited by the capacitive load of the column line. If required, additional column line capacitance can be added to further limit the bandwidth and improve noise performance. Realistic

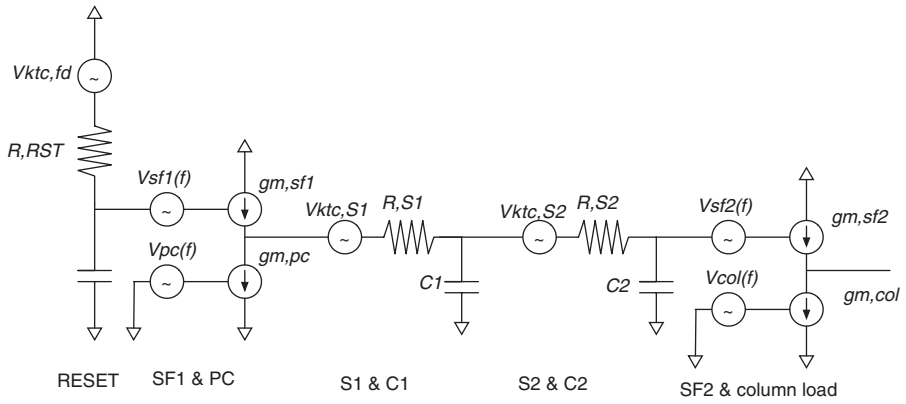

Figure 4 Noise model of the 8T pixel.

values are I_{load}=5 µA, $g_{m,sf2}$=94 µS and C_{load}=4 pF. Assuming that $g_{m,col}$=$g_{m,sf2}$, then the resulting integrated input referred white thermal noise on SF2 is 38 µV RMS. This is significantly smaller than the kTC noise contributions of C1 and C2. We will ignore the thermal noise contribution of SF2 in the further analysis. We will also assume an ideal gain of 1 for the second source follower to simplify the analysis. SF1 will not be ignored; its impact will be analyzed below.

After the sampling process of the global shutter, the resulting noise on capacitor C2 is:

$$\overline{v_{C2}^2}=\frac{kT}{C2}+\frac{kT}{C_{fd}}+\int_0^\infty S_{sf1}\left|H(f)\right|^2 df \tag{10}$$

and on C1:

$$\overline{v_{C1}^2}=\frac{kT}{C1}+\frac{kT}{C_{fd}}+\int_0^\infty S_{sf1}\left|H'(f)\right|^2 df \tag{11}$$

where $H(f)$ and $H'(f)$ are the transfer functions of source follower SF1 during the sampling process. They are slightly different due to the change of load capacitance. During row readout, the correlated double sampling calculates the difference according to Eq. (4). The following noise level is achieved after CDS:

$$\overline{\Delta v_n^2}=\left\{\frac{C1}{C1+C2}\right\}^2\left(\overline{v_{C1}^2}+\overline{v_{C2}^2}-\overline{2v_{C1}v_{C2}}\right) \tag{12}$$

The product in the last term of Eq. (12) shows the correlated noise component between the samples on C1 and C2. This is the kTC noise on the floating diffusion capacitance as given by Eq. (5). Eq. (12) can then be rewritten as:

$$\overline{\Delta v_n^2}=\left\{\frac{C1}{C1+C2}\right\}^2\left(\frac{kT}{C1}+\frac{kT}{C2}+\int_0^\infty S_{sf1}\left|H(f)\right|^2+\int_0^\infty S_{sf1}\left|H'(f)\right|^2\right) \tag{13}$$

Without source follower noise, this simplifies to:

$$\overline{\Delta v_{n,mode1}^2}=\frac{C1}{C1+C2}\cdot\frac{kT}{C2} \tag{14}$$

When $C1=C2=C$, this leads to the simple equation $\overline{\Delta v_n^2}=kT/2C$. With 16 fF sample capacitors, this is 359 µV RMS. The effect of the source follower noise is taken into account later again. But first the timing of the S2 switch is considered. In the above equations, it is assumed that the switch S2 is kept closed during readout of the second pixel sample in the CDS process, which yields signal V_b of Eq. (3). This is most beneficial for noise reasons, as opening the switch again would add an additional uncorrelated kTC noise to the sample on C2. However, there is an imbalance in charge injection and gate source capacitive coupling between the samples V_a and V_b. V_a is taken with S2 low, and V_b is taken with S2 high. A variation in capacitive coupling or charge injection between different pixels results in an increased pixel-to-pixel offset variation after CDS. This appears as fixed pattern noise (FPN). To avoid this FPN increase, the S2 switch can be opened again before sampling. As said, this increases the noise by an uncorrelated kT/C term. The noise contribution is derived, referring to Figure 5. When S2 is opened, the charge present on the capacitors C1+C2 is split over C1 and C2. Owing to charge conservation, the noise charge on each of the capacitors must be equal.

$$q_{n,c1}=-q_{n,c2} \tag{15}$$

There is only one degree of freedom in the system of Figure 5A. The thermal energy is then kT/2. We can apply the equipartition theorem:

$$\frac{1}{2}\left\{\frac{q_{n,c1}^2}{C1}+\frac{q_{n,c2}^2}{C2}\right\}=\frac{kT}{2} \tag{16}$$

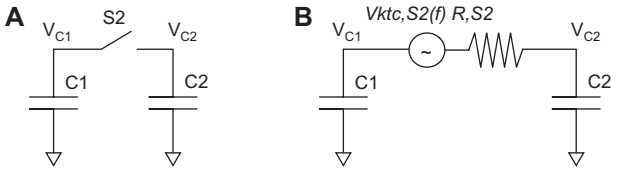

Figure 5 (A) Charge splitting over C1 and C2; (B) noise model for the charge splitting operation.

from which we can derive that:

$$q_{n,c1}^2 = q_{n,c2}^2 = kT\frac{C1 \cdot C2}{C1+C2} \tag{17}$$

and therefore the voltage noise on C2 when S2 is opened is given by:

$$v_{C2}^2 = \frac{q_{n,C2}^2}{C2^2} = \frac{C1}{C1+C2} \cdot \frac{kT}{C2} \tag{18}$$

This result can also be derived from the equivalent noise model in Figure 5B. This term is not attenuated by the capacitive redistribution. The resulting noise after CDS in this mode is then given by:

$$\overline{\Delta v_{n,mode2}^2} = \left\{ \left(\frac{C1}{C1+C2} \right)^2 \left(\frac{kT}{C1} + \frac{kT}{C2} + \int_0^\infty S_{sf1} |H(f)|^2 + \int_0^\infty S_{sf1} |H'(f)|^2 \right) \right\} + \frac{C1}{C1+C2} \frac{kT}{C2} \tag{19}$$

When the thermal noise is ignored the equation can be written as:

$$\overline{\Delta v_{n,mode2}^2} = \frac{2C1}{C1+C2} \cdot \frac{kT}{C2} \tag{20}$$

When $C1=C2=C$, this further simplifies to $\overline{\Delta v_n^2} = kT/C$. With 16 fF sample capacitors, this results in 509 µV RMS read noise.

It is clear that in both modes, the kTC noise is considerably higher than the thermal noise of the second source follower SF2. For the first source follower SF1, this is now analyzed. The first source follower operates during the global shutter timing, synchronously in all pixels. The bias current provided by the PC transistor flows concurrently in all pixels. This means that the current must be limited, to avoid further peak current. A suitable bias current is 1 µA or lower. This means that SF1 can operate in weak inversion or close to weak inversion mode. Assuming I_{pc}=1 µA, $g_{m,sf}$= 2 µS and $g_{m,pc}$=20 µS, then the integrated thermal noise of SF1 is 458 µV RMS, referred to the output of SF1. This is similar to the kTC noise levels. The temporal white noise of the first source follower cannot be ignored.

The flicker noise component should be considered in combination with the CDS sampling process. Flicker noise on SF1 relates to the global shutter sampling process. Typical global shutter sampling interval times between the sampling of the floating diffusion reset and signal levels are approximately 10 µS. This time period is determined by the duration of the peak currents occurring during the global shutter sampling and by the settling times on the various control and supply lines. The latter form large RC networks across pixel array. Flicker noise on SF2 relates to the CDS sampling process. The typical sampling interval between both samples is <1 µS. For these short sampling periods, the flicker noise can be ignored. For further reading on the effects of flicker noise and the influence of CDS on it, we refer to [5].

To convert the noise back to electrons, the floating diffusion capacitance and the attenuation by the charge sharing and the source followers must be taken into account. The conversion gain, after the CDS subtraction at the pixel output is given by:

$$CG\left[\frac{\mu V}{e^-}\right] = \frac{q_{el}}{C_{fd}} \cdot G_{sf1} \cdot \frac{C1}{C1+C2} \cdot G_{sf2} \tag{21}$$

where q_{el} is the elementary charge and G_{sf1} and G_{sf2} are the gains of the source followers SF1 and SF2, respectively. For SF2, we have assumed that its gain is unity in the above noise analysis. It can also be considered as if Eqs. (13) and (19) are referred to the input of this second source follower.

Table 1 shows calculated noise values from the above pixel noise model, for pixel parameters implemented in 5.5 µm global shutter pixels, developed in a 0.18 µm CMOS image sensor process. The calculated noise values fit well to the actual measured values. The read noise of the image sensor is clearly dominated by pixel noise. Fixed pattern noise is also measured. In mode 1, the fixed patter noise is approximately 30% higher than in mode 2, due to mismatch of gate source coupling of the S2 switches between different pixels. A camera with external fixed pattern noise correction can benefit from the lower noise in mode 2 to further improve image quality.

Figure 6 shows the temporal read noise of a pixel, expressed in e- RMS, as a function of the relative size of the storage capacitances C1 and C2. The total area in the pixel available for the capacitors is constrained by the pixel pitch. Usually, C1 and C2 are NMOS gate capacitors, biased in inversion. For a 5.5 µm pixel in 0.18 µm CMOS, the capacitive density is approximately 5 fF/µm² for an NMOS 3.3 V inversion capacitor. The total capacitance of C1 and C2 together is then approximately 32 fF. This value

Table 1 Noise values calculated for an 8T 5.5 µm global shutter pixel developed in a 0.18 µm CIS process, and measured values.

Parameter	Symbol	Value	Unit
Floating diffusion capacitance	C_{fd}	1.4	fF
In-pixel sample capacitances	$C1$	16	fF
	$C2$	16	fF
Transconductance first source follower (SF)	$g_{m,sf1}$	32	µS
Transconductance, load of first SF	$g_{m,pc}$	20	µS
Gain of source follower SF1	$gain_{sf1}$	0.83	
Source follower SF1 thermal white noise, referred to SF1 output	$V_{n,sf1}$	457	µV RMS
C1/C2 kTC noise (1×kT/C)	$\sqrt{kT/C}$	508	µV RMS
Conversion gain (at output of pixel, assuming gain of 1 for SF2)	CG	47	µV/e-
Temporal noise after CDS, mode 1	$\Delta v_{n,\ mode\ 1}$	483	µV RMS
model Eq. (13) (S2 on during read)	$\Delta v_{n,\ mode\ 1}$	10.1	e- RMS
Temporal noise, mode 1, measured	$\Delta v_{n,\ mode\ 1}$	10	e- RMS
Fixed pattern noise, mode 1, measured		17	e- RMS
Temporal noise after CDS, mode 2	$\Delta v_{n,\ mode\ 2}$	602	µV RMS
model Eq. (19) (S2 off during read)	$\Delta v_{n,\ mode\ 2}$	12.6	e- RMS
Temporal noise, mode 2, measured	$\Delta v_{n,\ mode\ 2}$	13	e- RMS
Fixed pattern noise, mode 2, measured		13	e- RMS

was taken as a constraint in Figure 6 and the values of C1 and C2 are swept within this constraint. Other parameters are identical to the ones used in Table 1. The figure clearly shows that the lowest read noise is achieved when C1=C2, for both noise models.

Figure 7 shows the total read noise as a function of the capacitance C. C1 and C2 are equal now. It can be seen that the noise drops only moderately once the capacitors

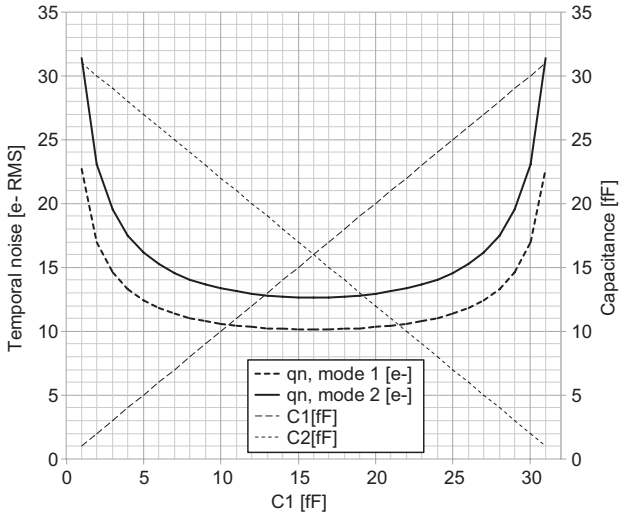

Figure 6 Temporal read noise of an 8T pixel as a function of C1 and C2, with a total capacitance of 32 fF.

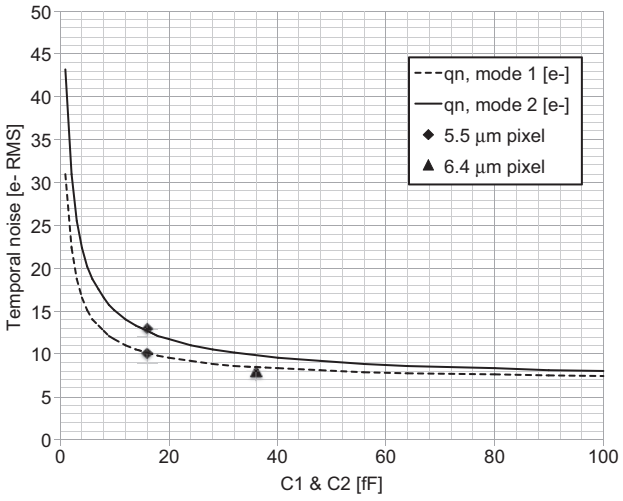

Figure 7 Temporal read noise of an 8T pixel as a function of capacitor size. C1=C2=C.

extend above 40 fF. The difference between both operating modes reduces also, because of the dominance of the source follower noise. Data from two products, using 5.5 and 6.4 µm pixels, are also shown (with data for both modes for the 5.5 µm pixel). The 6.4 µm pixel slightly performs better than predicted through the model, but this pixel has approximately 10% higher conversion gain, which explains its lower read noise, and which is not taken into account in the curve.

2.3 Saturation and anti-blooming performance

For dynamic range, next to read noise, the saturation level is also important. A pixel saturates when one of these three conditions is reached:

1. When the photodiode has reached the maximum amount of charges that it can store.
2. When the swing on the floating diffusion limits the full charge transfer.
3. When the readout clips the signal (e.g., saturation of the pre-amplifiers or the ADC).

Each of the conditions can have different behavior with overexposure. In fact, these limits are not specific to the global shutter pixel as discussed here, but they also occur for 4T pixels and charge domain global shutter pixels with a separate overflow drain. We will analyze the dependencies of full well charge below, and start with the condition where the photodiode storage determines the saturation level.

At the start of exposure, the photodiode is fully depleted. There is no charge left on the photodiode. This is a clearly defined starting point, with no uncertainty, and this is the reason why low noise levels can be reached with pinned diodes. At saturation of the photodiode, the extra photocharges have to be drained away. There are two possibilities. Excess photocharges can diffuse to neighboring non-saturated pixels and be collected there. These neighboring pixels will then also quickly saturate. This causes so-called blooming or charge overspill. This is not desired and can be avoided in CMOS pixels by appropriate pixel biasing. The excess photocharges can be drained away via the transfer gate to the floating diffusion and the reset transistor. Figure 8 shows this flow of excess photocurrent in a saturated pixel. Although not specifically required, we usually hold the floating diffusion in reset state by closing the reset switch during exposure. When saturated, the excess photodiode current flows through the transfer gate. This transistor operates in weak inversion, with the following relation:

$$I_{pd} = I_{D0} \frac{W}{L} \exp\left(\frac{V_{gs}}{n kT/q}\right) \tag{22}$$

where V_{gs} is the drain gate voltage of the transfer gate, n is the subthreshold slope factor and W and L are the transfer gate width and length. I_{D0} is the subthreshold leakage current. V_{gs} is the difference between the transfer gate voltage in off-state $V_{tx,low}$ and the saturation voltage $V_{pd,sat}$ on the photodiode. Eq. (22) can be rewritten as:

$$V_{pd,sat} = V_{tx,low} - \frac{nkT}{q} \ln\left(\frac{I_{pd}}{I_{D0} W/L}\right) \tag{23}$$

From this equation, it is clear that the saturation level of the pinned photodiode depends logarithmically on the photocurrent I_{pd}, and hence on the light level. Under stronger light conditions, the photodiode can reach a more negative voltage. The photodiode has a larger full well charge under strong light conditions. $V_{tx,low}$ is often, but certainly not always, equal to 0 V. We can use this voltage to tune the saturation level of the photodiode. This voltage level is also used in some cases to put the transfer gate in accumulation because that reduces dark current. However, one must take care that excess photocharges are evacuated through the transfer gate. If the photodiode becomes forward biased, it will not collect any more charges and blooming will occur. This means that strong negative levels on the transfer gate must be avoided, unless another anti-blooming mechanism is foreseen. The logarithmic dependency of the light level means that the swing on the photodiode increases with approximately 58 mV per decade of light (assuming 300 K and n=1). This corresponds to an amount of electrons per decade of light, depending on the capacitance of the photodiode near saturation conditions. In Figure 9, the relation between full well charge and relative light level is shown for a 10 µm four-transistor pixel. The full well increases by 13 090 e- per decade of light for this pixel.

The full well charge of the photodiode is the integrated charge on the photodiode between the voltage level V_{pin} at which the photodiode is fully depleted, and the saturation level of the photodiode.

$$q_{pd,sat} = \int_{V_{pd,sat}}^{V_{pin}} C(v)dv \tag{24}$$

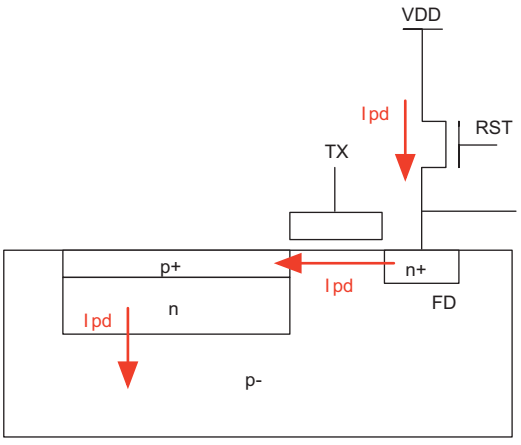

Figure 8 Flow of excess photocurrent during overexposure in an 8T pixel.

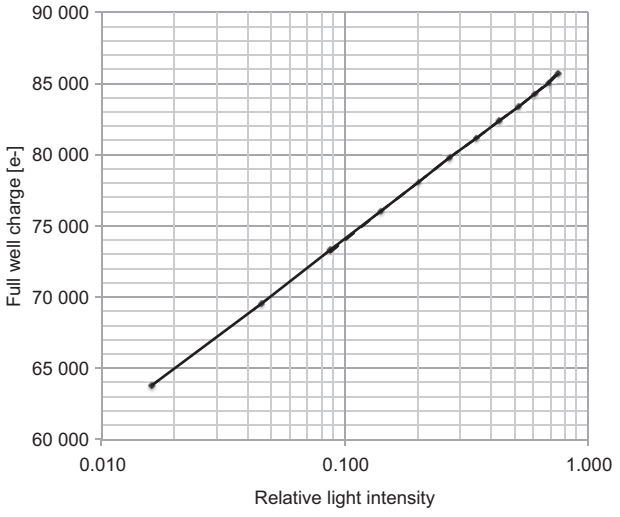

Figure 9 Relation between full well charge and relative light level is shown for a 10 µm four-transistor pixel.

The full well charge can be increased by:

- Increased V_{pin}. This is constrained by the swing on the floating diffusion. After charge transfer, the voltage on the floating diffusion should stay above V_{pin}. A higher V_{pin} makes it more difficult to maintain this.
- Increased photodiode capacitance. Shallower junctions with stronger electric fields help but may increase dark current, and can make the charge transfer more difficult.
- A lower voltage of the transfer gate, possibly as long as anti-blooming is provided.
- A higher threshold voltage on the TX gate (which reduces I_{D0}). This has a similar effect as a lower TX gate voltage.
- The dimensions of the transfer gate (W and L).
- Lower (absolute) temperature.
- A higher light level.

In some cases other effects can also influence the full well charge. A leakage current dependency on drain voltage has been observed in certain pixel designs and technologies. Such effects are usually avoided by design of the transfer gate device.

In the case when the saturation level is clipped by the pixel readout before CDS, or by the floating diffusion swing itself, an opposite sensitivity of the saturation level to light level can be observed in some cases. The reset level of the floating diffusion depends on the reset transistor. We refer again to Figure 8 to indicate that the excess photocurrent flows through the reset transistor during the reset of the floating diffusion. Two conditions can now occur, which are somewhat similar to the 'hard' and 'soft' reset schemes considered in three-transistor active pixels [8]:

- the high level of the reset gate is higher than its drain (pixel power supply) and its threshold voltage. The reset transistor acts as a switch which resets the floating diffusion to:

$$V_{res,fd}=VDD_{pix}-\Delta V_{Cgs,res} \tag{25}$$

  where $\Delta V_{Cgs,res}$ represents the amount of capacitive coupling between the reset gate and the floating diffusion. The reset level is independent of photocurrent or other variable parameters.
- The high level of the reset gate is lower. The reset transistor acts as a source follower in subthreshold regime. The floating diffusion reset level depends on the reset gate high voltage $V_{res,h}$ and the photocurrent I_{pd} (which flows through the reset transistor during the floating diffusion reset for a saturated pixel). The reset level of the floating diffusion is given by:

$$V_{res,fd}=V_{res,h}-\frac{nkT}{q}In\left(\frac{I_{pd}}{\frac{I_{D0}W}{L}}\right)-\Delta V_{Cgs,res} \tag{26}$$

  where n, I_{D0}, W and L are the subthreshold slope factor, the subthreshold leakage current and the width and length of the reset transistor, respectively. The reset level drops logarithmically with increased photocurrent.
  If the signal is clipped with this condition at a fixed level before CDS, on the floating diffusion or in the readout path, then the signal swing drops logarithmically with the light level. This behavior is opposite to the situation of a photodiode limited saturation level discussed in the previous paragraph. This dependency of the saturation level on light level can be avoided by clipping the signal after CDS.

It depends on the pixel design and its bias conditions which mechanism determines the saturation level. In the 5.5 µm pixels discussed previously, the full well charge is limited by the photodiode to 13 500 e-.

The useable full well charge may be limited by linearity constraints. The pixel response near saturation becomes less linear due to several effects:

1. non-linearity of the floating diffusion capacitance, in particular the reverse-biased junction capacitance;
2. non-linearity of the source followers in the pixel, imposed by the body effect on these transistors.

Linearity of the sense node was a concern in the past with three-transistor active pixels, because these were operated until relatively low reverse bias voltages. With pinned photodiode pixels, the floating diffusion sense node is operated at a reverse bias of at least 1 V, the junction capacitance is more linear in that range. The non-linearity of the source follower depends on the actual signal range used and the transistor parameters. For the 5.5 µm pixel mentioned above, the curve deviates 10% from the linear fit at a photocharge of approximately 10 800 e-, and 2% for a photocharge of 9300 e-.

2.4 Parasitic light sensitivity

Parasitic light sensitivity is the sensitivity of the pixel at the moment that the electronic shutter is supposed to be off (optically 'closed', not light sensitive). It can be measured by halting the readout after exposure, and measure the increase in signal with longer halt time. In these 8T global shutter pixels, the parasitic light sensitivity is very low. There are three reasons for this:

1. The capacitors C1 and C2 itself do not collect any charges, only the junctions of the switches S1 and S2 will do this.
2. When an electron is collected by the drain of the S1 or S2 switches, its impact on the signal is attenuated by the ratio of the capacitances of the floating diffusion and the storage capacitors C1 or C2 ($C_{fd}/C1$ or $C_{fd}/C2$). It is clear from Eq. (21) that the lowest read noise (in e-RMS) is achieved with the smallest floating diffusion capacitance. The typical design goal is to use the smallest possible floating diffusion capacitance, and the largest possible storage capacitors, in order to reach the lowest noise floor. This is also beneficial for a low parasitic light sensitivity.
3. There is an equal chance for the capacitors C1 and C2 to collect such parasitic photogenerated electron. The parasitic light signal appears as a common mode signal on the two samples taken from the pixel (V_a and V_b). After CDS, the effect is cancelled.

A parasitic light sensitivity of 1/100 000 has been measured on a frontside illuminated 4 MPixel CMV4000 [9]. The parasitic light sensitivity does not rely on light shielding and remains good also for backside illuminated devices. This was demonstrated on 2 and 4 MPixel image sensors [9] and a parasitic light sensitivity of 1/25 000 was measured. This is the only demonstration of global shutter backside illuminated CMOS image sensors so far.

2.5 Characterization results

A variety of sensors have been designed with these 8T global shutter pixels. Table 2 gives an overview of the key specifications of the devices. All are developed in 0.18 µm CIS technology with two different foundries. The noise model presented in this article fits well to the measurements on these devices.

3 Global shutter pixels with correlated double sampling and in-pixel charge storage

Figure 10 shows a schematic of a global shutter pixel with in-pixel charge storage in an embedded CCD. The photodiode and CCD are shown in cross-section. The pixel contains a pinned photodiode, a three-phase embedded CCD channel, and a charge-to-voltage conversion stage similar to typical 4T pixels. A horizontal anti-blooming gate is foreseen to evacuate excess charges at overexposure conditions, and to determine the start of the exposure time. After exposure, the photocharges are moved synchronously in all pixels from the photodiode to the center CCD phase ø2 by pulsing ø1 and ø2. It stays there until the pixel is read out. Readout happens through a reset of the floating diffusion, sampling of the reset level as the reference

Table 2 Key specifications of devices developed at CMOSIS in 0.18 µm CIS processes with 8T global shutter pixels.

Device	CMV300	CMV2000	CMV4000	CMV12000	CMV20000	Unit
Parameter						
Pixel count	0.3	2.2	4	12	20	MPixel
Resolution	648×488	2048×1088	2048×2048	4096×3072	5120×3840	Pixels
Pixel pitch	7.4	5.5	5.5	5.5	6.4	µm
Full well charge	20 000	13 500	13 500	14 500	15 000	e-
Read noise	12	13 (10)	13 (10)	13 (10)	8	e- RMS
Dynamic range	64	60	60	61	65	dB
Parasitic light sensitivity	<1/50 000	<1/50 000	<1/50 000	<1/50 000	<1/60 000	
Quantum efficiency[a]	55	60	60	55	45	%
Dark current at 20°C	100	125	125	125	125	e-/s
FPN	<20	<13	<13	<13	<30	e- RMS
PRNU[a]	1	1	1	1.3	1	% RMS
Frame rate	300 (600)	340	180	150 (300)	30	fps
ADC resolution	12	10/12	10/12	8/10/12	12	Bits
Power	300	600	600	3500	1100	mW
Optical format (pixel array diagonal)	1/3″ (6 mm)	2/3″ (11 mm)	1″ (16 mm)	APS (28 mm)	35 mm (43 mm)	
Package	64 BGA (CSP)	95 µPGA	95 µPGA	237 µPGA	143 PGA	

[a]Monochrome, microlens, 550 nm. PRNU, Photo response non-uniformity.

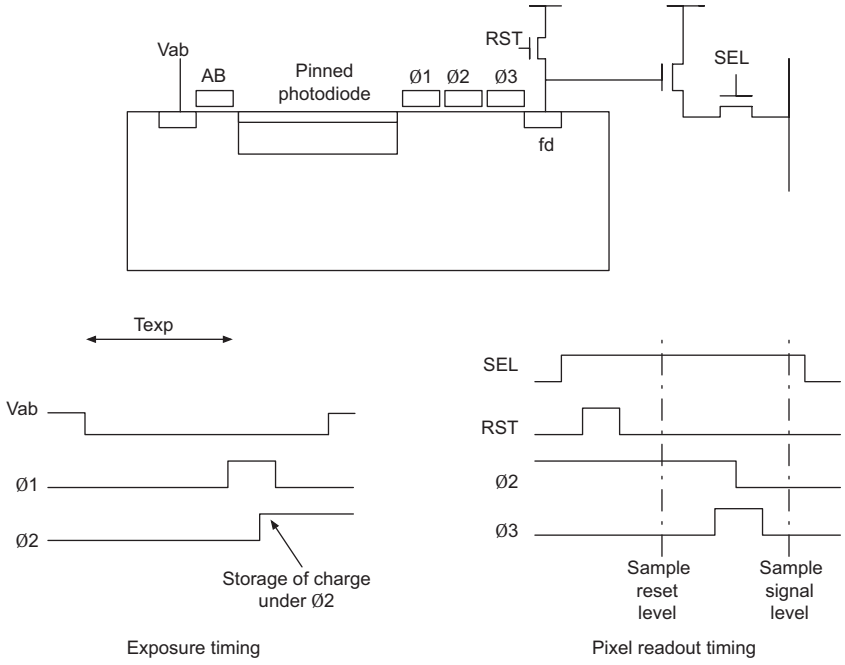

Figure 10 Global shutter pixel with in-pixel charge storage.

for correlated double sampling (or CDS), transfer of the charge from the center gate to the floating diffusion by pulsing ø3 and ø2, and sampling of the signal level.

This principle was reported by several teams. In [1] a read noise of 10 e- was reported on an 8×8 μm pixel in 0.18 μm CMOS. The pixel had a rather large shutter leakage of 2.3%, which corresponds to a parasitic light sensitivity of 1/43. In [2], the principle was further refined. The ø2 gate was replaced by a pinned diode with a higher depletion voltage than the photodiode. This pinned diode forms a virtual phase for ø2. The drawback is that the potential on that storage node cannot be changed, in contrary to a real gate. A low read noise of 2.7 e- RMS is reported for high readout gain conditions. For unity gain the readout noise was 14.3 e- RMS. Full well is 10 000 e- (for a linearity of 1%). The reported shutter efficiency is 99.7%, corresponding with a parasitic light sensitivity of 1/333. Finally, a 5.86×5.86 μm^2 pixel with two transfer gates made in 90 nm CMOS was reported [3]. The gate adjacent to the pinned diode contains a transfer gate with a potential well at the side opposite to the photodiode. This creates a storage node, which can be read out with the second gate. A read noise of 4.8 e- RMS is reported, at +16 dB gain, and a saturation signal of 32 000 e- (in single storage mode). The reported dynamic range of 76.5 dB cannot be reproduced in one scene, as the noise at unity gain is not reported and will likely be higher. The reported shutter efficiency is excellent, 100 dB, or 1/100 000. A dedicated light shield layer close to the silicon surface is implemented, but no further details are given on how this good shutter efficiency is achieved. A high dynamic range mode with a dual storage scheme, storing bright signals on the floating diffusion is also reported.

4 Conclusion

The results of the 8T global shutter pixels are compared against other global shutter pixels with correlated double sampling in Table 3. The reported noise in charge domain global shutter pixels is lower owing to the noise-free storage of the charge packet inside the pixel. However, this advantage is only apparent when a high gain is used in the readout path. At unity gain, the reported noise levels are similar. Parasitic light sensitivity appears to be solved on the device reported in [3], but no details are given how, except the use of a low level light shield.

The noise model reported in this paper shows the contributions of the kTC and source follower thermal noise to the pixel read noise. The contribution of the in-pixel source follower that buffers the floating diffusion cannot be ignored. Care must be taken in the design of 8T pixels to ensure that this noise does not become dominant.

A further challenge for new smaller pixels is the scaling of the in-pixel capacitors. Currently, these are implemented as NMOS gate capacitors, with the gate biased in inversion. All transistors used inside the pixel

Table 3 Key specifications of reported global shutter pixels with CDS.

Reference	[1]	[2]	[3]	This work	Unit
Parameter					
Pixel pitch	8×8	7.5×7.5	5.86	5.5–7.4	µm
Full well charge (single storage, 2% lin.)	–	14 000	32 200	13 500–20 000	e-
Read noise (unity gain)	10	14.3	–	13–8	e- RMS
Read noise (at +18 dB gain)		2.7 (15× gain)	4.8 (8× gain)	–	e- RMS
Dynamic range	–	60	(76.5)	61–65 dB	dB
Parasitic light sensitivity	1/43	1/333	1/100 000	1/50 000–1/100 000	
Quantum efficiency	–		–	60–55	%
Dark current at 20°C	–	58 (est.[a])	–	125	e-/s
Technology node	180	180	90	180	nm

[a]119 e-/s at 27°C reported.

are thick oxide 3.3 V transistors. These remain available in more advanced CMOS nodes, but the gate thickness hence the capacitance per unit area remains constant. This makes it difficult to scale this pixel to smaller dimensions. One solution is the use of a dual gate oxide pixel. The storage gates and possibly some other low voltage devices in the pixel can use thin oxide devices. Some of the other pixel transistors, such as the reset transistor, transfer gate and first source follower, can use high voltage thick oxide devices. Care must be taken on the voltage levels on these gates, to avoid stressing the gate oxide.

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