Views

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ITRS lithography roadmap: status and challenges

Abstract: Recent ITRS lithography roadmaps show a big technology decision approaching the semiconductor industry about how to do leading edge lithography. The need is rapidly approaching for the industry to select an option for the 22-nm half pitch, but no decision has been made yet. The main options for the 22-nm half pitch are extreme ultraviolet (EUV), ArF immersion lithography with multiple patterning, and maskless lithography. For the 16-nm half pitch, directed self-assembly (DSA) is also an option. The EUV has the most industry investment and is the closest to current lithography in the way it works but still faces challenges in tool productivity and defect-free masks. The nanoimprint needs to overcome the defect, contamination, and overlay challenges before it can be applied to the semiconductor production. Maskless lithography may be used first for prototyping and small volume products where mask costs per chip produced would be very high. Double patterning could be extended to multiple pattering, but would give tremendous process complexity and exponentially rising mask costs due to the many exposures needed per level. The DSA, which only recently has emerged from the research stage, has the potential for very high resolution but represents a huge change in how critical dimensions are formed and controlled.

Keywords: lithography roadmap; photolithgraphy; semiconductor manufacturing.

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1 Introduction

The International Technology Roadmap for Semiconductors (ITRS) [1] has been published every 2 or 3 years for almost 20 years. In recent years, there have been new roadmaps every 2 years, with updates in the in-between years. The roadmap projects semiconductor technology progress for a 15-year period and includes sections on device properties, process technologies, such as lithography and metrology, process integration and interconnect, packaging, and many other areas. It is a global effort sponsored by the international semiconductor associations and put together by the leading semiconductor technology experts and representatives from companies in the semiconductor industry all over the world.

A key function of the ITRS roadmap is to enable equipment and materials suppliers to know future requirements and be able to develop new products in time to meet these requirements. Progress for the industry is defined as a series of technology nodes, with each node having the smallest printed dimension of about 70% of the previous node along with new process and device innovations. This provides better performing chips with a lower cost per transistor and is the key to the tremendous progress the semiconductor industry has shown over the past half century.

The roadmaps' technical pace typically shows companies meeting Moore's law [2], which seems like a fast pace. But experience has shown that the industry typically beats the roadmap rather than fall behind it, and this happens despite the fact that many of the technical targets in the roadmap look undoable. Sometimes, a technology is extended further than expected, or sometimes, new technologies are adopted that enable fast progress. There is always an uncertainty in how the industry will meet the roadmap, even while there is confidence that it will. In the lithography section, the roadmap team has dealt with this uncertainty by creating a chart showing the possible options for printing smaller critical dimension and necessary decision dates for selecting from among those options. The 2009 chart is shown in Figure 1.

The 45- and 32-nm nodes are using optical lithography to print critical dimensions. The lithography technology choice for the 22-nm node has not been decided yet, and the decision will have to be made by the end of 2012 to be in time for the manufacturing scale up. The choice for the 16-nm node also has not been made and will have to be decided by the end of 2015. Now, it is 2012, and one might have expected that these choices would have narrowed considerably compared to 2009. But looking at the

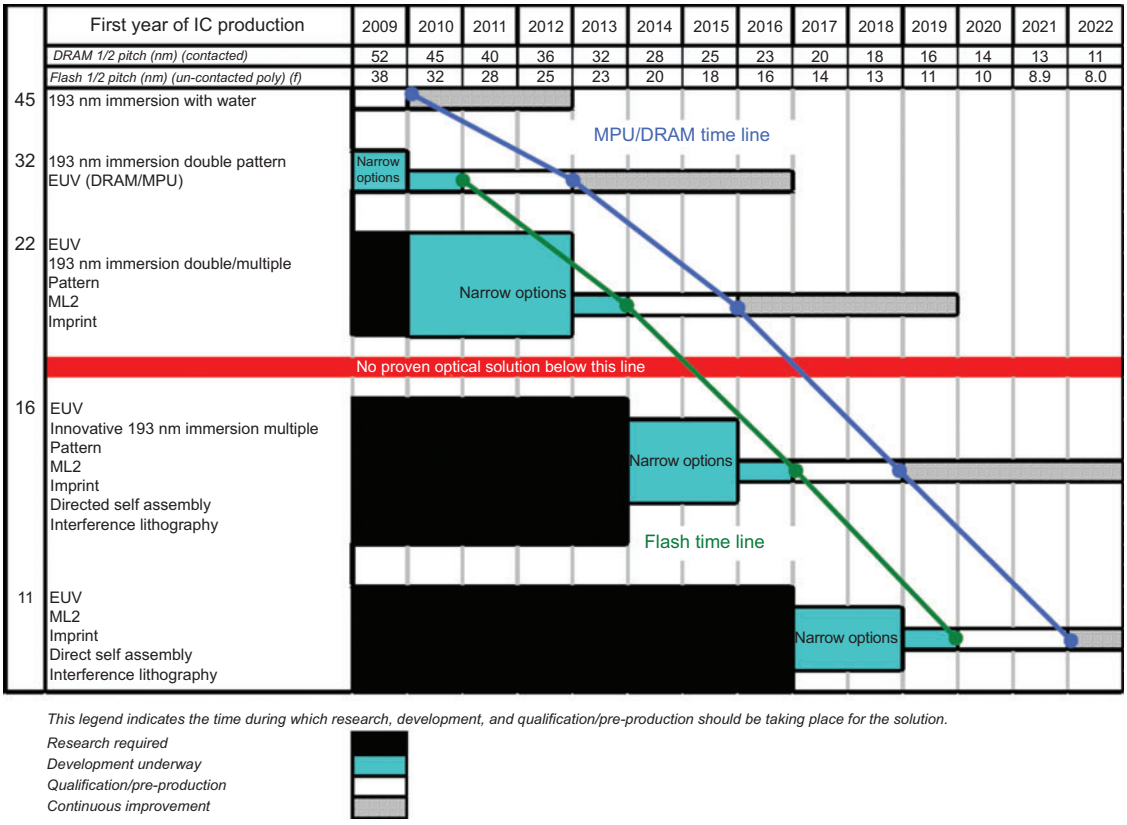

Figure 1 The 2009 ITRS lithography roadmap.

2011 roadmap shown in Figure 2A and 2B, it shows that this is not the case [3]. For the 22-nm flash memory, double patterning with optical lithography is the choice, but for the 22-nm half pitch DRAM memory and microprocessors (MPUs), no narrowing of options has occurred, even though the decision date is still at the end of 2012. For the 16-nm devices, almost all the choices are still there, and the decision date is still at the end of 2015. This lack of decisiveness does not reflect a slowing of the technical progress. Instead, it is a consequence of a real technical roadblock: how to overcome the resolution limits of optical lithography.

In the past decades, shrinking the size of the printed features has involved improvements in the resolution limits of the exposure tools along with the periodic shrinking of the optical wavelengths, starting with broadband illumination (a kind of blue light), moving to the G line (435 nm), I line (365 nm), KrF (248 nm), and Arf (193 nm). Of course, the exposure tools changed as the wavelength did, but they still used lenses to focus the light and also progressed by collecting more of the light diffracted by the reticle and enabling a higher resolution for a given wavelength. Light sources were arc lamps or lasers, both of which are well-understood readily available types of sources. After ArF was introduced, the industry started work on the next wavelength, 157 nm. But the development of immersion lithography for the 193 nm made the 157 nm unnecessary. The use of immersion gave more resolution improvement than moving to the 157 nm would have, but without the need of developing new glasses for the 157-nm lenses and fundamentally different resist polymers. Some work was done to assess the possibility of the 157-nm immersion, but suitable immersion fluids for the 157 nm were very difficult to find, and the work was abandoned. This means that there is no obvious optical wavelength to adopt that would enable a better resolution. Without a smaller wavelength available than 193 nm, the resolution of the projection optics is then limited to $0.25\,\lambda/\mathrm{NA}$, where the maximum NA is limited to the refractive index of the immersion fluid. For the ArF immersion, that fluid is water, with a refractive index of 1.44, and the smallest half pitch that could possibly be resolved is about 34 nm. The actual constraints of real tools and lithography processes mean that one can approach this number but not hit it exactly.

The roadmap's 32-nm half pitch node is already below this half pitch and is in production today using optical printing. How did the industry do this? It adopted 'double

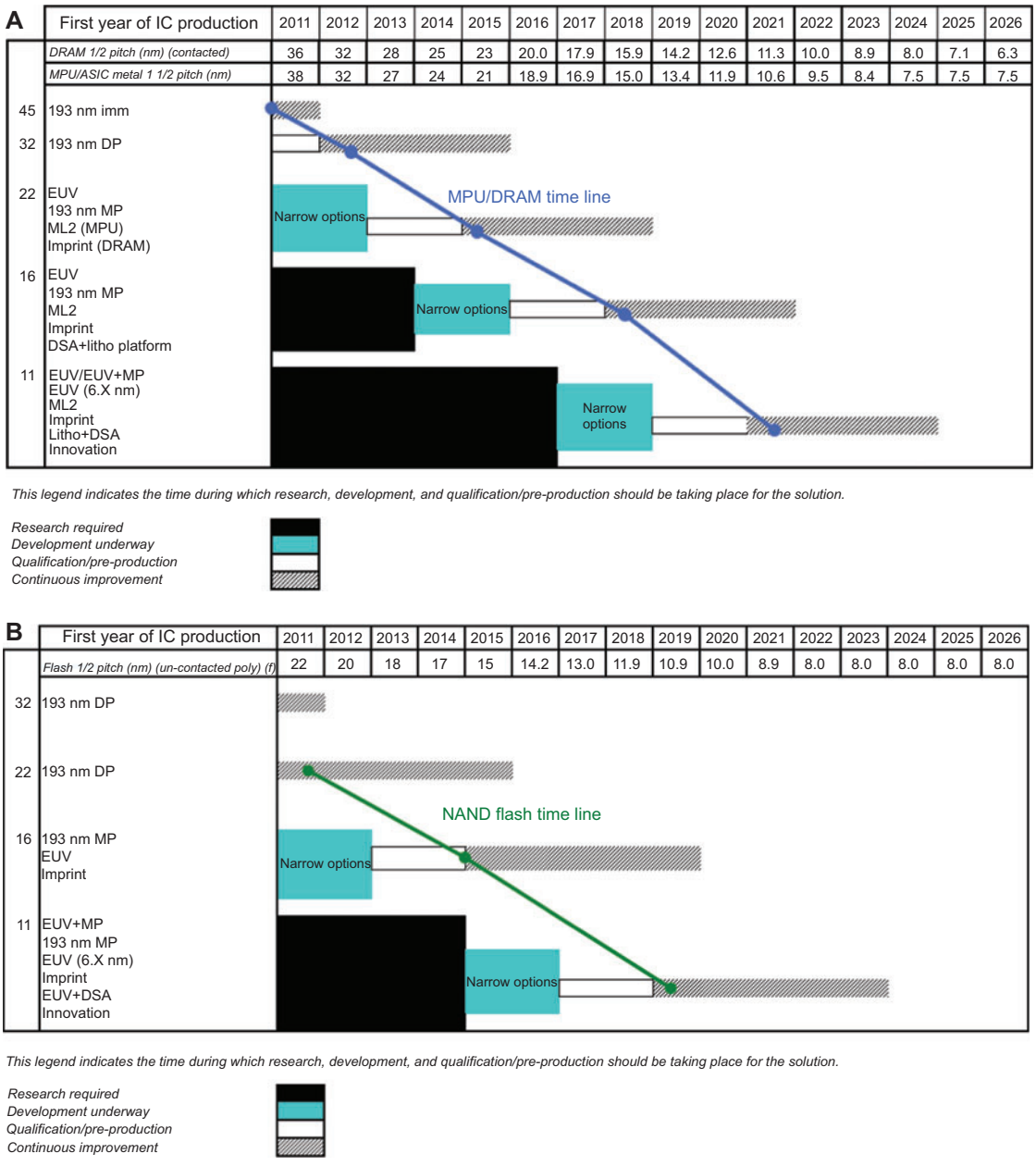

Figure 2 (A) The 2011 ITRS lithography roadmap for DRAM and MPU half pitch.
(B)The 2011 ITRS lithography roadmap for flash memory.

patterning', a set of process technologies that take a pattern printed at a larger pitch and double the density through multiple process steps or print features twice in order to get a higher density than can be obtained with one exposure. Such 'multiple patterning' requires many process steps and is quite expensive for a semiconductor producer, but it has enabled the industry to advance an entire process node (from 45 nm to 32 nm), without improving the fundamental resolution limit of exposure tools.

Future nodes could conceivably be done by extending double patterning to quadruple patterning (i.e., double double patterning), octuple patterning, and so on. But the nature of double patterning makes this difficult. Double patterning only doubles the pitch of long lines. It does not help cut the ends of the lines to make realistic features or to create associated features like small contacts or vias. Other exposure and processing steps are required to do these functions, which add considerably to the number of exposures that will be needed for each critical level. These ancillary exposures have their own difficulties and resolution limits too. For nontrivial patterns, such are found in DRAMs and in MPUs, so many exposure steps

and processing steps would be required that the industry is investing large resources to find novel ways to create smaller patterns than can be done with the ArF immersion lithography. These resources are being applied to the options shown in Figure 1.

2 Extreme ultraviolet lithography (EUVL)

EUVL is the leading candidate to enable patterning for the 22-nm half pitch and below. It is like optical lithography in that it is a projection lithography using a system of lenses to project the image of a mask on a photoresist film. However, the photons have a wavelength of 13.4 nm, which is 14 times smaller than that of the 193 nm and completely changes their interaction with matter. All reflective optics using multilayer mirrors in a vacuum and using reflective masks is necessary. There are no sufficiently powerful lasers available for this wavelength, and light sources with sufficient power for reasonable lithographic throughput are a new technology being developed to make the EUVL work. Currently, the EUV output of those plasma-based light sources is not yet sufficient to meet the manufacturing requirements. Addressing this productivity challenge, i.e., making the EUV light sources work reliably at the high-power levels required, has taken longer than expected. However, the industry is investing the resources required to address these challenges [4]. The first generation of production tools to be delivered in 2013 is likely to have bright-enough sources to support sufficient productivity for chip makers to phase in the EUV for some critical levels at the 22-nm half pitch node in the pilot production, and then to ramp-up to HVM at the 16-nm half pitch node.

Other critical areas are the masks and resist. The masks are available for pilot line use, but masks with manufacturing-grade defect levels are not available yet. The industry has made progress in reducing the mask defects to a level that will enable memory makers; but a further ~50–100× defect reduction is required to meet the foundry and logic requirements. With continued progress along the defect reduction trajectory of the past 2–3 years and with mask shops becoming more and more proficient at mitigating the EUV mask blank defects, this technical goal is achievable. A bigger challenge will be to ensure a mask blank supply that can meet the industry demand for the mask blanks in 2014–2016. To support the expected EUV mask demand in 2015, a mask blank supply of ~5000 quality mask blanks in 2015 is needed.

The EUV resist materials have seen a dramatic improvement in resolution over the past 2 years with the chemically amplified resists now demonstrating modulation down to 16 nm half pitch and below. The resist sensitivity varies between 10 and 20 mJ/cm^2 for the line and space resists and 30–70 mJ/cm^2 for the contact hole resists. All the resist materials still produce a line width roughness (LWR) significantly higher than the ITRS specification. The LWR reduction in post-exposure processing is seen as the key element to meet the post-etch 'transferred LWR requirements'. The issue with the resist is not 'will resists be available'. Resists already are available. The question is whether they can meet the LWR requirements at a reasonable photospeed. If not, higher exposure doses will be necessary. This will reduce the exposure tool throughput and increase the EUV production costs. Going to the nodes beyond 16 nm half pitch will require further improvement in the EUV technology. The usual industry routes for improving the resolution for new nodes have been higher NA exposure tools, improved resist materials and processing, and further wavelength shrinking. All of these are possible with the EUV. The EUV production tools scheduled for introduction in 2013 have a NA of 0.33. The EUV lens designs are known with higher NAs, such as 0.45 and 0.60. The challenge of these new lens designs will be to accommodate the higher illumination angles with multilayer mirrors and absorbers while maintaining good optical efficiency. Even without a higher NA, EUV tool double patterning would extend the EUV's applicability one additional node, if the industry found this to be cost effective. Finally, some work has started looking at shorter EUV wavelengths. The lens designs would be similar to the current ones for a new wavelength, but a new source, new resists, and new mirrors and absorbers would have to be developed. In the next 1–2 years, or as soon as the first generation of EUV production tools is established, the industry will have to make a decision on which of these approaches is the most viable EUV extendibility path.

3 Nanoimprint (NIL)

The NIL is a technology of creating a patterned template like a stamp that is pressed onto a thin film of liquid on a wafer. The template is transparent, and a brief flash of light polymerizes the liquid so that when the template is lifted off, a relief pattern of polymeric material is left behind. The features in the template need to

be the same size as the final features (unlike current lithographic techniques where the mask is 4× the final feature size). As a 1× technology where the patterning media (the template) actually touches the wafer, the major challenges for the NIL are defects, contamination, and overlay issues. While the NIL can deliver excellent resolution and good line edge roughness, the industry has not yet found a practical solution to the template manufacturing and lifetime challenges. Defect levels are also not yet where they are needed. The technology is still in the roadmap for the future nodes, but the template challenges that are already proving difficult at the 22-nm half pitch will become much more difficult at the 11-nm half pitch node. Semiconductor applications are not the current drivers for this technology, so the semiconductor specific issues are not being addressed quickly. This technology may provide a good approach for early design prototyping, but it will be very difficult for the NIL to become adopted into the HVM chip manufacturing.

4 Maskless lithography (ML2)

Maskless lithography involves using an e-beam writer to expose the resist and write the desired pattern. It completely avoids any mask-related issues. The e-beam-based patterning can provide excellent resolution and at the same time faces a pixel scaling challenge, which limits its productivity. Unlike optical lithography, the pixel throughput gets slower as the features get smaller. To overcome this, multi-e-beam column approaches are being pursued, where the tool will use many e-beams that write at once. So far, production-type tools are not yet available. The LWR is still a problem for this technology because fast writing, and thus high throughput, requires fast resists; but such resists typically have high LWRs. On the other hand, an individual e-beam multibeam writer is likely to be much less costly than an ArF immersion scanner. So even if the throughput is low, it might provide the needed solution for producing the parts that are needed in limited volume. Such chips typically are very expensive if they need an entire new mask set for producing a few chips. But if no mask set is needed, the cost saving might justify a slow e-beam writing tool. This may provide an entry path for the ML2 into wafer patterning. A challenge for all the maskless technologies is defect inspection, and most likely, it will require a die-to-database inspection of the wafers to replace the die-to-database inspection of the masks.

5 Directed self-assembly (DSA)

Certain types of polymers can separate into different phases when annealing. If the polymer consists of two blocks of dissimilar materials, the size of the blocks will determine the size of the regions of the different phase. This is called ‘self-assembly’ and, in the absence of constraints or directing forces, will provide random patterns of the different phases. If some sort of constraint can be applied, the patterns can be made much more regular. For example, if the self-assembly is constrained between parallel linear walls, a pattern of lines can be assembled, or if there is a pattern of holes, the self-assembly may give smaller holes within those holes. This directing of the patterns formed by applying the constraints is called ‘directed self-assembly’ or ‘DSA’. In semiconductor patterning applications, the guiding patterns would have to be put down lithographically, and then a film of a block copolymer would be applied and annealed. If the natural pitch of the block copolymer is suitable for the guiding pattern, very regular patterns of lines and spaces or of cylinders can be achieved. If one of the polymer blocks can be selectively removed, say, by etching, then you have a usable patterning mechanism.

The process flows that can do this across a whole wafer have been demonstrated, and the available feature sizes easily meet the needs of the 16- and 11-nm nodes. The reported LWR of these features is very good and close to what is required in the roadmap. But low defects are a big worry. No one really knows the defectivity of such a process as it is so different from what has been done before. Another issue is that the only patterns that can be made are extremely simple. Realistic circuit patterns will need design tricks and other patterning steps to provide terminated features, empty areas, and other normal circuit features. None of these design issues have reported solutions yet.

Of course, lithography does not go away with this approach. The industry just has to print guiding features, rather than dense features. Ancillary exposures are also needed, such as ‘cut’ exposures that turn patterns of long lines into discrete line segments. These guiding and ancillary features will also have to scale. It is an open question how good the guiding feature lithography will have to be to make the DSA a success.

The resolution capability of the DSA has attracted a lot of interest, and the pace of work in the field seems to be increasing, but is a very new technology to process development. If it succeeds, it would mark a complete change in how the semiconductor industry thinks about controlling critical dimensions. Instead of being driven by a mask and/or an exposure tool’s settings, a critical dimension

would come from a bottle and from the intrinsic properties of the polymer in the bottle. Instead of reworking a wafer and changing the exposure dose to change a feature size, a new bottle of the material would have to be ordered and plumbed. This would be a tremendous transition for the industry. It would be a change from the optical feature sizes to chemical ones.

6 Summary

Extending double patterning to multiple patterning for <20 nm will be technically very challenging and costly. The industry needs to stay on the device shrink roadmap that doubles its function per area roughly every 2 years. While the EUV still faces challenges, it is seen as the only technology that matches the semiconductor industries' current design and patterning infrastructure. The NIL is currently limited to niche applications such as early design verification where high resolution is required and defects do not matter. The e-beam seems promising mostly for low-volume parts where the saving on the mask costs justifies the slow and expensive patterning. The DSA promises excellent scalability and cost, but is so new to the industry that any classic lithographic solution like the EUV would be easier to adopt. While the HVM application approach for the ML2 still faces many technical challenges, some version of it is likely to be used for prototyping and for the low-volume part numbers.

The ITRS lithography roadmap shows a big technology decision approaching the semiconductor industry about how to do the leading edge lithography. New technology is needed to keep supporting the improvements in the device density mandated by Moore's law. The technical options are diverse and interesting, each with their own set of challenges. The leading option and also the option with the most industry investment is the EUV. But the decision on whether to go ahead with the EUV in production depends on the successful infrastructure scale up in time for the roadmap's decision points. Much will be decided in the next 12 months, and it will be interesting to see the final choice.

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