Review Article

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Review of computational lithography modeling: focusing on extending optical lithography and design-technology co-optimization

Abstract: Advances in computational lithography over the last 10 years have been instrumental to the continued scaling of semiconductor devices. Competitive scaling requires two types of complementary models: fast predictive empirical models that can be used for pattern correction and verification; rigorous physical models that can be used to identify key physical effects that must be considered to ensure pattern fidelity, but are too resource intensive to use for full chip applications. Today, all computational lithography efforts such as the optical proximity correction (OPC) and the optical rules check (ORC) depend on the ability to predictively model the lithography and metrology processes. We discuss some of the current modeling practices in optics, mask, resist and etching, leading to the "Holy Grail" of predictively modeling entire patterning process which we call "virtual fab". Extreme ultraviolet (EUV) modeling is discussed due to its potential to extend optical lithography scaling for future nodes. Modeling of novel technologies such as Diblock Copolymer patterning is also discussed to demonstrate new opportunities for continued scaling. Complexity of the "virtual fab" approach is extremely high as there are multiple dimensions in this approach. The need to overcome this complexity, by reducing the number of dimensions of the problem, is evident. Lastly, the ability to leverage lithography modeling in design co-optimization is an important element of semiconductor device scaling.

Keywords: computational lithography; computational scaling; design for manufacturability; design-technology co-optimization; extreme ultraviolet; lithography; OPC; optical lithography; predictive modeling; scaling; simulation; SMO.

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1 Introduction

Computational lithography is informally defined as using extensive computational methods to enable patterning of semiconductor devices with dimensional scaling that fulfills Moore's law [1]. Extensive computation techniques have been developed over the years to enable further scaling when physical scaling is impossible. To understand this, we need to look at the most important equation in lithography, namely, the lithography first principle, as shown in eqn. (1). Resolution R (usually expressed as half-pitch) is proportional to the exposure wavelength but inversely proportionally to the numerical aperture (NA) of the projection optics. The proportionality constant, k_1 factor, is a lumped parameter that represents the complexity and manufacturability of the lithography process, with a practical limit of 0.4 a manufacturable process.

$$R=k_1\frac{\lambda}{NA} \tag{1}$$

For many generations, scaling of physical dimensions in semiconductor devices was enabled by reducing the exposure wavelength (λ) from UV broadband to h-line, g-line, deep UV (248 nm), 193 nm, and ultimately to 193 nm immersion. Extreme ultraviolet (EUV) theoretically has the wavelength that can fuel scaling over several technology nodes, but there are several technical factors that could delay the deployment of EUV technology into high-volume manufacturing. For this reason, scaling may need to continue relying on computational techniques such as multiple mask decomposition, together with the use of advanced optical proximity correction (OPC) and source mask optimization (SMO) in order to reduce the k1 factor. This effectively increases pattern resolution as well as pattern fidelity using diffraction-limited imaging. Both computational and physical advances are needed to enable continued device scaling.

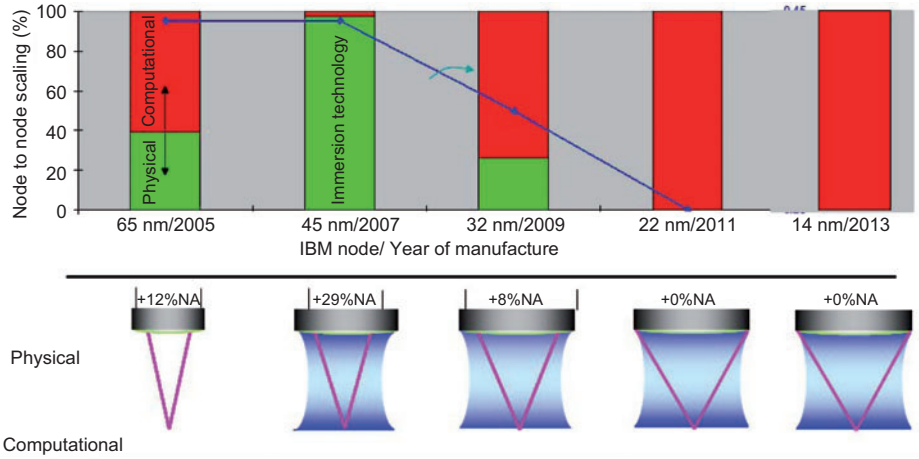
1.1 Scaling scenarios

The contribution of both physical and computational factors in scaling is best illustrated in Figure 1. Before the 32-nm node, lithography scaling was enabled by significant increases in the exposure tool numerical aperture (NA) and the introduction of immersion lithography. However, for the 32-nm node, the increase in NA was only about 8%, and for 22-nm, no increase in NA was achieved. Computational techniques, including advanced resolution enhancement techniques, such as off-axis illumination (OAI) and OPC, become the dominant driving force in scaling for 32- and 22-nm nodes. SMO is an advanced form of OPC that was first adopted in the 22-nm node. EUV lithography will regain the resolution not from NA but from a much smaller wavelength. However, due to various technical issues, EUV is too late to intercept the 22-nm, and even the 14-nm, node. So the use of multiple patterning to achieve subresolution feature sizes becomes essential for 14 nm and beyond. This scaling scenario is illustrated in Figure 1. Moreover, EUV has its own modeling challenges to consider.

Model-based computational patterning is a key enabler for device scaling. Our modeling approach has two components. The first component is based on rigorous scientific process models, which are accurate but resource intensive and limited to small areas. These models are used to understand physical effects and to calibrate approximate models. The second component is the resource-efficient empirical models, which are predictive and fast enough for full chip applications like OPC and ORC. The first component is computationally intensive and requires large Linux clusters and even Blue Gene clusters to run over small areas and volumes. The second component is no less challenging due to large area processing requirements, but requires large clusters and hundreds or thousands of CPUs.

Predictive modeling is becoming a vital part in semiconductor technology because it enables us to develop mask and debug wafer issues with minimum wafer costs. We witness this recent trend by the spin off of the modeling-intensive OPC and resolution enhancement techniques (RET) work from the traditional process-intensive lithography group into separate organizations in many leading edge semiconductor companies. In addition, the size of the modeling/OPC business in major electronic design automation (EDA) vendors and the number of corresponding startup companies is rising at a steady rate. There is a tremendous investment in this new business area and is becoming an indispensable component for the lithography industry. This pathway also brings in new business requirements such as complex design and dataprep solution, utilization of massive computing platforms, as well as a much tighter interaction to the circuit design community in order to extend the technology to the next generation node.

In our vision for the future of semiconductor system R&D, it is not only essential to have an advanced fab with state-of-the-art fabrication tools, which can support new



	65 nm	45 nm	32 nm	22 nm	14 nm
k1<0.6	OPC	OPC	OPC	OPC	
K1<0.5	OAI	OAI	OAI		
k1<0.35				SMO	SMO
k1<0.25					Double patterning

Figure 1 Scaling from the 65- to 14-nm nodes showing both physical and computational scaling scenarios, illustrated in a similar way from [2].

generation integrated processes, but also a "virtual" fab that can provide 100s of Tera-flops of computing power that enable the modeling of complex processes. Many companies or research institutes have established computation centers as a "virtual" facility that has installed high-performance computer clusters. Combining the "real" and "virtual" fab allows us to have the bandwidth to advance computational technology and especially predictive modeling.

It is undisputable that today's chips could not be built without modeling, simulation, and corrections. Statistics will give us some good idea about the scale of the problem. For example, in some layers, about 400 m lithography simulations are required per chip level, about 150 billion fragments are being corrected per chip, and clusters of hundreds of CPUs are used. One supporting result for the usefulness of predictive modeling in correction is that good models enable first time right production. Figure 2 shows that a first time 32- and 22-nm OPC model, if done carefully, can make accurate predictions to experiments in the first OPC iteration, which significantly shortens development cycles.

1.2 History of simulation software

The high level of sophistication in lithographic simulation is much in debt to the landmark work of several researchers, which was pioneered by Dill with his ABC model [3] to describe the basic resist exposure and develop a mechanism, which is the foundation of all lithography simulations. Later, the Neureuther Group at U.C. Berkeley developed a full simulation package that included image formation simulation and is termed SAMPLE [4]. The first commercial simulation software called PROLITH [5] was offered by Mack (now marked by KLA-Tencor Inc.) and followed shortly by SPLAT [6] from the Berkeley's group. All these software are upgraded to vector imaging as time progress. An early mask electromagnetic field (EMF) simulation software called TEMPEST [7] was written by the Berkeley group who treated the mask topography rigorously to enable a feature size similar or lower than the wavelength to be accurately modeled. All of these earlier models are based on physical optical formulations and lumped parameter resist approaches. These models paved the way to the computational efficient models for full chip applications. Resource-efficient optical model approaches rely heavily upon coherent kernels generated by the so-called sum of coherent sources (SOCS) method [8]. SOCS reduces most image calculations into a set of fast Fourier transforms (FFT), which can be accelerated either by advanced algorithms or special purpose hardware. This kernel-based method is well suited for the OPC and replaces the slower Abbe-based formulations. Fast empirical methods for modeling resist such as the variable threshold model (VTM) [9] or the kernel-based compact model such as CM1 [10] were developed to approximate resist threshold variation. These empirical models require extensive model calibration to provide predictive power. A similar effort in predictive modeling of etching [11] and patterning density effects have also developed to optimize mask shapes for the overall pattern transfer to wafer. All of these advancements enable computational lithography to maintain aggressive scaling requirements mandated by mainstream technology.

1.3 Value of predictive modeling

A major application of intensive predictive modeling is the optical model generation for OPC. Early forms of correction were just basic precompensation of mask shapes, introduced in the 1980s, using systematic biasing, serifs [12] and in the early 1990s, the subresolution assist features [13]. In the mid-1990s, simulators were used for rule generation and also used in hand tweaking of DRAM and SRAM cells (for the 240 to 180 nm). Because of the full field requirement and non-optimized hardware platforms, the early forms of OPC were rule-based (180–130 nm) [14, 15]. As k1 shrunk and 2D imaging became increasingly more complicated, the need for model-based OPCs became critical. With significant improvements in both algorithms and high-performance computing (HPC) systems (cluster of hundreds of CPU and hardware acceleration), the current OPC is using almost a rigorous optical model. A hybrid approach is still used in the resist model, as a physical resist model is still challenged in the computation speed.

2 Current modeling practices

In the early days, lithography was operating in the geometrical optics regime, and most work done was mainly empirically. This was very successful for the early process nodes like the half-micron node or before. Only the first-order effect of the imaging components were important and could be well understood through simple theoretical framework and basic characterization methods. All the higher-order effects were small enough to not impact the imaging process and process accuracy. Modeling and

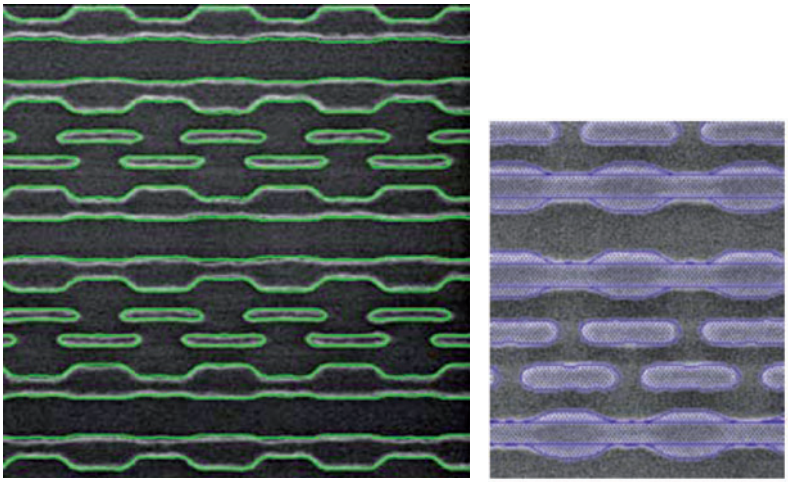


Figure 2 First time right OPC model shows the good match between the extrapolated model [16] and the first wafer SRAM result for both the 32-nm cell (sub-0.200 μm^2) and the 22-nm node (sub-0.160-μm^2) [17]. The two pictures are not of the same scale.

simulation was then treated only as a sidekick of the experimental-intensive development process. In those days, most predictive modeling approaches were used in predicting overlay error as well as focus/dose budget. Undoubtedly, these are still the dominant forms of process detractors in current lithography. However, as we are pushing the limit of technology, a wider examination of the whole lithographic system is needed. A holistic approach of modeling, including the image formation process, the metrology process for patterning prediction, the model-based pattern correction, the design for manufacturing as well as variation-based yield prediction, are needed.

As photolithography is pushing its limit, most of the previously neglected second-order effects in various components in lithography have now become non-negligible. One reason is the increase of NA of the scanners and the use of lower k1 design through scaling, which requires the rigorous treatment of full vectorial effect of the optical train (light source, illuminator, mask pattern shape, mask topography, pellicle, projection lens, and resist stack), as shown in Figure 3 [18]. In EUV lithography, specific effects such as flare mask shadowing and telecentricity error need to be also included. Nowadays, most lithography simulation software is equipped to handle some part or all of these secondary effects. However in most cases, after the image in the resist is obtained, the subsequent processes such as resist development and etch are still modeled in a semiempirical way due to the complexity of the first principle models.

In an optical projection lithography system, all the pattern information is contained in the mask. The optical trains act as an information low-pass filter. The computed images, after optical propagation and nonlinear reaction of resist, based on resource efficient models, must have high fidelity to the actual physical images formed. Traditionally lithographic imaging is based on the computation of the diffraction orders as a simple set of Fourier series orders from the Manhattan only shapes on an ideal screen. All the other 2D effects (shape roundedness or line end pullback on mask) or 3D effects (mask topography) are ignored. We will address the advanced modeling of these secondary effects in the next session.

In a real mask, patterns are not identical to the design data because a mask writer introduces systematic deviations from an ideal Manhattan layout. These deviations come from an e-beam writer as well as a laser writer, as shown in Figure 4. Empirical models are calibrated and used today to predict the exact mask shape after the manufacturing process. The systematic mask manufacturing corner rounding and the line-width errors can be predicted to reduce its impact on model accuracy.

Another critical mask effect is the EMF scattering due to mask topography, which produces diffraction patterns, which are quite different from that of an ideal thin mask that was assumed in earlier technology nodes. The EMF effect impacts the diffraction order amplitude and phase, hence, introducing feature-dependent CD and focus deviation [20], as shown in Figure 5A. An EMF bias was attempted as a zeroth-order correction to the thin-mask assumption (TMA) approach to model the EMF effect in the 45- and 32-nm nodes but may not be capable to provide required image accuracy in the 22-nm and beyond nodes. Rigorous Maxwell solver is needed and was addressed with a fully parallel internal FDTD code on Blue Gene™ [20] with a good scaling behavior as shown in Figure 5B.

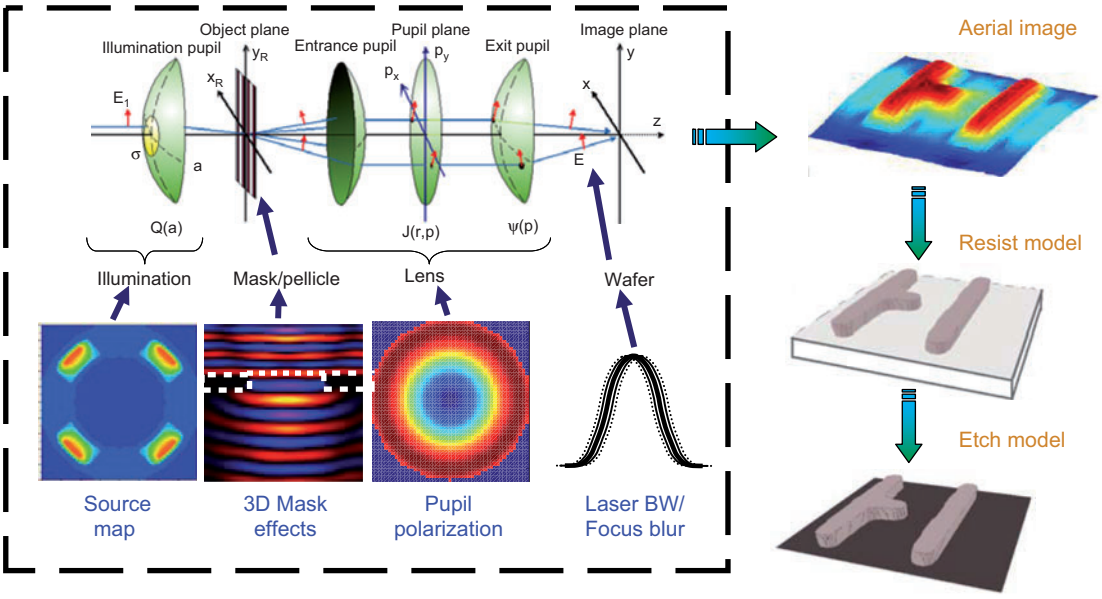


Figure 3 Schematics of the modeling elements in the optical train [19].

There are also other rigorous algorithms that can be used such as the waveguide method, rigorous coupled wave analysis (RCWA), and the Finite Element Method (FEM) [22]. Nevertheless, we still need simplified models that accurately models the EMF effect with speed comparable to the TTMA for a full chip correction scenario. Several approximate models were proposed to take into account the primary behavior of the EMF effect by adding corrections to the TMA. These methods include the boundary layer method [23], the domain decomposition method [24], and the frequency domain correction method [25].

In Table 1, a spectrum of resist modeling approaches that has been introduced is shown. From top to bottom, the models become faster but less predictive.

Each model has its own preferred application area in lithography. Lumped parameter models provide 3D capability that enable through-process prediction of assist printing at the top of resist, and the speed advantage of the diffusion aerial image model enables a full chip detection of litho hot spots. The rigorous resist model, however, is tough to use for full chip applications as it has to model complex simultaneously occurring physical and chemical phenomena that are not thoroughly understood and difficult to model. These models need to consider polymer dynamics, evaporation, deposition, reaction, diffusion, photochemistry, electrodynamics, etc. One example of the use of rigorous model is the prediction of resist pattern collapse.

Etch modeling approaches are important because a real resist profile will affect the pattern transfer to the final etch profile. The final pattern CD might not be correlated to resist CD if the resist profile is not considered ideal.

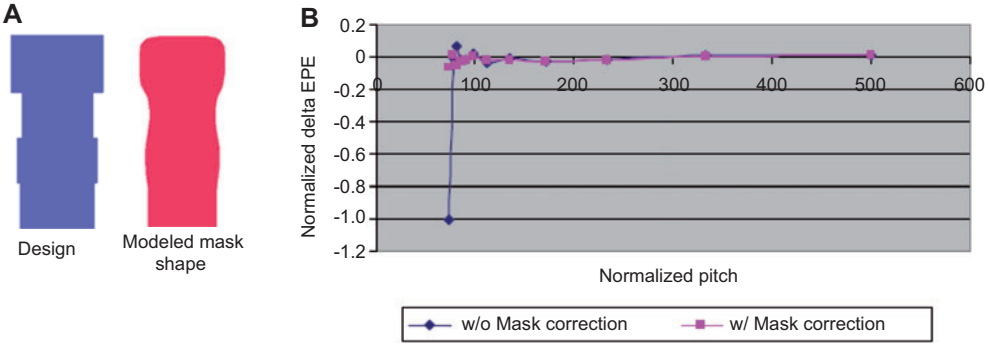


Figure 4 (A) Comparing the design shapes and the modeled mask shapes. (B) By applying a mask model, one can reduce the error in the OPC EPE error (normalized here) especially in the small pitch range [21].

Model type	Focus application	Examples
Molecular models	Simulation of molecular-scale effects	Willson, de Pablo, Gogolides
Continuum physical models	Physical description of exposure, bakes, and development	Dill, SAMPLE, PROLITH, solid-C, STORM
Lumped parameter models	Compact diffusion and development models	PROLITH, Brunner-Ferguson
Diffused aerial image model	Aerial image parameters and physics	Fukuda, CM1
Aerial image models	Fit threshold behavior to image parameters	Constant threshold, variable threshold

Table 1 A spectrum of resist models showing the slow but more predictive models from the top to the fast but less predictive models at the bottom.

However, resist modeling is similar to resist modeling in its complexity. A resource-efficient empirical plane-view model has successfully modeled through-pitch etch bias in wafer plane and was used in etch-aware OPC schemes. The etch model spectrum is shown in Table 2.

Both Tables 1 and 2 suggest that a spectrum of models are available, and the selection is based on the user's tradeoff between accuracy and run time. Fast empirical models, in general, describe less first principle physics or chemistry compared to more rigorous models but require more data to calibrate the models.

2.1 Integrating all elements

Our ultimate goal in modeling is to leverage critical modeling elements for processing steps into an integrated tool that we called "virtual fab". Virtual Fab flows require separable models from mask to post-etch wafer profiles. These flows should be capable of producing plane-view and cross-sectional profiles and contours in 2D and 3D. The final profile can then be passed to the device simulator for device prediction. This approach is desirable as the pattern variability can impact the device performance and hence circuit yield. To find a better overall performance merit, it is necessary to go beyond pattern fidelity. Figure 6 shows an example that the best electrical matching might not be corresponding to the best pattern matching. This brings up the question of why not use electrical parameters for our pattern correction? A few objectives such as Vt variation, device stress, spacer thickness, saturation current, leakage current, cell delay, etc. may be used. However, in these cases, we need accurate and yet efficient Si-contour-based device models and shape-based parasitic extraction for timing delay models. Figure 7 shows an example of different CD retargeting optimized for each device in a SRAM cell could result in shifted lithographic process variation bands (PV-bands) that are beneficial to the device yield.

The direct optimization of device metrics from pattern correction allows us to achieve a higher-level optimization that is more relevant to circuit performance. However, there is another component, which is the device model accuracy that is equally critical compared to device dimensions. The extensive use of computational patterning provides an accurate structural information to a device model for more accurate voltage-current (VI) prediction. Because the accuracy of a device model is important for the final yield calculations to model device characteristics, it is desirable to briefly mention the trend of device simulation to understand the key requirements. The current device models use continuum models to solve the drift-diffusion equation or hybrid drift equations with full band structure and quantum effect included. In the next 5 years, increasing granularity in doping profile and device structure require us to include full 3D field

Type of model	Comments
Empirical-full chip model	Captures microloading effects, takes into account influence of density loading through visibility kernels
Chemical/physical predictive model-reactor scale to full chip and below	Goal is to model RIE process through chemistry and distributions of energetic species at idealized plane for contacts
Level set front propagation modeling of etch processes	Can take into account etch chemistry, re-deposition, and re-emission processes
Multiple level set/fast marching methods	Describe plasma, chemical kinetics, absorption, re-emission, sputtering, etc.

Table 2 A spectrum of the etch model showing the fast but empirical model from the top to the slow but more physical model at the bottom.

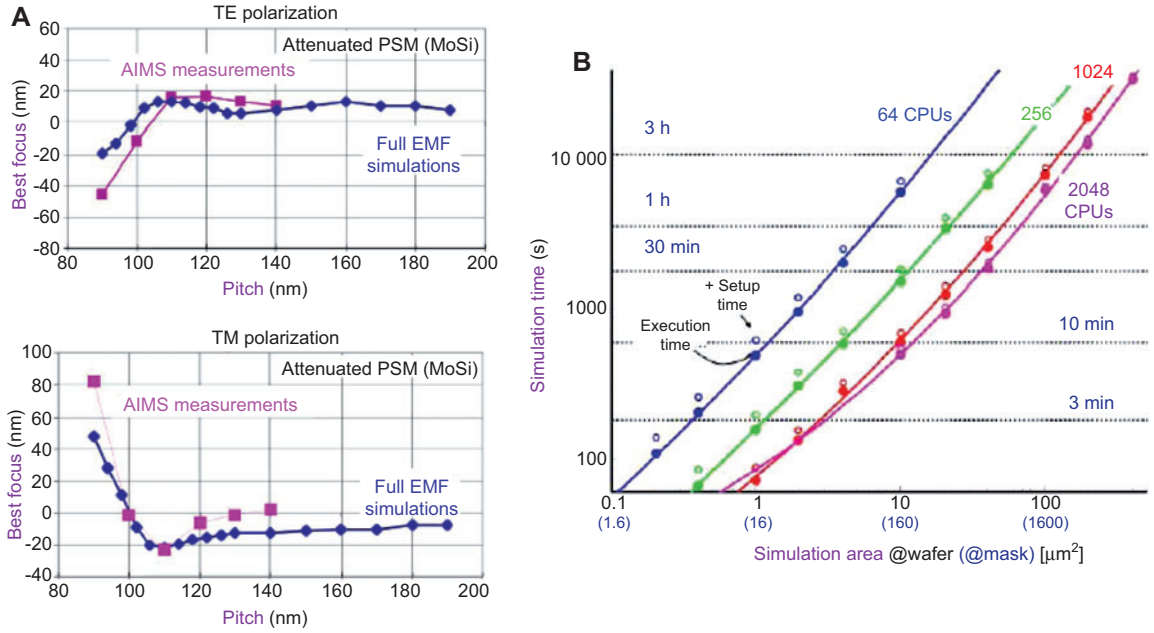


Figure 5 (A) Best focus shift vs. pitch behavior from FDTD simulation and AIMS measurement for TE mode and TM mode. (B) Scaling is linear for FDTD EMF simulation in Blue Gene™ [20].

fluctuations. As the device is shrunk further, the material is strictly granular, and better material models with transport properties for granular structure are necessary. This, of course, increases the complexity of the model by a large extent. Table 3 shows the evolution of the device models as predicted.

2.2 Model calibration

Model calibration is a key component for a quality model, especially an OPC model. A model can only be as good as its calibration data. We need to make sure that the expected output value of the model prediction is the same as the true mean of the population. An optimum sampling scheme is desired. There are three main aspects of optimum sampling that can improve model accuracy. First, we need optimum spatial sampling that capture all error types such as Wafer to wafer, Die to Die, and within die and across features error. Second, we need to have an optimum spectrum of samples types, such as 1D, 2D features, and maybe special calibration structures. More recently, contour-based calibration [28] is gaining acceptance as an alternative to CD-based calibration. Third, an optimum sampling size choice is required to boost the confidential level of the sample prediction under a specified error budget to avoid oversampling or undersampling. A parameter such as the maximum effective sample size

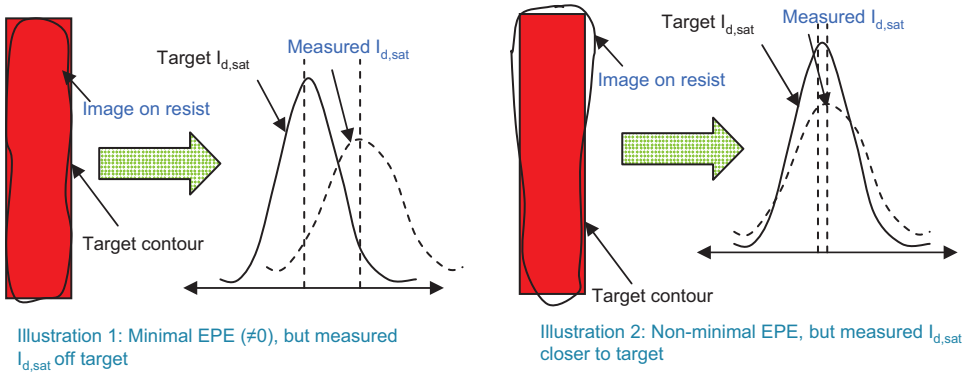


Figure 6 Illustration of case that minimizing EPE error might not correspond to minimize device saturation current error and vice versa [26].

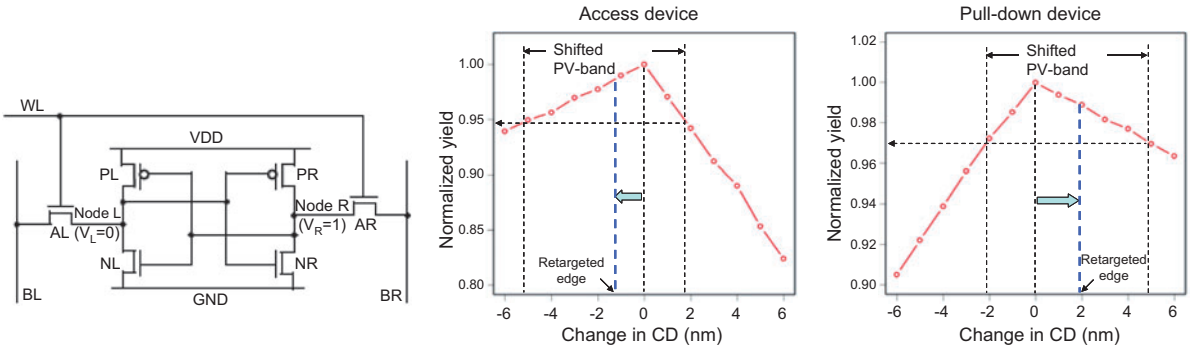


Figure 7 Best SRAM yield achieved by allowing different design retargetings on each device to skew the PV bands favorably in terms of electrical characteristics [27].

(n_{eff}) was proposed [29] as a function of sample confidence level, total variation, and the error budget. One might want to select a sampling plan that has the highest overall n_{eff}, as illustrated in Figure 8. This approach ensures us to have same confidence levels on the sufficiency of the sampling on various calibration features based on the sensitivity of individual feature to process variations.

$$n_{eff} \cong \frac{4t^2_{\alpha/2}\sigma_{tot}}{k^2 EB^2} \tag{2}$$

where σ=confidence parameter, $t_{\sigma/2}$ is the Student-*t* parameter for the corresponding confidence level, σ=total variance, and EB=error budget.

2.3 Modeling in metrology

Modeling practice is not only limited to pattern formation in lithography but also includes the physical modeling of many physical metrology processes such as scatterometry or CDSEM. Among these metrology processes, scatterometry has been enabled by the fast rigorous EMF modeling of the resist gratings using algorithms such as RCWA. Scatterometry enables massive data collection for process/Tooling analysis and maybe in OPC calibration as well. The pattern profile parameters such as pitch, CD, sidewall angle (SWA) etc can be extracted using multiple beams with different incidence orientations and polarizations, and this open an opportunity for complex profile geometry to be characterized after the etching of the patterns [30] as shown in Figure 9B. Moreover, it is also possible to predictively model the stochastic focus and the dose variation by scatterometry on lithography data [31]. Figure 9A shows the CD measured by scatterometry against groups of focus values.

Rigorous and predictive models for metrology are not currently explicitly used in imaging and patterning calculation, but they are becoming more important as they can improve the model calibration data quality and maybe in the future, it can be incorporated in the computational patterning flow with some new applications.

2.4 Modeling of EUV

EUV light propagation is governed by the Maxwell equations and also subjects to diffraction limitations. Many optical modeling techniques can be applied to EUV except some unique imaging features that are worth mentioning. First, EUV optics require the use of an all-mirror design, which make the imaging field an arc field, and inherently, the chief ray becomes θ (~6°) tilted from the optical axis. The chief ray angle tilt causes the system to be maskside nontelecentric [32] so the source pupil is shifted inside the system pupil (Figure 10).

Model types	Device	Process	Timing
Continuum models	(DDE and HDE, full band MC, Poisson-Schrodinger solver) geometry, QM effects	Fick's law, rate equations, structure, materials	Now
Doping and structure granularity	(3D DDE and HDE), field fluctuation	3D diffusion, oxidation, structure	+5 years
Granular matter	Transport properties for finite structures	Material, dopant, interface interaction	+10 years

Table 3 A spectrum of the device models starting from the fast continuum model to the slow but accurate granular model.

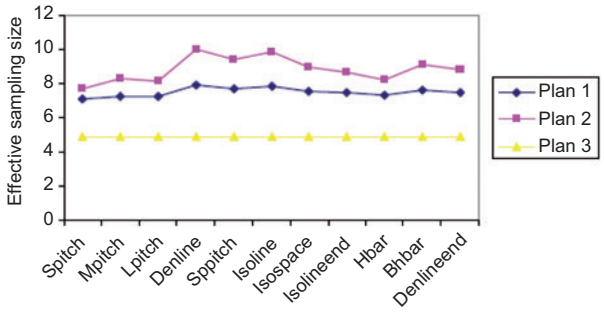


Figure 8 A plot of n_{eff} across different pattern types for three different sampling plans. It is shown that plan 2 has the highest n_{eff} across all features and is the best sampling plan among the three [29].

Another effect of the chief ray tilt is the so-called "shadowing effect" [33] when light rays are reflected through the reflective EUV mask that has absorbers of high aspect ratio. Figure 11 shows the shadow casted by the absorber, which is different in different orientations. In a first order, the CD bias due to shadowing for an absorber of height h can be expressed as the following using pure geometric optics argument.

$$S_v = h\tan\theta\cos\phi, \quad S_h = h\tan\theta\sin\phi$$
$$H\text{-}V\ Bias \quad HVB = S_v - S_h \tag{3}$$

Here, θ is the CRA and is about 6° from the normal and is the angle between the optical axis from the field center to the field edge, as shown in Figure 11.

As the critical dimension of the absorber on the mask become smaller, but with the same absorber height, the geometric shadow model will break down, and the rigorous EMF simulation model is needed as in the optical thick mask, but the simulation will need to include the reflection from many layers of the Bragg mirrors underneath the absorber patterns, which is computational intensive unless a certain set of simplifying boundary conditions are applied.

Another unique feature for EUV modeling is the relatively high flare level in EUV optics because total integrated scattering (TIS) is inversely proportional to wavelength squared as shown in Eq. (4). Although the number of mirrors in EUV lenses is smaller than the number of lenses in a 193-nm immersion system, the flare level as a whole is much higher. The point spread function of the EUV flare usually implies a power spectrum that resembles a fractal power law [35] of r, as shown in Eq. (5).

$$TIS \propto e^{(4\pi\sigma/\lambda)^2} - 1 \approx \left(\frac{4\pi\sigma}{\lambda}\right)^2 \tag{4}$$

$$PSF(r) = \frac{K}{r^\gamma}, \quad r_{\min} \le r \le r_{\max} \tag{5}$$

where K is a multiplicative factor, γ generally referred as a fractal exponent that modulates the speed of the decay of the point spread function (PSF), λ is the wavelength, σ is the RMS roughness of a reflective surface, r_{min} is chosen as the minimum radius that closely related the optical radius for most OPC imaging models where r_{max} is the practical radius limit that the user can define based on the accuracy requirement of flare calculation, for example, the 90% energy inclusion zone extent.

There is a special case for the PSF that seems very interesting which is when γ≤2, when we calculate the total flare contributed to a single point by integrating the PSF over a field. When

$$\text{Net Flare} = \text{Flare PSF} \otimes \text{Reticle Transmission}$$
$$\text{Flare}(\vec{\mathbf{x}}) = \int_{r_{MIN} \le |\vec{x}-\vec{x}'| \le r_{MAX}} \frac{K}{|\vec{\mathbf{x}}-\vec{\mathbf{x}}'|^\gamma} m_T(\vec{x}')\, d^2\mathbf{x}' \sim \int \frac{r dr}{r^\gamma} \sim r^{2-\gamma} \tag{6}$$

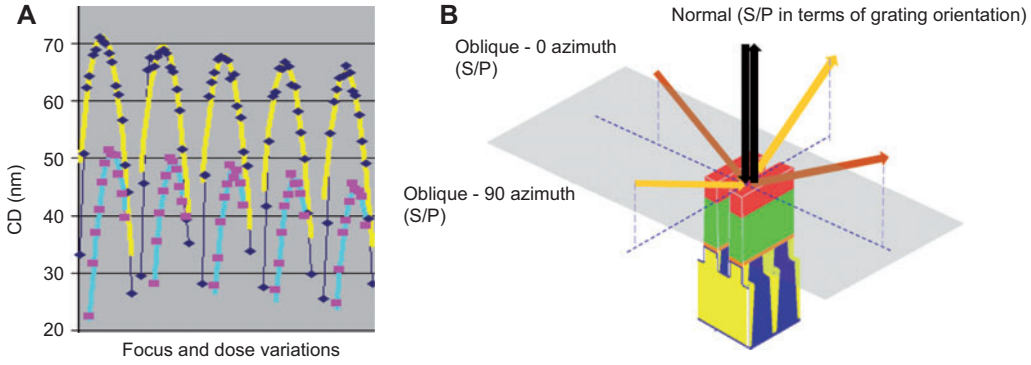


Figure 9 (A) Modified Bossung curves calibrated by scatterometry CD data with focus and dose variations. Good prediction for focus and dose from scatterometry CD is obtained [31]. (B) Possible opportunities for complex scatterometry application to determine 3D profiles of etched features by using multiple incidence angles and polarizations [30].

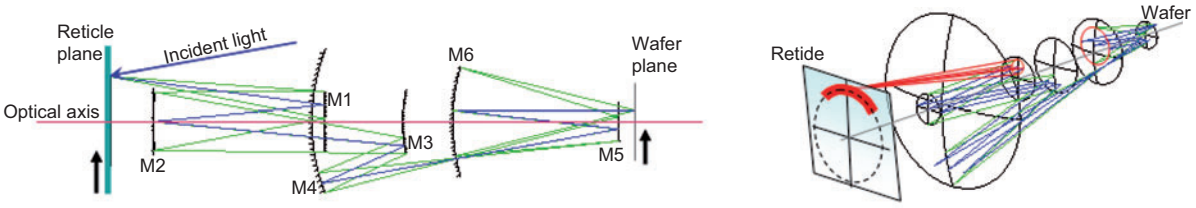


Figure 10 One example of a EUV projection optics system showing the arc field and maskside telecentricity [33].

When $\gamma \leq 2$, the integral is divergent, which implies a very long range of interaction (in the mm range). EUV optics PSF usually has a slope very close to 2, and hence, EUV flare is important across the whole chip. Practically, a large optical kernel is needed to estimate the flare contribution. Fortunately, the flare is mainly impacting the image incoherently, and because of its large kernel, the flare can be calculated using an averaged pattern density instead of an exact geometry on the mask. Most of the OPC software nowadays supports this long-range pattern-density-related flare calculation to provide a better correction on the EUV mask. Another type of long range flare, which is basically out-of-band (OOB) radiation, comes from the nonzero reflection of OOB radiation from reticle blades and other surfaces of the scanner and will affect mostly the edge of the exposure field [36].

There are other imaging issues that are relatively strong in EUV such as line edge roughness (LER) of features, non-uniform CD (Figure 13), and the secondary electron blurring of resist from EUV exposure. Line edge roughness and CD micro-non-uniformity is more pronounced in EUV because of the requirement of the high photo speed resist because of the insufficient EUV power available from the current EUV sources. High photo speed means less photons are required to expose the resist, but stochastic variation, called shot noise, causes a micro-nonuniformity in the reticle field and, in turn, creates roughness on the resist edge (Figure 12). One way to improve LER is to reduce the photo speed, but again, this requires high EUV power. This dilemma can be explained by the famous RLS (Resolution-Line edge roughness-Sensitivity) constraint for EUV lithography and theoretical treatment has been developed [38].

$$\sigma_{LER} \approx \left(\frac{I}{\partial I}\right)_{edge} \sqrt{\frac{T}{\rho_{PAG} \alpha Q \nu E_{size} R^3}}$$
$$Blur^3 \cdot \mathrm{LER}^2 \cdot \mathrm{Dose} \sim \mathrm{Constant} \tag{7}$$

where σ_{LER} is the roughness (nm), I is the image intensity, E_{size} is the sizing dose (#photons/nm^2), and R is the PEB diffusion range (nm), Q is quantum efficiency, ν is the photon-PAG interaction volume (nm^3), α is the absorptivity (nm^{-1}), and ρ_{PAG} is the PAG loading (#PAG/nm^3).

Shot noise also manifests itself as a CD uniformity detractor. This can be seen in the stochastic modeling of

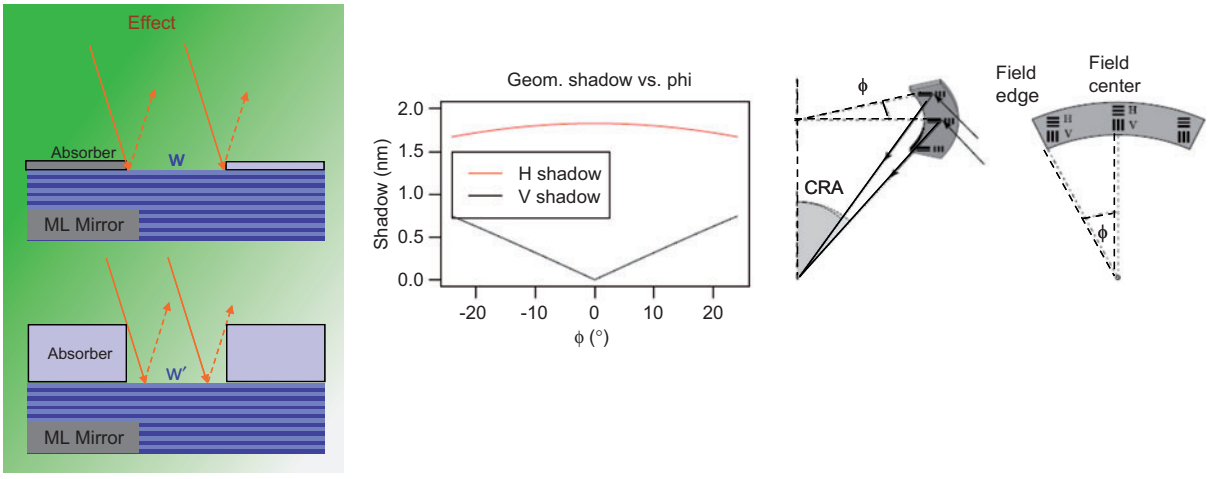


Figure 11 EUV mask shadowing effect due to tilted chief ray angle (CRA) [33] and the breakdown of a simple geometric shadow bias and the corresponding spatial configurations due to CRA and the arc field [34].

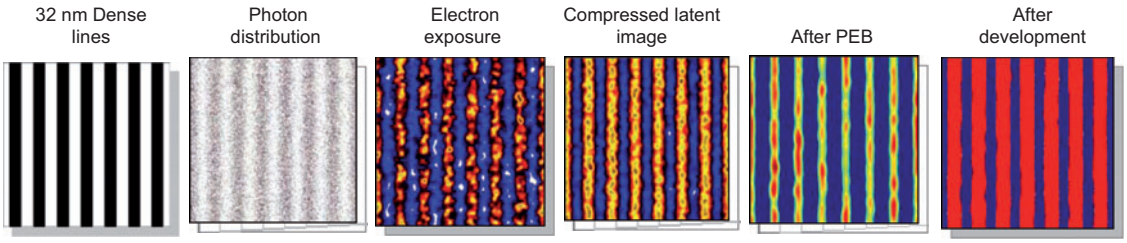


Figure 12 Resist model results at L=13.5 nm with stochastic exposure. The granularity of the latent image is due to shot noise, and the fluctuation is transferred to the photo resist edge roughness [37].

the printing of a holes array using high photo speed resist as shown in Figure 13.

Modeling of a shot noise effect is time consuming because a large-scale Monte Carlo simulation is needed. OPC modeling with a shot noise effect could be tough, but there may be ways to work around this as most Monte Carlo simulation is embarrassingly parallel, which means lookup tables and certain probability density function (pdf) could be used. However, there are studies that correlate image log slope (ILS) with line edge roughness (shown in Eq. (7) also) so a simple ILS metrics might be used in a phenomenological model to predict the impact of LER in a full chip OPC application.

The secondary electron blurring of the latent image in a chemically amplified EUV resist comes from the generation of secondary electrons due to very energetic EUV photons impinged on the resist. As the acid generator is sensitized by the presence of secondary electrons, the blurring in resist requires the calculation of accumulated energy of secondary electrons by tracking the electron trajectories by calculating the elastic and inelastic scattering in the resist material. This method requires a full-scale Monte Carlo simulation, which is time-consuming. A PSF can instead be used for the calculation of accumulated energy profiles to reduce the processing time significantly. Based on Kozawa et al., the EUV secondary electron blurring can be modeled as a PSF kernel [39] as shown in Figure 14 and probably able to be absorbed in a calibrated empirical resist model for OPC purpose.

3 Modeling of novel technologies

Modeling of the mainstream optical lithography patterning techniques is being widely practiced by the industry. However, there are also novel areas that require modeling to enable basic research. One example is the use of block-copolymer (BCP) self-assembly for sublithographic patterning. If not directed, the self-assembly processes are not suitable for forming patterns in a large area application because of its intrinsic high defect density. Establishing optimal guiding lithographic patterns, either chemical or topographical, is critical to guide the assembly process in a much favorable way to form highly regular segregated phases resulting in a minimal energy state. The concept of directed self-assembly (DSA) is illustrated in Figure 15 showing the effect of guiding patterns in reducing the randomness of the self-assembly process.

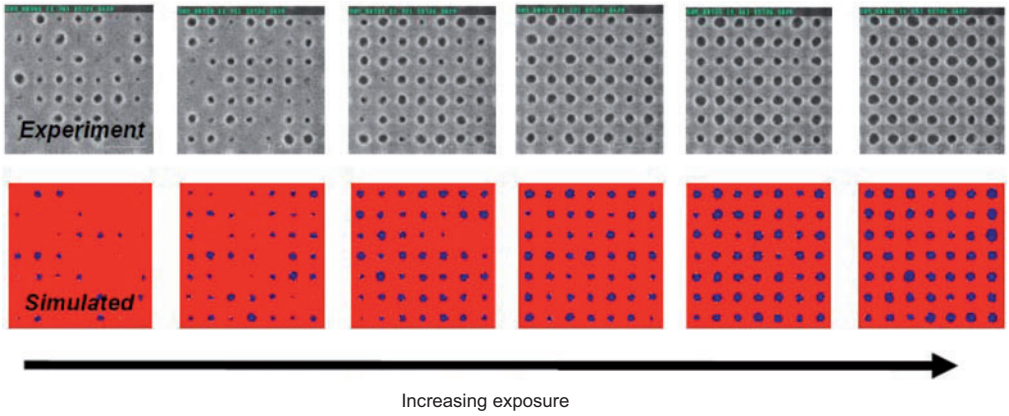


Figure 13 Experiment and simulated 32-nm dense contacts using NA=0.25 and λ=13.5 nm [37].

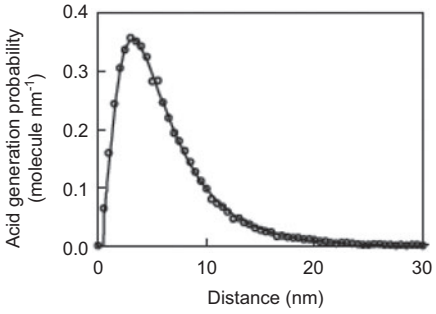


Figure 14 PSF of chemical amplified resists used for EUV lithography. This PSF represents the probability of acid generation at the distance r from the EUV absorption point. The open circles represent the acid generation probability per spherical shell thickness induced by a single EUV photon, which were obtained by calculating the electron trajectories in a model system of EUV resist by a Monte Carlo method [39]. By convolving this PSF with the EUV photon distribution, the extent of the boundary of the resist edge can be determined.

Different molecular simulation models are suitable for working on different molecular length scales. For BCP, it is very impractical to perform molecular level simulation. There are multiple approximations that treat polymer as structureless volumes that has a coarse length scale, with spatially uniform density often held constant. Table 4 below indicates that the different types of mesoscopic polymer field calculation existed for BCP simulation as well as compact DSA models that are resource-efficient for OPC purpose.

There are two main categories of DSA applications, namely, for pitch reduction and via rectification. Pitch reduction for line and space features is achieved by forming vertical lamella structures of opposite phase that can be selectively etched to form a grating that has a resolution beyond the diffraction limit. Figure 16 shows some of the Monte Carlo simulation of line/space formation guided by a trench structure by a self-consistent field theory (SCFT) and mean-field Monte Carlo simulations. The goal is to guide the development of new patterning technology to complement traditional lithograph for further scaling without further increase in optical resolution. A similar frequency multiplication can be achieved for via array that decreases the pitch of a hexagonal closed-packed (hcp) via array into half. The success of the DSA frequency multiplication depends on the precise control of the guiding patterns as shown in Figure 16. Lower resolution guiding patterns can be printed using immersion lithography, hence, extending well-established optical lithography methods such as OPC infrastructure, to enable next generation scaling.

Another application is called via rectification as shown in Figure 17. DSA vias tend to form a vertical cylinder even if the guiding pattern has severe distortion or CD error. This self-healing effect is useful to print very small vias with a CD control unattainable by conventional lithography, which is prone to a high mask error enhancement error (MEEF). This effect can be represented by the SERF factor, which is the ratio of the CD variation of self-assembled features to the percent CD variation of the DSA guiding pattern. The final error factor is defined by MEEF*SERF [42].

The benefits of DSA via rectification can be readily seen in Figure 18, which plots the MEEF and exposure latitude for a dense via staggered array across several technology nodes. This indicates the benefit of DSA to extend optical lithography to the 15-nm node and beyond with just a single exposure.

Defects traditionally have been a problem for the self-assembly processes because defect formation is

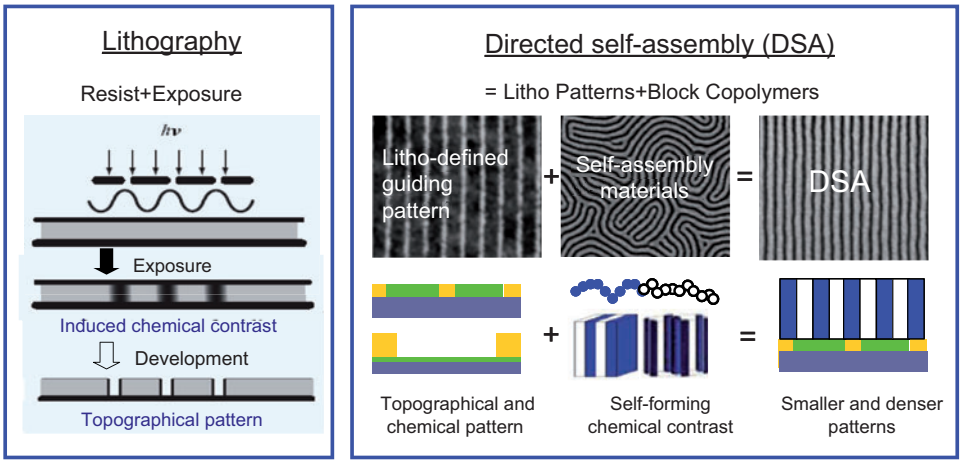


Figure 15 (A) Illustration of the concept of directed self-assembly [40].

Purpose	3D	Compact 2D for OPC
Optimization	SCFT (Fredrickson)	Pseudo-free energy model (IBM)
Optimization	Simple force balance	
Simulation	Cahn-Hilliard-Cook model (Bosse)	Pseudo-free energy model (IBM)
Simulation	Monte Carlo/molecular dynamics using Hefand-Tagami Hamiltonian (dePablo/Detcheverry, J. W. Pitera)	New models to be developed
Simulation	Complex Langevin	
Simulation	Particle simulation (Glotzer)	

Table 4 A Spectrum of 3D but slow models and compact 2D but fast DSA models (Courtesy of Jed Pitera).

thermodynamic in nature and subjected to stochastic variation of localized free energy and resulting in fluctuation in morphology of the system. By using the Monte Carlo method to simulate DSA lamellae formation within a guiding pattern, defects formation can be predicted, and the free energy barrier for defect formation can be calculated to optimize the guiding channel width for a minimum defect density possible. This information is essential for the determining optimal target bias in DSAOPC (Figure 19).

Most of the simulation models for DSA are still too computational intensive to be suitable for full chip OPC. As an early effort to bridge OPC with DSA, we have developed a fast compact 2D model that is suitable to predict the locations of DSA vias and achieved roughly five orders of magnitude speedup. Figure 20 shows a comparison of prediction between the 3D model and the 2D compact model. This fast DSA model enables a full chip OPC for creating mask shapes that print high-fidelity guiding patterns and is possible with the use of a mask optimization algorithm that we called DSAOPC. Figure 21 shows the example of using DSAOP to print a group of vias that is too close to be resolved by conventional immersion lithography.

A similar model in theory can be developed for forming DSA lines and spaces for the application on layers that uses dense gratings.

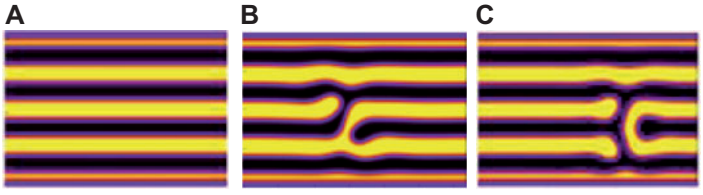


Figure 16 (A) The simulation of self-aligned patterns from diblock polymer lines in a narrow prepatterned trench. Note that there are certain boundary conditions that favor the formation of parallel lines inside the trench [41]. Examples of simulated polymer density profiles of (B) dislocations and (C) disinclination defects [41].

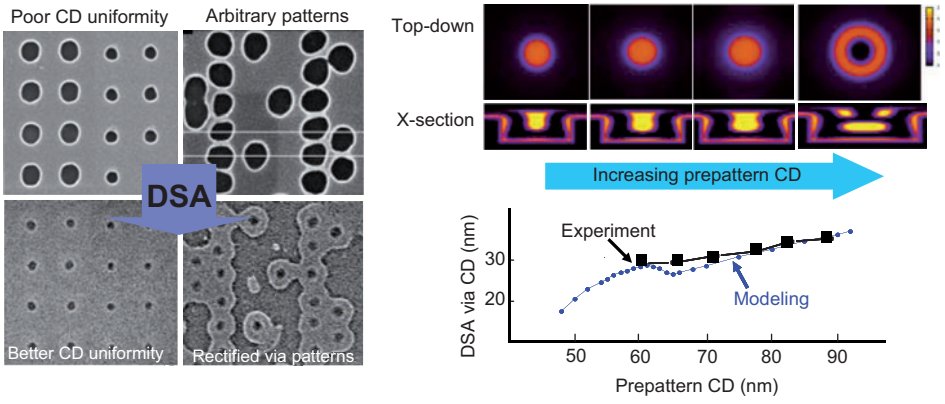


Figure 17 (A) Via rectification and (B) the 3D Monte Carlo simulation for DSA vias and its comparison with experiments [40].

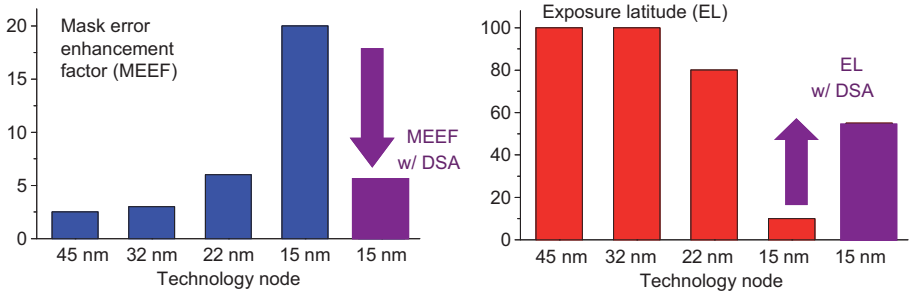


Figure 18 Benefit of DSA via rectification in reducing CD errors and improving both MEEF and exposure latitude [42].

4 Modeling specifics for source mask optimization

Before we switch to a design-related topic, we would like to discuss briefly the issues on applying a resource-efficient model to full chip patterning optimization techniques, which are design construct specific. Basically in OPC, as long as the empirical model provides a good sampling of the parameters and a robust fitting of the parameters, there is no special issue. However, for the advanced pattern correction technique like SMO, there will be separate issues that need to be taken care of.

The first issue is the resist modeling for SMO [44]. In the current OPC model, the resist model may not be completely decoupled to the optical model (see Figure 22), and actually, it is a function of illumination, optics, film stacks, resist chemistry, metrology, etc. During source optimization steps, illumination keeps on changing so the resist model needs to be 100% decoupled from the optics, and it should be only a function of resist chemistry. Figure 23 shows the difference in imaging for resist models of the same resist calibrated differently and applied to the same SMO solution. This founding supports our argument about the resist model requirement here.

The second issue is model differentiability. This issue is important when resist profile calculation is included during the optimization loop where the resist model is evaluated many times, and the gradients and Hessians of the resist profile are being used to guide the internal search of the parameter space. If the model is not differentiable, there may be chances that optimization might not converge normally. Many sophisticated nonlinear kernel-based models or simple variable threshold models might not be differentiable, while a simple linear convolution kernel model will be perfectly differentiable but might not be able to have the best model fitting results. Careful balance of the SMO requirement on model accuracy and optimization stability is required.

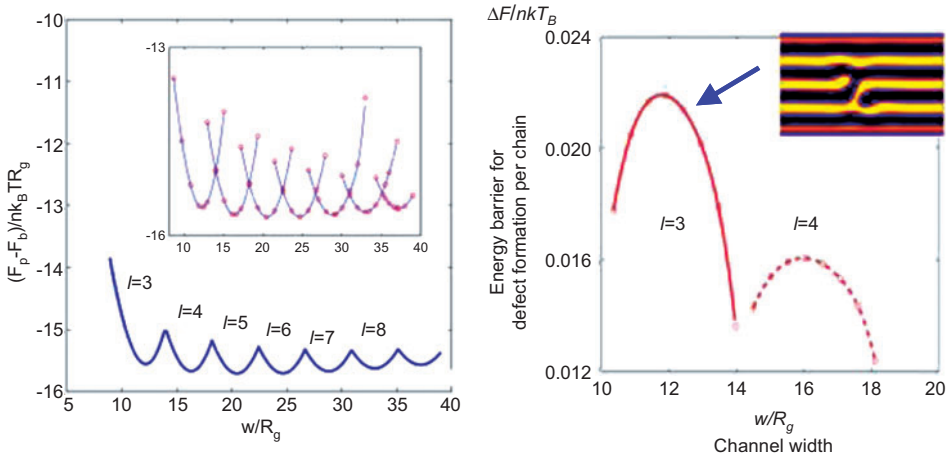


Figure 19 (A) The plot of free energy difference of free energy of forming perfect lamella (Fp) to bulk free energy (Fb) showing the window of stability. (B) The plot of free energy barrier for defect formation vs. guiding channel width (w), indicating an optimum channel width for the formation of a specific number of DSA lines [41].

Figure 20 The accuracy of the fast 2D DSA model compared to 3D Monte Carlo model in the prediction of DSA via locations for merged guiding patterns [43].

5 Design-technology co-optimization

Traditional design scaling is lagging in pace to produce a system optimum for a certain technology node because most designs are agnostic of the lithography implementations and the corresponding limitation, so the need for new computational lithography tools to enable scaling is thus imminent. Besides SMO, which is still a lithographic technology, we need collaboration with the design community for a much more global optimization. Design-technology Co-optimization (DTCO) co-optimizes both lithography and design scenarios. A methodology has been developed to score designs using a tool called the lithography manufacturing assessor (LMA) so a well-balanced ranking of designs can be made. Figure 24 shows such an example of the LMA assessment of different designs [46]. A common outcome of this assessment could be a set of restricted design rules or a set of acceptable design library, which is litho-friendly (i.e., possess adequate process latitude). The LMA tool also allows the designer to create litho-aware layouts. In the litho-aware layout, the designers complement traditional design rules with direct litho modeling to achieve physical and parametric yield targets for aggressive layouts, which are resolution challenged. Figure 25 shows an example of applying the layout process variability bands, which provide an opportunity for layout enhancement for new technology nodes.

Computational lithography tools such as SMO and LMA have to rely on accurate predictive models to enable DTCO. In such applications, often many design clips or large area designs are needed to be optimized and evaluated in order not to miss "hot spots" that can only be detected with sufficient areas or context around clips. For DTCO, not only predictive lithography model is needed but many other predictive unit process models (such as etch, CMP, and thin film deposition) and device models (for electrical characteristic and parasitic) are required to produce a designer-intent design solution. In principle, all process and device performance can be predicted so a better device or process design can be obtained before starting any costly experimental work.

5.1 Ultimate design for scaling

Recently, there are reports on the feasibility of using unidirectional designs for simplifying designs to enhance the design migration to future generations and potentially improve circuit yield. One derived advantage is the improved process windows due to a simpler RET solution because of more regular designs. A simpler OPC [47] and a reduced number of hotspots are possible as shown

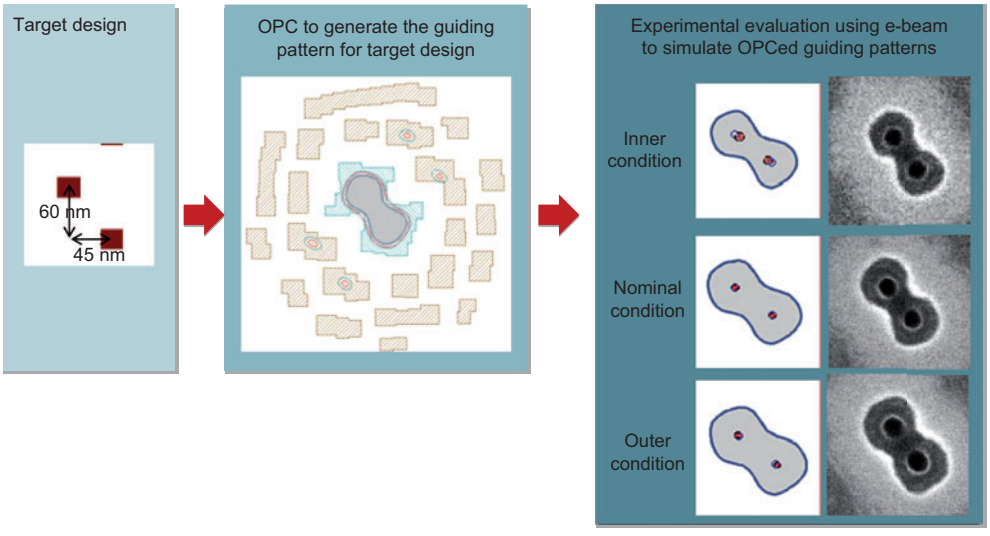


Figure 21 Schematic showing the generation of mask pattern by DSAOPC to print an optimum guiding pattern that predicts to form vias as targeted through extreme process conditions and the experimental verification of the results [43].

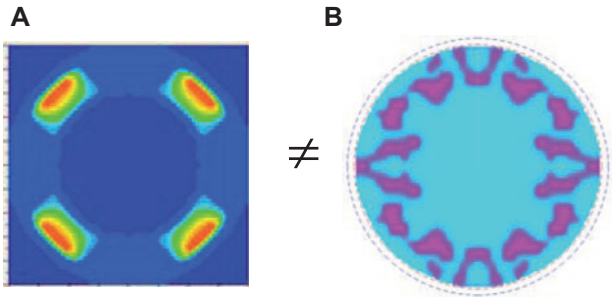


Figure 22 Example of (A) conventional illumination and (B) SMO pixelated illumination. The resist model derived from the OPC calibration data might be different from these two cases.

in Figure 26. Much fewer constructs are needed for the designers to construct standard cell designs for unidirectional designs [48, 49]. This actually might be a more effective form of DTCO that can drive to a true global optimum in terms of design and manufacturing cost for the scaling of device dimensions. Figure 27 shows some preliminary study comparing bidirectional M1 designs and unidirectional designs with the constraint that the total cell areas are kept more or less the same [48].

6 The curse of dimensionality of lithographic optimization

A full but efficient variation modeling engine that can overcome the curse of dimensionality will be crucial for virtual fab implementation due to the huge complexity of the lithographic process itself. The term "curse of dimensionality" is coined by Richard Bellman to describe the problem caused by the exponential increase in volume associated with adding extra dimensions to a (mathematical) space [50]. The number of predictors (dimensions) for variances in virtual fab lithography simulation or

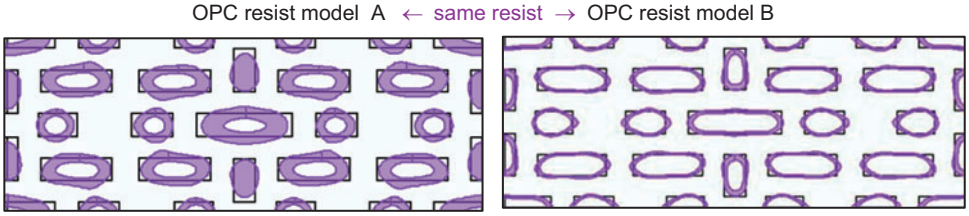


Figure 23 The difference of imaging resulting from using two OPC models (A and B), which are derived from different illumination schemes. The resist material used is the same for both OPC resist model [45].

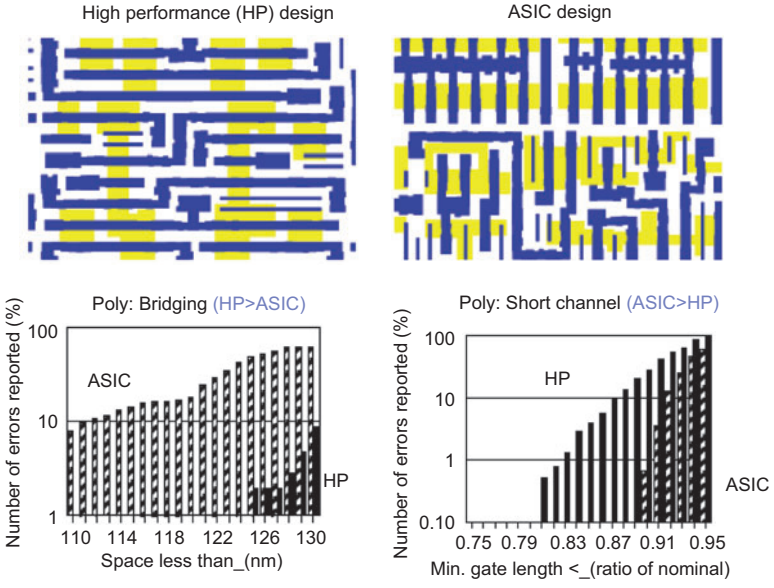


Figure 24 A LMA of two different poly designs, one for high performance (HP) and the other for ASIC. Owing to the design difference, the litho performance vs. ground rules yields different litho error distributions. For example, poly-bridging is less severe for HP design, but poly-short channel effect behaves in the opposite way.

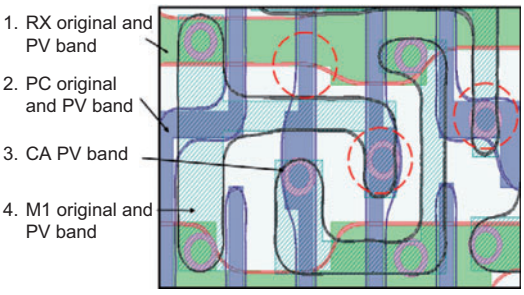


Figure 25 Litho-aware layout showing process variation bands overlaying on top of design layers illustrating the critical design hot spots.

optimization may cause a combinatorial explosion. We need to reduce the dimensions of the problem to break the curse and is frequently used in optimization problem and machine learning.

Therefore, the big question here is whether dimensional reduction is possible in lithography modeling. Theoretically, it is possible if, first, the problem can be divided into subdomains (spatial) to take advantage of parallel computing. Of course, the overhead in communication and stitching back all the domain solutions need to be tackled. This technique has been commonly used especially in full field application. Second, if the variances of the predictors are small, and somehow, there are correlations between them, then, a decomposition of the problem into a few strongest eigenvectors is possible. If the variance of each predictor is small, it is possible also to decompose into the first few terms of the Taylor expansion of the function. An early example of that is the so-called variational lithography model (VLIM) [51]. The defocused image at any depth of the resist are expanded into the Taylor series with the first term being the best focus image and the second term with a coefficient independent of the depth. The result is that all the images at different focuses can be evaluated at once, and thus, there is no need to build an extra OPC model at a different focus. Third, another approach is to use perform basis transformation through techniques like PCA [52] or reduced basis method [53]. This basically involves reducing the rank of the governing matrix through the transformation and prerunning a lot of time-consuming parametric variation calibration to construct new basis. It is our optimism that many more problems, especially when they can be described as a set of partial differential equations, can be handled in

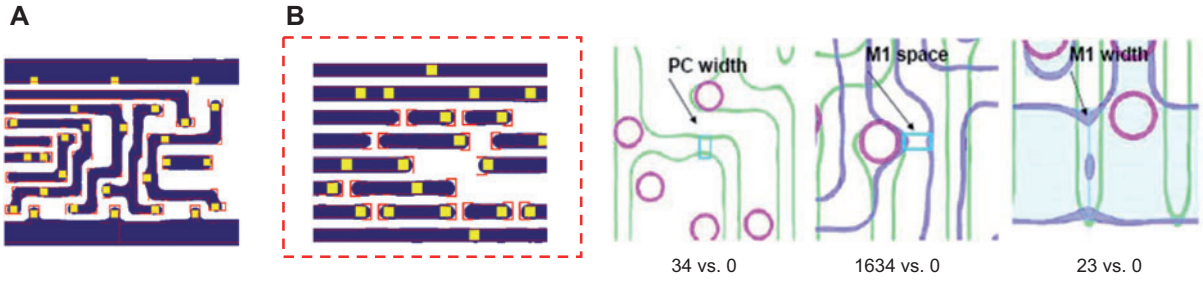


Figure 26 (A) Simplification of OPC due to unidirectional designs [47]. (B) Hot spot count for conventional vs. RDR showing reduction for RDR designs. The number stands for hot spot count for conventional designs vs. RDR designs.

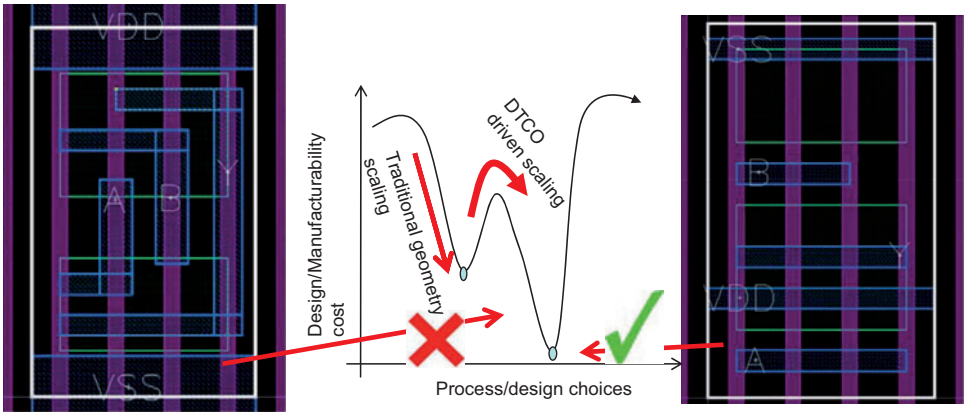


Figure 27 Illustration of the benefit of using computational lithography techniques when comparing unidirectional designs to bidirectional designs [48].

reduced dimension and hopefully significantly improving simulation run times by orders of magnitude.

7 Conclusion

In conclusion, we recognize the critical role of predictive modeling, software, and high-performance computing in semiconductor and nanotechnology research, development, and production. No matter what type of technologies are being adopted, modeling and model-based pattern correction are always required, and often, new modeling techniques are desired. In all cases, both highly rigorous models and resource efficient models are needed for different applications. The use of high-performance computing platform and efficient algorithms are unavoidable to achieve continued scaling. Ultimately, our goal is to accelerate the rate of discovery and time to implement new enabling technologies. Realizing this vision will require the active collaboration of funding agencies, universities, and industry. We believe that we can keep semiconductor scaling practical and vibrant well into the future.

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