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Light-Effect Transistor (LET) with Multiple Independent Gating Controls for Optical Logic Gates and Optical Amplification

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Modern electronics are developing electronic-optical integrated circuits, while their electronic backbone, e.g., field-effect transistors (FETs), remains the same. However, further FET down scaling is facing physical and technical challenges. A light-effect transistor (LET) offers electronic-optical hybridization at the component level, which can continue Moore's law to the quantum region without requiring a FET's fabrication complexity, e.g., physical gate and doping, by employing optical gating and photoconductivity. Multiple independent gates are therefore readily realized to achieve unique functionalities without increasing chip space. Here we report LET device characteristics and novel digital and analog applications, such as optical logic gates and optical amplification. Prototype CdSe-nanowire-based LETs show output and transfer characteristics resembling advanced FETs, e.g., on/off ratios up to $\sim 1.0 \times 10^6$ with a source-drain voltage of $\sim$1.43 V, gate-power of $\sim$260 nW, and a subthreshold swing of $\sim$0.3 nW/decade (excluding losses). Our work offers new electronic-optical integration strategies and electronic and optical computing approaches.

Keywords: light-effect transistor, Field-effect transistor, Moore's law, II-VI semiconductor, CdSe nanowire, optical logic gate, optical amplification, metal-semiconductor-metals

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INTRODUCTION

As basic electronics building blocks, a field-effect transistor's (FET's) primary switching function is widely used in both logic and memory chips. A typical FET is a three-terminal device consisting of source (*S*), drain (*D*), and gate (*G*) contacts—where the *S*-*D* conductivity is modulated to realize on and off states by applying a voltage or an applied electric field through *G* [1]. Although FETs have evolved structurally from early planar to their current 3D geometries in parallel with the continual shrinkage of its lateral size, the basic operating principle remains the same. This has led to ever greater fabrication complexity, and ultimately to challenges in gate fabrication and doping control [2–6]. Various new technologies, such as FinFETs [4, 7], and tunnel-FETs [8], have been developed in recent years to enable the continuation of Moore's law [9], but further development with current technologies are uncertain [10]. Other options are being explored as alternatives, which include semiconductor nanowire (SNW) based FETs [11–13], FETs comprised of 2D materials [14, 15], and FETs with sophisticated gate structures [16], such as multiple independent gates [5, 6] or a gate with

embedded ferroelectric material [17]. There is, however, no clear pathway for overcoming a FET's intrinsic physical limitations [18–20] dictated by its operation mechanism, such as random dopant fluctuations [3] and gate fabrication complexities [21], and no viable rival technology currently exists. We offer a competitive alternative with additional unique functionalities. The light-effect transistor (LET) is a two-terminal device composed of a metal-semiconductor-metal (M-S-M) structure, where each M-S junction serves as either the *S* or *D* contact, and the two contacts are separated by a semiconductor nanostructure-based channel. **Figure 1** contrasts SNW-based LET and FET structures to reveal the apparent structural simplicity offered by a LET—no physical gate is required. A LET's operation mechanism is distinctly different from a FET in two regards: (i) the *S-D* conductivity is solely modulated by light or an optical frequency electromagnetic field, which contrasts a FET's electrostatic control through an applied DC voltage, and (ii) current carriers are generated through optical absorption rather than by thermal activation of dopants. In other words, a LET employs optical gating based upon the well-known photoconductive mechanism [22] that has typically been of interest in photo-detection. Inherent advantages stem from a LET's simplistic architecture, which include (i) eliminating gate fabrication complexity, and (ii) avoiding difficulties with doping control. These attributes remove the two primary challenges or intrinsic limitations for down scaling conventional FETs to the quantum regime [23], and they offer the potential for reduced fabrication costs. While a LET's most basic application emulates a FET when it operates under one-beam illumination (as in a photo-detector), it offers functions not readily achievable by either a FET [24] or a photo-detector [25, 26], when it operates differently than a typical photo-detector (e.g., when responding to multiple independent light beams).

Light-induced electrical conductivity changes are a well-known phenomenon typically used for photo-detection. In fact, SNW devices structurally similar to our LET have been investigated as photo-detectors [25, 26]. At first glance, it may appear that a LET simply employs a photo-detector's switching function to emulate a FET. In reality, most photo-detectors lack desirable FET-like characteristics and are therefore unsuitable for LET use. It is therefore important to understand the differences between a photo-detector, LET, and FET to appreciate the LET's novelty. Photo-detection typically relies upon a p-n junction-based device, because it usually offers superior performance over a simpler M-S-M device based on the photoconductive mechanism. This arises from the M-S-M structure typically requiring a larger bias to drive carriers through the *S* region [1, 22]. Note that a p-n junction based photo-detector has a distinctly different I-V characteristic under illumination than a photoconductive-based one, and only the latter can offer a light I-V resembling that of a FET with gate voltage on. The photoconductive mode's disadvantage is eased through reduced device dimensions, as demonstrated by SNW-based photo-detectors [25, 26], and the LET application in this work. Its structural simplicity should provide further advantages at the genuine nanoscale. We note that photo-detector structures that are difficult to dope may also employ a M-S-M structure [1, 22].

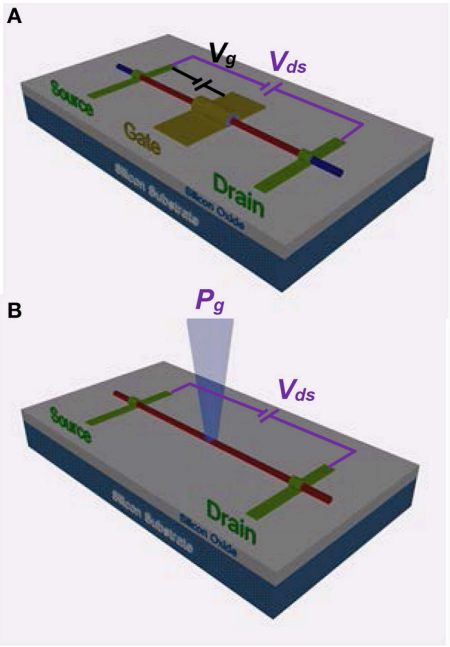

FIGURE 1 | Schematic comparison between a semiconductor-nanowire-based (SNW-based) field-effect transistor (FET) and a light-effect transistor (LET). (A) A FET is a three terminal device where the source-drain, *S-D*, current, is driven by an *S-D* voltage, and may be modulated through a gate (*G*) voltage applied through its *G* contact. **(B)** A LET is a two terminal device where the *S-D* current is modulated with one or multiple independently controlled light beams fused together through an optical combiner. Color codes are SNWs in red, *S* and *D contacts in green*, *G* contact in yellow, and the gate dielectric (under the *G* contact) is in bluish-gray. The blue-colored SNW tips past the *S* and *D* contacts indicate different FET doping types along the conducting SNW channel. It is assumed that these devices are resting upon an insulating substrate.

Therefore, a LET does not employ a new device structure or mechanism. Its novelty stems from its stringent electrical and optical characteristics that can (i) replicate the basic switching function of the modern FET with competitive (and potentially improved) characteristics, and (ii) enable new functionalities not available in modern FETs nor offered by conventional photo-detectors. While under single-beam illumination, a LET yields a high on/off ratio under optical gating, which resembles a FET under gate-voltage control or a photo-detector with high photoconductive gain. Despite this similarity, a LET should be characterized with a pertinent FET parameter known as "subthreshold swing," which measures how much gate action is required to turn the device on, and is normally not of interest in photo-detection applications. Under simultaneous multi-beam illumination, which is usually irrelevant for photo-detection, the multiple independent gating capability enables a LET to demonstrate previously unreported functions, such as optical logic (*AND* and *OR*) gates and optical amplification as an analog application. In contrast, multiple independent gating has been a very challenging task for FETs [6]. These unique functionalities are of great interest for optical computing and novel optical detectors. To summarize, LET novelty, in

comparison to photo-detectors, is two-fold. First, LETs are characterized electrically in a very different manner than photo-detectors, as photo-detectors are not typically explored for the electronic functions found in a FET. Second, LETs utilize their multi-beam response while a photo-detector does not. In comparison to FETs, a LET's gating mechanism is distinctly different from a FET's, which easily enables a LET's multi-gate capability, and allows a LET to offer functions beyond those in a typical FET. Furthermore, a LET's frequency response or switching speed is limited by the carrier transit time through its conducting channel. While this effect is shared with a FET, a FET's response is limited by its gate capacitance.

In this work, we employ readily available CdSe SNWs [27, 28] to demonstrate the LET concept and functions. We first characterize the material and devices, and then explore single-beam optical gating effects with different wavelengths and laser powers ($P_g(\lambda_g)$), manifested in both *output characteristic* ($I_{ds} - V_{ds}$) and *transfer characteristic* ($I_{ds} - P_g$). Finally, we operate the LET by applying multiple independent beams to demonstrate novel device functions, which are not achievable in conventional FETs, such as, optical logic gates and optical amplification.

MATERIALS AND METHODS

Nanowire Synthesis and Device Fabrication

CdSe nanowires were grown in a vertical array through gold-catalyzed chemical vapor deposition, as described elsewhere, [27] and were then dispersed in alcohol and drop cast onto a Si/SiO_2 chip, which consists of Si substrate coated with a 300-nm thick SiO_2 layer. After CdSe nanowires were dispersed onto a chip, a thin poly-methyl methacrylate (PMMA) layer was spin coated onto the chip, followed by electron-beam lithography to open channels at a nanowire's ends. Exposed PMMA was removed by developing the chip. Afterwards, the chip was transferred to a thermal evaporator (Cressington-308R) for indium metallization (30 nm), followed by lift-off in acetone to obtain a finished device. The other indium wire end was bonded to a large gold pad used for placement of a gold-coated electrical probe. The samples were air stabilized for at least a week prior to testing.

LET Characterization

Optical gating through $P_g(\lambda_g)$ has two basic control parameters: wavelength, λ_g, and power level, P_g, under one-beam CW operation, but it can be readily extended to other operation modes. For instance, multiple independent beams and pulsed illumination may be represented as $P_g(\lambda_{g1}, \lambda_{g2},\ldots,\lambda_{gN})$ and $P_g(t, \lambda_{g1}, \lambda_{g2},\ldots,\lambda_{gN})$, respectively. We fully characterize LET output and transfer characteristics under one-beam CW operation with two illumination conditions: (i) illuminating the center of the SNW with a focused CW laser ("focused illumination") with an optical diffraction-limited spot size at wavelengths of 633, 532, 442, or 325 nm; and (ii) illuminating the LET uniformly with "white light" from a halogen lamp ("uniform illumination").

The novel LET concept requires performance metrics for evaluation and comparison against FETs; thus, FET figures of merit are adapted, such as the two important input-output relationships: (i) "*output characteristics*" or I_{ds} vs. V_{ds} under a constant illumination condition $P_g(\lambda_g)$, which is equivalent to the FET's output characteristic under a constant gate voltage V_g; and (ii) "*transfer characteristics*" or I_{ds} vs. $P_g(\lambda_g)$ under a constant V_{ds}, which is equivalent to a FET's I_{ds} vs. V_g under a constant V_{ds}. A FET's gate voltage, V_g, is replaced by a LET's gate power $P_g(\lambda_g)$, which not only serves the same function of modulating *S-D* conductivity but also offers an avenue to achieve novel functions beyond those in a FET. Characteristic (i) is shared by both LET and photo-detection applications, while characteristic (ii) is required for LETs and FETs as a measure of turn-on energy, and in particular, for LETs to realize novel functions.

Optical and Electrical Measurements

I_{ds} vs. V_{ds} measurements were collected with a Keithley® 2401 low voltage sourcemeter® that was remotely operated with LabTracer v2.9 software via a GPIB connection. For currents below ∼1 nA, a Stanford Research System SR570 current pre-amplifier was used in conjunction with the Keithley®. Illumination sources consisted of halogen light, 532, 441.6, and 325 nm lasers ported through a Horiba LabRAM HR800 confocal Raman system with an internal 632.8 nm laser. Due to limited probe spacing for electrical measurements, all illumination sources were focused through a 50x long working distance (LWD) objective lens (*N.A.* = 0.50), except 325 nm, which went through a 10x MPLAN objective lens (*N.A.* = 0.25). Laser powers were limited to absolute powers of ∼3 μW, as measured on the sample side of the microscope lens, to avoid potential laser-induced material modifications. Laser powers were altered through a combination of a standard neutral density filter in the Raman system and an adjustable neutral density filter in the laser path. Laser powers were measured with a Thor Labs PM100D power meter, and six and ten averaged measurements were used for D1 and D2, respectively, to calculate average powers. The total power of the halogen light was estimated to be 69.1 μW.

Estimated Actual Power Absorbed

The laser spot size is estimated by the optical diffraction limit formula $1.22\lambda/N.A.$, where *N.A.* is the numerical aperture of the microscope lens. The fraction of the laser power actually absorbed is estimated by taking the ratio of the nanowire diameter to the laser spot size. The estimated ratios for the 632.8, 532, 441.6, and 325 nm lasers are 5.18, 6.16, 7.43, and 10.1% for a nanowire with an 80 nm diameter (device D1). For halogen illumination, the fraction of actual absorbed light is estimated using the ratio of the nanowire's cross section to the total illumination area. For the 50x LWD (10x MPLAN) objective lens, the illumination area is ∼279 (∼1450) μm^2. The ratio for the 80 nm wide/10 μm long nanowire (D1) is ∼3.2 10^{-6}, and the power estimation for light actually absorbed is ∼0.22 μW (which is comparable to that for the focused laser beam). All the illumination powers mentioned in the manuscript were applied powers, unless an actually absorbed power was explicitly stated.

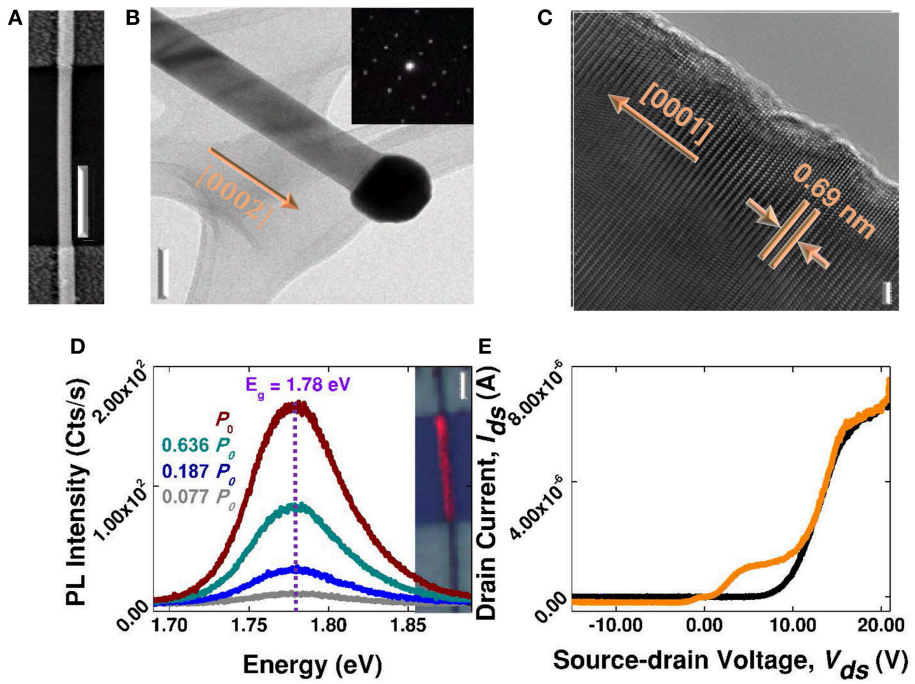

FIGURE 2 | LET characterization. (A) SEM image of a typical In-CdSe-In device (2 μm scale bar). **(B)** TEM (100 nm scale bar) with SAED inset, and **(C)** HRTEM image (2 nm scale bar) of a representative CdSe nanowire. The TEM results indicate single crystalline CdSe with well-ordered lattice plane spacing of 0.69 nm along the [0001] growth direction. **(D)** PL spectra obtained under 442 nm excitation at different powers (P_0 = 1.5 μW). Inset contains PL map overlaid upon an optical image of D1 (4 μm scale bar). **(E)** Source-drain current, I_{ds}, as a function of source-drain voltage, V_{ds}, under dark (black line), and halogen light illumination (orange line) conditions.

RESULTS

Nanowire and Device Characterization

Figure 2 provides material and device characteristics. **Figure 2A** displays an SEM image of a 10-μm-long CdSe SNW (device 1 or D1) with indium (In) contacts forming M-S junctions at each end. The uniform single-crystalline CdSe SNW was grown in wurtzite phase along the [0001] axis with a diameter of ∼80 nm, as revealed by the low magnification transmission electron microscopy (TEM) image in **Figure 2B**, with the selected area diffraction pattern (SADP) as inset, and **Figure 2C**'s high-resolution TEM (HRTEM) image showing a 0.69 nm inter-planar spacing. The gold catalyst at the SNW end (**Figure 2B**) suggests the vapor-liquid-solid growth mechanism [29]. The CdSe-SNW's laser-power-dependent photoluminescence (PL), **Figure 2D**, shows a strong emission peak at 1.78 eV that matches CdSe's bandgap energy [30]. The inset overlays a PL map upon an optical image to demonstrate relatively homogenous SNW emission, and by extension, homogenous material quality across the SNW channel. In **Figure 2E**, the output characteristic, S-D current I_{ds} vs. *S-D* voltage V_{ds}, is demonstrated for the device with and without light illumination using a halogen light, where illumination optically modulates or "gates" the electrical conductivity between dark ("off") and illuminated ("on") states. The I_{ds} vs. V_{ds} curves for these two states clearly resembles those of a FET's off and on states [1], respectively, especially when $V_{ds} < \sim 7$ V.

Output and Transfer Characteristic

Results for two devices, device 1 (D1) and device 2 (D2) with lengths of ∼10 and ∼5.5 μm and similar diameters (∼80 nm), are presented to illustrate general LET properties, and to demonstrate the potential for characteristic tuning and optimization. The two devices were fabricated in essentially the same way.

Device dark currents reveal negligible reverse bias current and rectification (diode-like behavior) under forward bias, e.g., **Figure 2E**. LET operation occurs under forward bias for both devices. Rectification is indicative of asymmetric In/CdSe contacts for both devices, where one M-S junction is close to ohmic and the other forms a Schottky contact [31]; large asymmetric contacts are desired as they drastically reduce the dark current or off state and thereby improve the on/off ratio. The Schottky barrier largely determines the turn-on voltage, $V_{D,on}$, which is ∼8 V for D1 and >21 V for D2. For instance, D2 shows nearly resistive behavior up to $V_{ds} = 21$ V with I_{ds} reaching only ∼15 pA, compared to D1's range from ∼1 nA to ∼4 μA over 1–21 V. The vast difference between the two devices might stem from a thin SeO_x layer ($x = 2$–3) [32] at the In/CdSe junction, although the details require further study. These results hint that dark or off state parameters can be controlled through M-S contact engineering.

Representative LET output characteristics are shown in **Figures 3A–D** for D1 and in **Figures 3E,F** for D2, respectively,

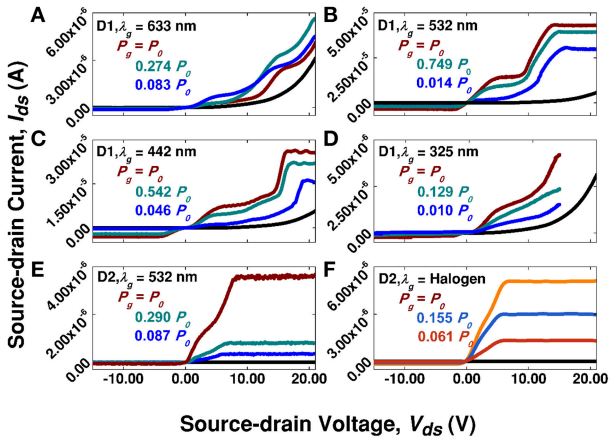

FIGURE 3 | LET output characteristics: Source-drain current, I_{ds}, as a function of the applied source-drain voltage, V_{ds} with varying gate power, P_g, and wavelength, λ_g, for two devices (D1 and D2). (A–D) are for D1 under 633, 532, 442, and 325 nm illumination with P_0 values of 1.40, 2.07, 2.38, and 2.25 μW, respectively, while **(E,F)** are for D2 under 532 nm and halogen excitation with respective P_0 values of 1.38 and 69.1 μW. The dark current is represented as black lines.

to exemplify how LET performance depends on the gate power/wavelength, illumination condition, and device variation. D1 exhibits two well-separated plateaus, respectively, starting at $V_{ds} \sim$ 4–5 and ∼14–18 V depending on the gate wavelength and power. For example, the second plateau's onset is at ∼14–15 V for 633 nm illumination but shifts to ∼16–18 V under 442 nm excitation. Two tunable plateaus can potentially offer two distinct, customizable on states. For D2, the first and second plateau are comparatively not well separated, and both 532 nm and halogen illumination have their first plateau at ∼2 V with respective power-dependent, second plateaus at ∼6–7.5 V (532 nm) and ∼5–5.75 V (halogen). Each plateau appears at respectively lower V_{ds} values than in D1, and because of the extremely low dark current, the long second plateau extends to the highest V_{ds} measured. For D1, the maximum on/off ratios typically occur at $V_{ds} < 5$ V, and vary from 10^2 to 10^4 depending on the gate power and wavelength. For instance, **Figure 3B** contains on/off ratios of $\sim 5 \times 10^4$ and $\sim 2 \times 10^4$ at $V_{ds} = 1.43$ and 4.95 V, respectively, when $P_g(532\,nm) \approx 2$ μW. The on/off ratios for D2 in **Figure 3E** are $\sim 1.0 \times 10^6$ and $\sim 1.1 \times 10^6$ at $V_{ds} = 1.43$ and 4.95 V when $P_g(532\,nm) \approx 2.6$ μW. When $P_g(halogen) \approx 69$ μW in **Figure 3F**, the on/off ratios are $\sim 6 \times 10^5$ and $\sim 1 \times 10^6$ at $V_{ds} = 1.43$ and 4.95 V, respectively.

Differences between D1 and D2 indicate that a LET's characteristics may be tuned and optimized through material and device engineering. A large M-SNW contact barrier is generally desirable for producing small off state currents over the operation range, and can be optimized to maximize the on/off ratio. Note that current levels for different "gate" wavelengths in **Figures 3A–D** showed considerable variations, which is fundamentally due to wavelength-dependent light-matter interaction effects, e.g., absorption and carrier dynamics, and illumination conditions, e.g., power density and beam size. This feature offers the unique LET advantage of flexibility in achieving gate functions compared to FETs.

The transfer characteristics allow extraction of several performance metrics. A FET's threshold gate voltage, V_T, and subthreshold swing, S, are respectively defined as the onset of a linear region in the $I_{ds} - V_g$ curve (i.e., voltage-controlled resistor behavior), and as the inverse linear slope on a semi-log $I_{ds} - V_g$ plot [4]. Their physical interpretations, respectively, are the gate voltage required for device operation and the gate voltage increment to induce an order of magnitude current change below V_T. A small S-value implies a small energy or power consumption to turn on or operate a FET. **Figure 4** contains D1's and D2's transfer characteristics, which in general, resemble a FET's transfer characteristics, e.g., increasing I_{ds} as the gate power P_g increases under constant V_{ds}, except a LET replaces V_g with P_g. A LET's threshold gate power, P_T, then, corresponds to the onset of a linear $I_{ds} - P_g$ region for a given λ_g, and S_{LET} is its subthreshold swing. Significantly, FETs usually do not operate in the "subthreshold swing" region, while a LET can employ this range to realize optical logic gates and for an interesting optical amplification effect. Taking D2's I_{ds} vs. P_g curves, **Figure 4E**, with $\lambda_g = 532$ nm as examples, typical P_T and S_{LET} values at V_{ds} =1.43 (4.98) V are, respectively, ∼30. (∼30.) nW, and ∼2.8 (∼2.5) nW/decade. For reference, advanced FETs have respective V_T and S parameters of 100–200 mV, and ∼70–90 mV/decade [33]. At $V_{ds} = 1.43$ V, $P_g = 0.11$ μW yields $I_{ds} \approx 0.35$ μA, and a LET dynamic power consumption of ∼0.5 μW, which is comparable to advanced FETs [34]. A LET's off-state energy consumption can be very low. For instance, the dark current is ∼1 pA at $V_{ds} = 1.43$ V with a corresponding off power consumption of ∼1.5 pW, which is lower than a FET of similar length [34]. Switching energy, or the amount of energy needed to go from off to on states, is a frequently quoted metric. Our current measurement system prevented a direct measurement of the switching time, although it may be reasoned that LETs can have lower switching energies than modern FETs. Note that a LET may be viewed as a FET without the gate, which means that a LET's switching time is limited by the carrier transit time rather than a FET's capacitive delay. Most direct band gap semiconductors possess room temperature carrier lifetimes on the order of 100 ps without an applied bias, where applying a bias, especially for a short conducting channel length, reduces the transit time by more quickly wiping out free carriers. Simple estimates based on D2's performance support lower switching energies in LETs. For example, even an assumed 100 ps delay time would yield a switching energy of 0.05 fJ/switch (0.5 μW × 100 ps) associated with the S-D current, and 0.01 fJ/switch (0.1 μW × 100 ps) from the optical gating action, which yields a total switching energy less than typical FET values of 0.1–1.0 fJ/switch [35]. The switching energy could be further reduced by reducing the channel length and optimizing the contacts.

Application Demonstrations

LET transfer characteristics are used to illustrate the underlying principles for a few important applications. D2's 532 nm illumination characteristics, **Figure 4E**, are re-plotted on a double log scale in **Figure 5A**, with only $V_{ds} = 1.43$ and 4.98 V shown

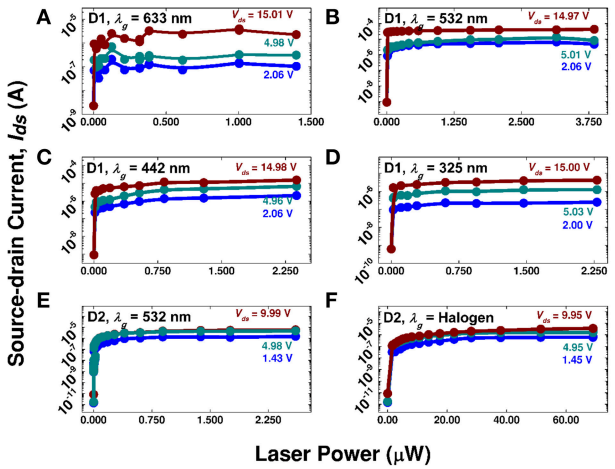

FIGURE 4 | LET transfer characteristics: Source-drain current, I_{ds}, as a function of laser power under different source-drain voltages, V_{ds}. (A–D) are for device D1, while (E,F) are for device D2 using the same conditions as in Figure 3.

for clarity, to more clearly portray the three major operating regions: super-linear (dark gray region), linear (medium gray), and sublinear/saturation (light gray). Different regions can offer different unique applications, as the examples highlighted below.

AND Logic Gate and Voltage Amplifier

Figure 5B demonstrates single beam illumination as a hybrid *AND* logic gate, which replicates the most basic FET logic function [1, 36], using electrical input A = V_{ds} and optical input B = P_g with output denoted as *AxB*. This is achieved when V_{ds} = 5V and P_g is modulated between 0 and 2.60 μW. One-beam operation could also act as a current source or voltage amplifier when operating in the output characteristic's saturation region, or even when utilizing a LET's two distinct on states (e.g., the first and second plateaus in **Figure 3B**) to realize two-level logic gate and voltage amplifier functions. Furthermore, two LET devices may be combined in parallel or series to respectively create universal *NOR* and *NAND* logic gates, as shown in Figure A1 in Supplementary Material with their corresponding truth tables.

Multi-Independent-Gate Capability

An important LET advantage is multi-independent-gate operation, where optical gates do not increase device dimensions. As an example, two-beam operation is demonstrated with independently controlled uniform illumination with halogen light and focused illumination from a 532 nm laser, denoted as P_{g1} and P_{g2}, respectively. Illumination by either individual light beam produces its corresponding transfer characteristics, e.g., I_{ds} vs. P_g in **Figure 4**, while two-beam illumination results in a 3D I_{ds} vs. (P_{g1},P_{g2}) plot (Figure A2-A in Supplementary Material). However, the two-beam response fundamentally reflects the linearity of the single-gate response shown in **Figure 5A**. To more clearly show this effect, a current enhancement factor R is introduced by converting $I_{ds}(P_{g1},P_{g2})$ to $R(P_{g1},P_{g2})$, where $R = I_{ds}(P_{g1},P_{g2})/[I_{ds}(P_{g1}) + I_{ds}(P_{g2})]$. Figure A1-A's in Supplementary Material data were converted with this definition and the corresponding R-values are displayed in **Figure 5C**'s contour plot. Using the LET response characteristics in **Figures 5A,C**, we demonstrate a few distinctly different LET functions that are not readily achievable using a FET, and can be realized with a single LET device. **Figures 5D–G** demonstrate dual-gate applications in three important $R(P_{g1},P_{g2})$ regions illustrated in **Figure 5C**. Additionally, the nonlinear response under 633 nm is also extended to two beam illumination with the addition of halogen light (Figure A3 in Supplementary Material).

Optical amplification

This occurs in **Figure 5A**'s super-linear or subthreshold swing region and yields a region where R >> 1, for instance, R ≈ 9–11 in **Figure 5C**. **Figure 5D** yields single beam induced currents of $I_{ds,\ 532nm} \approx 11$ nA (dark cyan line) and $I_{ds,\ halogen} \approx 37$ nA (orange line), while simultaneous illumination produced ∼11 times their sum with a $I_{ds,\ 2beam} \approx 525$ nA (royal blue line). If the laser beam is viewed as a weak optical signal to be measured, and the halogen light (∼1.6 μW) as a gate signal, an amplification factor of $m \approx 48$ is obtained. Optically-induced amplification of a LET's electronic signal replicates three-terminal phototransistor function, e.g., a bipolar transistor with a semi-transparent electrode [37], where a small base-emitter bias leads to photo-current amplification. This feature may find broad application in weak optical signal detection.

Optical AND logic gate

Results shown in **Figure 5D** can also be used for important optical logic operations, such as that in **Figure 5E**. Two individually applied optical gates, with inputs of *A* and *B*, respectively, produce two low current or off states represented as *(1,0)* or *(0,1)* in addition to the *(0,0)* off state (not shown for clarity). Only under simultaneous illumination does output *C* produce the on or *(1,1)* state. LET-enabled optical logic operations could lead to new optical or quantum computing approaches [38].

Optical summation

Sum operations can be realized in **Figure 5C**'s linear response region, e.g., R = 1, as illustrated in **Figure 5F**. In this figure, $P_{g1,\ 532nm}$ and $P_{g1,\ halogen}$ generate two independent signals of 2.00 and 0.32 μA, while simultaneous illumination produces a current of 2.43 μA or approximately their numerical sum. This region is convenient for producing multiple states, such as for memory devices.

Optical OR logic gate

Current saturation is achieved when R = ½, and can function as an optical OR logic gate, **Figure 5G**. When A = P_{g1}(532 nm) = 0.63 μW and B = P_{g2}(halogen) = 69.1 μW, individual illumination as (1,0) and (0,1) states or dual illumination as the (1,1) state all produce comparable I_{ds} values; all three on states contrast the off state with pA-level I_{ds} denoted as (0,0) (not shown for clarity). A single LET could perform more complex logic functions concurrently by combining V_{ds} control with dual optical gate ability, such as a three-terminal AND gate with

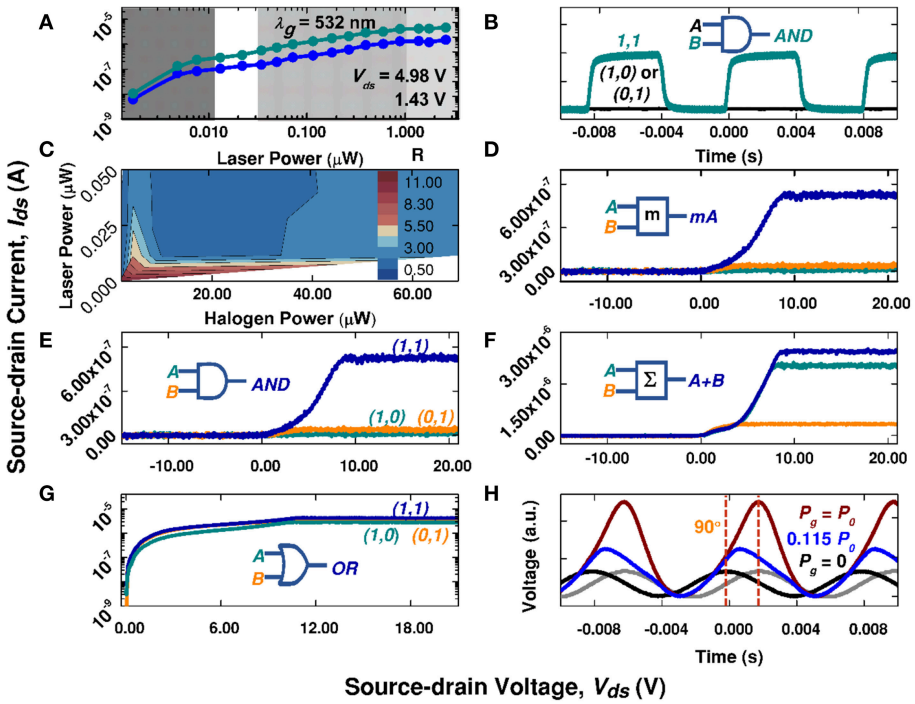

FIGURE 5 | Selected LET functionality demonstrations using D2. The axes are source-drain current, I_{ds}, vs. source-drain voltage, V_{ds}, except where noted otherwise. **(A)** Log-log plot of I_{ds} vs. P_g curves under 532 nm excitation with V_{ds} values of 1.43 and 4.98 V, where the three shaded areas are visual guides for distinguishing the super-linear (dark gray), linear (medium gray), and saturation (light gray) regions used to demonstrate LET behaviors and applications in **(B–H)**. **(B)** Optically modulated *AND* logic gate where $A = V_{ds}$ (5.00 V) and B = modulated P_g*(532 nm)* (up to 2.60 μW in amplitude). Dark line, $V_{ds} = 5$ V and $P_g = 0$; green line, $V_{ds} = 5$ V and P_g is modulated. **(C)** Various operation regions, according to ratio R (see text for definition), achievable with two-beam illumination under a fixed V_{ds} of 5.0 V. **(D)** A typical $R >> 1$ operation point, with P_{g1}*(532 nm)* = 2 nW and P_{g2}*(halogen)* = 1.57 μW, used as a demonstration of optical amplification; and **(E)** contains the same data as **(D)** but used as a demonstration of an optical AND gate instead. **(F)** A typical $R \approx 1$ operation point, with P_{g1}*(532 nm)* = 0.63 μW and P_{g2}*(halogen)* = 0.7 μW, used as a demonstration of a summation operation. **(G)** A typical $R \approx$ ½operation point, with P_{g1}*(532 nm)* = 0.63 μW and P_{g2}*(halogen)* = 69.1 μW, used as an optical *OR* logic gate. **(H)** LET operation under electrical modulation of $V_{ds}(t)$, while varying P_g (P_0 = 2.60 μW). The outputs $I_{ds}(t)$ were measured through a sampling resistor. The input is shown in gray (normalized to the black $P_g = 0$ output curve).

output AxBxC, or with simultaneous AND and OR gates with Ax(B+C) output. Truth tables for these logic operations and their proposed symbols are provided in the Appendix (Figure A4 in Supplementary Material). Significantly, a single LET can realize complex logic functions that typically require multiple FETs, but could require fewer devices to perform identical or enhanced functionality. Thus, LETs offer an additional pathway for achieving high device densities on a single chip.

Differentiator and Optically Gated Phase Tuner

Complementary to the above mentioned functions, LETs can also be used as a differentiator under zero or low P_g, and as a phase tuner as P_g is increased. **Figure 5H** shows the $I_{ds}(t)$ vs. $V_{ds}(t)$ curves for different P_g values, where $V_{ds}(t)$ is a sine wave modulation with an amplitude of 5.0 V and a DC offset to remove the negative portion. The $I_{ds}(t)$ curve exhibits a 90° phase delay with respect to $V_{ds}(t)$ when $P_g = 0$, which indicates that the device functions as a differentiator by converting a sine wave into a cosine wave; increasing P_g results in a tunable phase shift that gradually approaches zero, e.g., at $P_g = 2.6$ μW. This effect can be understood as changing the LET's impedance by varying the gate power.

DISCUSSION

LET Operation Mechanism

The $I_{ds} - V_{ds}$ curves in **Figure 3** may be understood qualitatively with the photo-conductivity model proposed by Mott and Gurney [22]. The first plateau could be associated with the "primary photoconductivity" which produces current as a result of photo-generated electrons and holes flowing through the nanowire under applied bias. A steady state condition is formed when just enough external carriers entering the nanowire through the electrodes replenish those leaving the device. Under single point illumination, the collection efficiency, Ψ, can be approximately described by:

$$\Psi = w \Big/ L\left(1 - e^{-x_0/w}\right), \tag{1}$$

where w is the carrier's mean free path (which is proportional to the applied field), L is the nanowire's length, and x_0 is the illumination site measured from the anode (cathode) when the carriers are electrons (holes). This theory suggests a continuous photocurrent increase from $V_{ds} = 0$ until saturation at a

sufficiently large V_{ds} to produce $w >> L$ and $\Psi \rightarrow 0.5$ (see Figure A5 in Supplementary Material for simulated Ψ vs. V_{ds} curves). Under uniform illumination, the collection efficiency is then:

$$\Psi = w \Big/ L \left[1 - w \Big/ L \left(1 - e^{-L/w} \right) \right]. \quad (2)$$

If all photons are absorbed, the sum of the collection efficiencies of both electrons and holes will yield a quantum efficiency, η_{QE}, defined as $I_{ph}/(eN_{ph})$, where I_{ph} is the photo-induced current, and N_{ph} is the number of absorbed photons. When current saturation occurs, $\eta_{QE} = 100\%$. For instance, absorbing 2 μW of 620 nm light with $\eta_{QE} = 100\%$ yields a 1 μA current. As V_{ds} approaches $V_{D,on}$, a major Schottky barrier reduction [31, 39] allows excess carriers to enter the nanowire through the electrodes, which then produce a drastic I_{ds} increase that allows $\eta_{QE} >> 1$. The detailed operation mechanism is likely much more complex than that described by the simple photoconductive mode, and deserves further investigation.

Significantly, the collection efficiency is expected to improve drastically at low V_{ds} with nanometer-length devices (Figure A5 in Supplementary Material), which should further reduce the static power consumption and provide lower V_{ds} than those demonstrated here. The maximum applied laser power is about 3 μW and corresponds to a power density of ∼0.60 W/mm^2, which is less than that delivered by an efficient light-emitting diode [40]. The gate power actually used is only about 10% of the applied power because the laser spot size is considerably larger than the nanowire diameter (see Section Materials and Methods for energy loss estimates). Reducing the beam size closer to the SNW's diameter could reduce P_g by at least a factor of 10 [41], and as is well established in FET devices, reducing the channel length can further reduce the required V_{ds} (Figure A5 in Supplementary Material). Enhanced efficiency and reduced energy consumption could significantly reduce thermal issues plaguing nanoscale FET-containing electronics devices. We note that FETs posses a thermal dynamic limit of $S \geq (kT/q)\ln(10) = 60$ mV/decade at 300 K, whereas for LETs, S_{LET} is extrinsic in nature through its dependence of w on the carrier density, which in turn depends on the defect density. Thus, S_{LET} can be significantly improved by shortening the conduction channel, perfecting the material quality, and by choosing materials with strong absorption.

Pathways to Further Miniaturization and Integration

LETs are also capable of quantum scale operation. A LET's structural simplicity removes potential obstacles that FETs face for further down scaling. A LET shares the same limit of a FET, that is, the nanostructure dimensions practically achievable, e.g., 1–7 nm for Si nanowires [42], but LETs do not require complex and sophisticated fabrication steps for physical gates and doping. In general, ballistic transport theory suggests that commercially viable currents could be achieved in quantum structures [43]. Quantum conductance, which limits 1-D ballistic transport, is given by $G = nG_0$, where $G_0 = 2e^2/h$ is the minimum conductance and n are integers representing quantized energy levels. This equation [44] yields a maximum quantum impedance for the conducting channel of $Z_0 = 1/G_0 = 12.9$ kΩ. The on-state energy consumption could be as low as ∼13 nW/LET when I_{ds} =1 μA, and the required minimal V_{ds} would only be 13 mV (not including the voltage drop over the S/M junctions). Given the highly localized nature of the 1-D energy density of states, LET conductivity is expected to be quantized, and thus, tunable using different photon energies.

Industry may employ at least two basic illumination modes in an integrated LET circuit depending on the application: (i) uniform, broad-area illumination over a high-density LET array with SNWs, or (ii) separated light beams directed to individual or small groups of LETs through, for instance, sharp fiber tips or nanoscale emitters embedded on the same chip. For either mode, multiple light sources of the same or different wavelength(s) and/or intensities can be combined into one beam but controlled independently.

CONCLUSION

In this work, we presented the LET concept as a drastically different approach for FET-based IC technologies by using an all optical, rather than a physical gate mechanism. A LET explores the well-known photoconductivity attribute of a semiconductor that is naturally and commonly used for photo-detection. Here, we demonstrate digital and analog applications typically only achievable with transistors, as well as, functions that FETs cannot achieve. Most significantly, the LET gate function can provide much greater flexibility than a FET, including tunable gate properties and multiple independent gates. Notably, a LET can continue Moore's law without the FET complications and limitations associated with gate fabrication and doping control through: (i) a simple device architecture to potentially reduce fabrication costs; (ii) feasible down scaling to the quantum level; (iii) efficient, multi-functional ability in a single device; and (iv) operation at low energy consumption, which negate thermal issues plaguing nanoscale electronics devices. The general LET operation principle is independent of a particular material system, thus, when applied to silicon, the existing silicon-based microelectronic and photonic technologies can be readily adopted by LET technology. The LET concept can also be extended to develop other light-effect devices.

AUTHOR CONTRIBUTIONS

YZ and WZ guided work at UNCC and UNO respectively. JM and YZ conducted the optical and electrical measurements and analyzed the data, SR grew the CdSe nanowires and fabricated the devices, and KW collected the TEM data and created the 3D schematics in **Figure 1**. YZ and JM wrote the manuscript. All authors have reviewed, edited, and commented on this manuscript.

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SUPPLEMENTARY MATERIAL

The Supplementary Material for this article can be found online at: http://journal.frontiersin.org/article/10.3389/fphy.2016.00008

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