CMOS-MEMS Oscillator Architecture and Phase Noise: A Mini-Review

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Over the past two decades, the advancement in microelectromechanical systems (MEMS) has been making headway in the development of miniaturized mechanical structures with integrated electronics. By adopting the existing layer in the complementary metal–oxide–semiconductor (CMOS) fabrication platform, the so-called "CMOS-MEMS" technology offers an intrinsic circuit-MEMS integration scheme, paving the way to realize monolithic micromechanical oscillators for frequency control and sensing applications. To enhance the functionality of the oscillator, it is cardinal to understand the secrets behind the resonator and circuit design techniques to generate high spectral purity signals. As the oscillator characteristics heavily depend on the resonator's motional parameters, the circuit configuration is determined in accordance with the post-CMOS processing technology and the mode shape of the resonator. In this mini-review, we attempt to summarize and appraise studies related to the design and optimization of CMOS-MEMS oscillators and to give directions for future researchers in terms of phase noise.

Keywords: CMOS-MEMS, resonator, oscillator, transimpedance amplifier, phase noise, nonlinearity

INTRODUCTION

Electronic oscillators are the most fundamental building block in almost any electronic system for a variety of applications such as frequency control (Achenbach et al., 2000) and environmental sensing (Bianchi et al., 2000; Walls and Gagnepain, 2002). In addition to traditional quartz resonator-based reference oscillators (Vittoz et al., 1988) and quartz crystal microbalance (QCM) sensors (Ferrari et al., 2006), miniaturized oscillators using microelectromechanical systems (MEMS) technology have been intensively studied in both academia and industry over the past two decades (Lavasani et al., 2011; Chance et al., 2014; Zaliasl et al., 2015; Naing et al., 2020; Kalia et al., 2021; Chang et al., 2022) to be used in demanding applications with size constraints. Among the existing MEMS oscillator fabrication approaches, the CMOS-MEMS technology is one of the most promising approaches to achieving the monolithic integration of mechanical resonators and electronic circuits (Xie et al., 2002; Dai et al., 2005; Chen et al., 2011; Li C.-S. et al., 2012; Chen et al., 2019; Valle et al., 2021). In this approach, MEMS mechanical structures can be formed from the back-end of line (BEOL) metal/dielectric (Verd et al., 2006; Li et al., 2012c; Li et al., 2015b; Liu et al., 2018) or the front-end of line (FEOL) polysilicon layers (Verd et al., 2005; Lopez et al., 2009) by removing predefined sacrificial layers, thereby eliminating the thermal budget constraints that are often encountered in other custom IC-MEMS integration processes (Fedder et al., 2008). Although the constituent materials of the CMOS-MEMS resonators are limited to the composite metals, dielectrics, and polysilicon, it still features great mechanical properties such as high-quality factor (Q) (Chen et al., 2012; Li et al., 2015a) and low-temperature coefficient of frequency (TCF) (Liu and Li, 2019), providing potential for being used in practical oscillator applications.

To make up an oscillator, the CMOS-MEMS resonator is connected in a positive feedback loop with a CMOS amplifier on the same chip (Verd et al., 2008). Such a monolithic integration scheme helps reduce the parasitic capacitance between the MEMS resonator and the amplifier, hence extending the available bandwidth of the amplifier and reducing the input-referred noise. According to the feedback oscillator theories, the Barkhausen stability criterion should be met: 1) the loop gain at the oscillation frequency equals unity, and 2) the phase delay in the oscillation loop should be equal to a multiple of 2π (Rhea, 2010). Despite the simplicity of the concept, implementing a high-performance CMOS-MEMS oscillator is not an easy task. There are several parameters to evaluate the overall performance of an oscillator, including the oscillation frequency, temperature stability, power dissipation, and phase noise. Since phase noise represents random fluctuations in the phase of the output signal (Rubiola, 2008), it should be kept as low as possible to enhance oscillator stability, which is critical for precision applications such as timing references and high-resolution sensors. However, the most challenging issue to achieve low-noise CMOS-MEMS oscillator is the high motional resistance (R_m) of the on-chip MEMS resonator. Although several energy transduction mechanisms including electrostatic (Li et al., 2015c), thermal-piezoresistive (Zope and Li, 2021), and capacitive-piezoresistive (Li C.-S. et al., 2013) have been explored in CMOS-MEMS technology, the electrostatic transduction is the most widely adopted scheme in resonator due to its simplicity. Since the typical transduction gap size from 400 to 1,000 nm is limited by lithographic limitations in 0.35 and 0.18 µm CMOS platforms (Li C.-S. et al., 2012; Chen et al., 2019), typical CMOS-MEMS resonator impedance lies in the MΩ range in previous reports even under high bias voltages (Liu et al., 2013). As will be shown in the next section, such a high impedance not only raises the design complexity and difficulty of the sustaining circuit but also contributes a significant portion to the phase noise. In addition to R_m, recent studies also confirm that the inherent nonlinearity in CMOS-MEMS resonators also plays a key role in the phase noise spectrum (Li et al., 2018). In order to make a breakthrough in the performance of existing CMOS-MEMS oscillators, it is crucial to understand the characteristics of the prior arts.

PHASE NOISE MODEL FOR COMPLEMENTARY METAL–OXIDE–SEMICONDUCTOR-MICROELECTROMECHANICAL SYSTEMS OSCILLATORS

To capture the important parameters that contributed phase noise in both MEMS resonator and CMOS circuit, an equivalent circuit model is depicted in **Figure 1A**. The circuit is divided into two stages where the first stage is a transimpedance amplifier (TIA) to convert the motional current i_m from the resonator to the corresponding voltage v_{TIA} and the second stage is a gain-boosting amplifier to provide an additional gain A to satisfy the Barkhausen criterion. Note that the transimpedance

gain should be in ohms rather than V/V. At the oscillation frequency f_o, the overall gain $R_A = R_{TIA} \cdot A$ should be greater than the equivalent resonator impedance Z_m and the overall feedback phase is $\varphi_{TIA} + \varphi_A + \varphi_{MEMS} = 2n\pi$. Considering a practical resonator with a certain nonlinear effect, Z_m is greater than R_m in a general case (Pardo et al., 2012). Based on this circuit, the phase noise of the oscillator can be expressed as

$$\mathcal{L}(f_m) = 10 \log \left\{ \frac{\left(4kTZ_m + \frac{\overline{i_n^2}}{\Delta f}Z_m^2\right)}{2\overline{V_{OUT}^2}} \left(1 + \left(\frac{f_o}{2Q_{\text{eff}} f_m}\right)^2\right) \right. $$
$$\left. + \left|\frac{\partial f_n}{\partial V_{OUT}}\right|^2 \frac{S_{An}(f_m)}{f_m^2} \right\} \qquad (1)$$
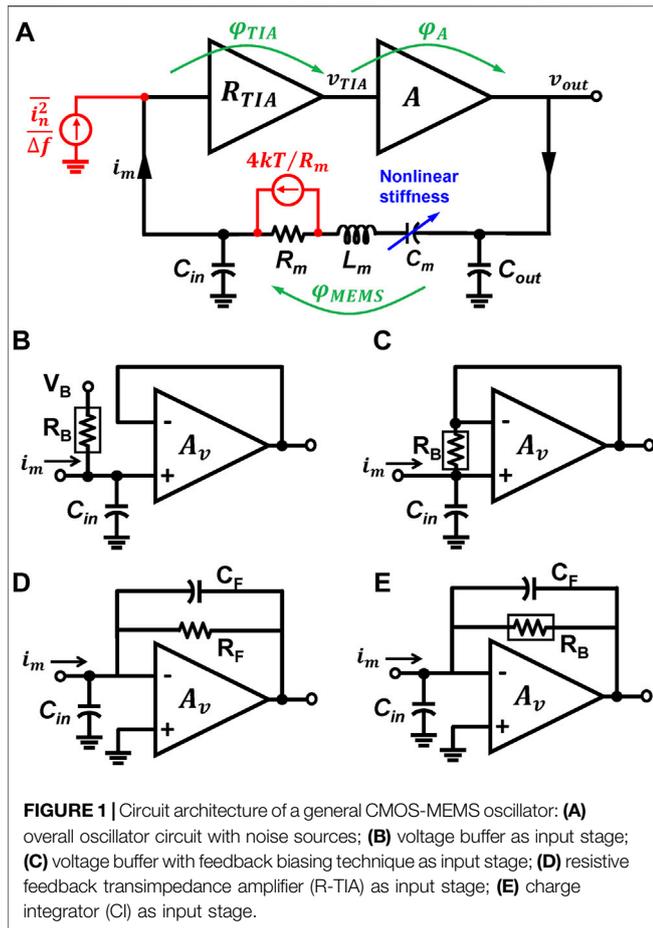
where k is the Boltzmann constant, T is the temperature in Kelvin, f_m is the offset frequency from carrier, $\overline{i_n^2}/\Delta f$ is the input-referred current noise density of the TIA stage, Q_{eff} is the equivalent quality factor of a nonlinear resonator, $|\partial f/\partial V_{OUT}|^2$ is a coefficient to describe the A-f effect of an nonlinear MEMS resonator (Li et al., 2018), and $S_{An}(f_m)$ is the amplitude noise spectrum of the oscillator. According to **Eq. 1**, the first component of phase noise is obviously from the Leeson effect and the second component is from the nonlinear amplitude-to-phase modulation (AM-PM) effect (Ward and Duwel, 2011).

From **Eq. 1**, it can be seen that the overall phase noise is dominated by the amplified circuit noise, $(\overline{i_n^2}/\Delta f) \cdot Z_m^2$. Since the typical values of Z_m lies in MΩ range for CMOS-MEMS resonators, the input-referred current noise of the TIA stage should be designed as low as possible to minimize this term. The resonator current noise $4kTZ_m$ is not significant for CMOS-MEMS devices. Therefore, some amplifier architecture, such as regulated-cascode TIA (Nabki et al., 2009), is not suitable for CMOS-MEMS oscillator design due to its high input-referred current noise. In addition to the impedance issue, when the resonator is driven at a large vibrating magnitude, the phase noise-folding caused by the AM-PM conversion can be described as an additive term, which dominates the close-to-carrier phase noise (Lee et al., 2011). To solve this issue, several design techniques such as high-stiffness driving (Su et al., 2015) and phase-feedback (Li et al., 2014) schemes were explored and implemented in CMOS-MEMS.

COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR-MICROELECTROMECHANICAL SYSTEMS OSCILLATOR ARCHITECTURE

Voltage Buffer as Input Stage

To compensate for the R_m of the CMOS-MEMS resonator, a high-transimpedance gain is desired. The simplest architecture uses a single capacitor to perform current-to-voltage conversion based on the charge integration over a sensing capacitor, C_{in}, as

FIGURE 1 | Circuit architecture of a general CMOS-MEMS oscillator: **(A)** overall oscillator circuit with noise sources; **(B)** voltage buffer as input stage; **(C)** voltage buffer with feedback biasing technique as input stage; **(D)** resistive feedback transimpedance amplifier (R-TIA) as input stage; **(E)** charge integrator (CI) as input stage.

resistor offers TΩ impedance, the input-referred current noise is low, which is favorable for low noise oscillator implementations. A subsequent voltage amplifier and phase compensation circuit are typically added after the voltage buffer to fulfill the oscillation condition. In addition to conventional all-pass filter-based phase compensation, a phase-locked loop (PLL) driving circuit is investigated in (Li H.-C. et al., 2012) to offer a wide-bandwidth frequency tracking. The implemented CMOS-MEMS PLL is used in mass sensor array systems (Wei and Lu, 2012), demonstrating a minimum mass resolution of only 23 pg by tracking the frequency shift over 12 MEMS resonant sensors.

Another voltage buffer-based sensing circuit was proposed by Verd et al., 2008 where the PMOS pseudo resistor is connected to the feedback loop, as shown in **Figure 1C**. Since the readout circuit is a unity-gain feedback buffer, the increase in C_{in} caused by the Miller effect and stray capacitance in the feedback path is negligible. The loop phase is compensated through the clever arrangement of the output impedance of the second stage amplifier and the parasitic capacitance at the driving port. In (Verd et al., 2008), a 6.32 MHz oscillator was demonstrated based on a very small CMOS-MEMS resonator (10 μm × 0.6 μm) with a huge R_m near 26 MΩ. In this example, we notice that the close-to-carrier phase noise appears $1/f^2$ trend. This behavior implies that the resonator is still operated under linear conditions since the quality factor is low (~100). On the other hand, the far-from-carrier phase noise of −94 dBc/Hz is limited by R_m, which can be explained by **Eq. 1**. When the oscillator is used in mass sensing applications, the combined mass resolution of 0.9 ag/Hz according to the frequency stability of 1.59 Hz for a typical averaging time of 1 s.

Resistive Transimpedance Amplifier as Input Stage

Series-resonant topology is often chosen in capacitive MEMS oscillators to minimize the degradation of the resonator's quality factor caused by the loading effect. A resistive feedback transimpedance amplifier (R-TIA) can be a suitable candidate for the sustaining circuit due to its low input impedance offered

shown in **Figure 1B**. To preciously control the value of C_{in} without affecting by the external parasitic capacitance, the resonator output is connected to a voltage buffer. An example is provided in (Li H.-C. et al., 2012) where the buffer is implemented by a two-stage source-follower circuit. Noted that the bias voltage of the input transistor is supplied through a high impedance pseudo resistor implemented with a subthreshold n-type MOSFET. In addition, as the pseudo

TABLE 1 | Phase noise comparison.

	Freq. (MHz)	Resonator type	Input stage topology	Resonator volume (μm³)	Phase noise (dBc/Hz)			
					10 Hz	100 Hz	1 kHz	Floor
Verd et al. (2008)	6.32	Cantilever	Volt. Buffer	4.5	NA	−35	−55	−94.3
Verd et al. (2013)	11	DETF	Charge Int.	3.52*	+8	−22	−50	−110
Li et al. (2013b)	1.2	DETF	R-TIA	8160*	−50	−80	−103	−110
Li et al., 2014; Li et al., 2015d	1.2	DETF	R-TIA	8160*	−64	−100	−112	−120
	1.2	DETF	R-TIA	8160*	−77[+]	−97[+]	−113[+]	−119[+]
Su et al. (2015)	4.22	Beam array	R-TIA	6938	−35	−65	−90	−121
Li et al. (2016a)	1.2	DETF	Charge Int.	8160*	−63	−93	−120	−122
Riverola et al. (2017)	0.55	Torsional	Charge Int.	NA	NA	−68.6	−103.9	−120.2
Sobreviela et al. (2017)	24	Torsional	Volt. Buffer	19.95	NA	−50[+]	−96[+]	−125[+]
Li et al. (2018)	1.2	DETF	Charge Int.	8160*	−80[+]	−97[+]	−112[+]	−127[+]

*The volume of the DETF only incorporates the two vibrating beams (ignore the coupling mass).
[+]Phase noise optimized by nonlinear phase feedback technique.

by the shunt-shunt feedback configuration, as depicted in **Figure 1D**. A typical R-TIA is composed of an operational amplifier, a resistive element R_F, and an optional damping capacitor C_F. In contrast to the voltage buffer-first topology described in the previous section, which runs the oscillator outside the 3-dB bandwidth of the entire sustaining circuit, in the series-resonant topology, the circuit bandwidth remains above the oscillation frequency. To design a high-frequency CMOS-MEMS oscillator, the R-TIA must feature a very high gain-bandwidth product to fulfill the oscillation condition, which consequently burns large dc power (Nguyen and Howe, 1999). As a result, the series-resonant topology is only compatible with those MEMS resonators with moderate R_m (mostly sub-MΩ) to offer reasonable phase noise under low power operation.

Although the application of series-resonant topology in CMOS-MEMS oscillator is difficult due to the relatively large R_m, there are still some vital examples (Li M.-H. et al., 2013; Li et al., 2015d; Su et al., 2015). In Li et al. (2015d), a 1.2 MHz CMOS-MEMS oscillator is designed with a 4-stage amplifier as the sustaining circuit. The circuit is designed based on a single-ended common-source amplifier to minimize the noise and power consumption. An overall tunable gain of 126–160 dBΩ, a maximum bandwidth of 20 MHz, and low input-referred noise of 0.6 pA/rtHz are obtained and burns only 1.3 mW, which is suitable for most CMOS-MEMS oscillator implementation in the MHz range. In this example, the phase noise of the oscillator at 1-kHz offset from the carrier is −112 dBc/Hz and at a 1-MHz offset is −120 dBc/Hz, resulting in an oscillator figure of merit (FoM) of −172.4 dB. Such a performance is comparable to other 2-chip MEMS oscillators (Lin et al., 2003) and MEMS-on-CMOS oscillators (Huang et al., 2008), which represents a breakthrough in monolithic CMOS-MEMS oscillator technology. Moreover, the same sustaining circuit is incorporated in an ultra-low-power oven-controlled oscillator design (Liu et al., 2016), which shows a maximum frequency variation below 4 ppm across a 90°C temperature span with sub-mW ovenization power.

With the development of CMOS-MEMS technology, novel resonators with deep sub-micron transduction gaps have been developed in recent years to further reduce R_m and thus be more advantageous in oscillator implementation. An example is given in Bhosale et al. (2021) where a clamp-clamp beam resonator with a submicron gap of 400 nm is configured with an R-TIA to form a compact active pixel based on the TiN-C post-CMOS process. The phase noise achieves -99.7 dB at 1-kHz offset and is lower than −120 dBc/Hz at 1-MHz offset thanks to the low R_m of the resonator, yielding decent frequency stability of 420 ppb for parallel sensing applications.

Charge Integrator as Input Stage

Charge integrator (CI) is a popular topology for emerging applications owing to its ultra-low noise behavior (Crescentini et al., 2013). A typical continuous-time charge integrator is composed of a feedback capacitor and a biasing resistor R_B, as given in **Figure 1E**. Once R_B is implemented by a diode-based pseudo resistor, the circuit behavior is dominated by the

capacitor. Unlike the voltage buffer topology discussed in the *Voltage Buffer as Input Stage* section, its integral gain is sensitive to the stray capacitance of the input node; the virtual short behavior at the input of the op-amp effectively eliminates the C_{in} at the input node to provide an accurate integral gain merely determined by C_F. In addition, as the R_B offers TΩ impedance, the input-referred current noise can be as low as sub-100 fA/rtHz (Crescentini et al., 2013), which is even better than the voltage-buffer topology.

As the charge integrator offers a phase shift of $\pi/2$, it needs additional phase compensation to satisfy the oscillation criteria (Riverola et al., 2017; Uranga et al., 2017). There are several ways to address the issue. The most common method is to build a Pierce-type oscillator circuit with the additional phase shift of the resonator and the input and output capacitors. In Verd et al. (2013), an 11-MHz Pierce CMOS-MEMS oscillator with a resonator feedthrough cancellation scheme is demonstrated with a dc-bias voltage of only 3 V. The circuit noise of 80 fA/rtHz is about 10X lower than an R-TIA shown in other works (Li et al., 2015d), which is the key to achieve low phase noise floor. The phase noise floor achieves −109 dBc/Hz is attributed to the large $R_m > 5$ MΩ and low output power of −17 dBm.

On the other hand, the integrator-differentiator TIA (ID-TIA) is also being explored in CMOS-MEMS oscillator applications (Li et al., 2016a; Li et al., 2016b). It is composed of two stages where the first stage is a CI, and the second stage is a differentiator. Since the differentiator provides an opposite phase shift to the CI, the overall phase shift through ID-TIA can be zero, thus offering a good condition for series-resonant oscillation. In Li et al. (2016a), and ultra-low-noise ID-TIA based 1.2 MHz 150 μW CMOS-MEMS oscillator demonstrates a good phase noise of −120 dBc/Hz at 1-kHz offset, which features a FOM of 190 dB with a resonator Q of 1900 and R_m of 2 MΩ. Such a FOM is superior to many MEMS oscillators designed in different technologies (Lin et al., 2003; Huang et al., 2008).

PHASE NOISE OPTIMIZATION OF COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR-MICROELECTROMECHANICAL SYSTEMS OSCILLATORS

Through the articles that have been discussed in the *Complementary Metal-Oxide-Semiconductor-Microelectromechanical Systems Oscillator Architecture* section, we observe large discrepancies in phase noise between distinct CMOS-MEMS oscillators, which can be attributed to differences in the dc-bias voltage, resonator volume, vibrating mode shape, and transduction gap size. To understand the reason behind this, the state-of-the-art CMOS-MEMS oscillators are tabulated in **Table 1** with their phase noise at different offsets. Apparently, the oscillators based on tiny resonators with small transduction gaps (Verd et al., 2008; Verd

et al., 2013) feature worse close-to-carrier phase noise compared to the other samples. This is because the tiny resonator elements usually have strong mechanical and bias-dependent nonlinearities (Chen et al., 2022), so the phase noise caused by the AM-PM effect is more pronounced. To overcome this issue, despite the conventional approach which operates the oscillator at lower carrier power to guarantee a linear MEMS operation, it has recently been demonstrated that the close-to-carrier phase noise can be effectively suppressed by increasing the excitation power as operating the MEMS resonator in the nonlinear regime (Yurke et al., 1995; Kenig et al., 2012). For a typical nonlinear Duffing resonator, there are two bifurcation points that present a steep phase-frequency slope to potentially minimize the AM-PM conversion coefficient. It has been shown theoretically and experimentally in a nanoelectromechanical oscillator system (Villanueva et al., 2013), that the phase noise of the nonlinear oscillator is greatly improved by operating the feedback phase closed to the lower bifurcation point.

For CMOS-MEMS oscillators, nonlinear AM-PM noise cancellation is firstly explored by (Li et al., 2014) based on a double-ended tuning fork resonator. By operating the oscillator at the lower bifurcation point through a variable-gain R-TIA, it can be observed that the phase noise changes drastically (close to 30 dB at 10 Hz offset) when the applied bias voltage is perturbed by only 0.1 V. The nonlinear phase noise cancellation leads to a great performance improvement, which is only 7 dB above the theoretical limit predicted by Leeson's model. In addition, this method is not restricted to a specific oscillator topology. The phase noise optimization is also achieved through an off-chip phase shifter circuit and supply voltage (V_{DD}) adjustment in other nonlinear CMOS-MEMS oscillator studies (Sobreviela et al., 2017; Uranga et al., 2017). In a recent study (Li et al., 2018), a 1.2 MHz 180 µW DETF oscillator combined with ultra-low-noise ID-TIA and nonlinear phase noise optimization technique achieves phase noise of -80 dB and -127 dB at 10-Hz and 1-MHz offsets, respectively, yielding a very competitive FOM of 189.3 dB.

CONCLUSION

CMOS-MEMS oscillator is an important technology to produce on-chip frequency references and oscillating sensors. In this review, we focused on the recent advances in CMOS-MEMS oscillators in terms of oscillator circuit topologies and phase noise performances. For high impedance resonators, it is reasonable to use voltage buffers and charge integrators as MEMS-circuit interfaces to take the advantage of their low input-referred noise. On the other hand, for low impedance resonators, resistive feedback TIA with moderate gain becomes a more suitable topology to avoid saturation and Q-loading effect. On the phase noise, it has been pointed out that the resonator impedance is the fundamental limit of the phase noise spectrum since the noise at the circuit input will be amplified by a factor of R_m to satisfy the oscillation criteria. Finally, the phase noise optimization based on phase feedback technique and nonlinear MEMS resonator operation is reviewed, which is a useful technique for oscillator stability improvements. So far, the CMOS-MEMS oscillators have been designed based on flexural mode resonators. The low stiffness characteristic becomes a fundamental limitation of frequency scaling. Thus, for future CMOS-MEMS oscillator designs, high-Q and high-frequency bulk-mode resonators (Chen et al., 2012) will be a potential solution to overcome current performance limitations.

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The author confirms being the sole contributor of this work and has approved it for publication.

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