frontiers | Frontiers in Energy Research

BRIEF RESEARCH REPORT
published: 29 June 2022
doi: 10.3389/fenrg.2022.922786

Common Ground Nine-Level Boost Inverter for Grid-Connected PV Applications

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The article discusses a nine-level switching capacitor-based common ground-type boost inverter for grid-connected photovoltaic applications. The proposed structure's direct connection between the negative terminal of the input source and the grid neutral eliminates leakage current. The proposed topology uses eleven switches, two diodes, and three switching capacitors to produce a double voltage boost with nine different voltage levels. Self-balancing switching capacitors eliminate the need for sophisticated independent control algorithms. The maximum voltage stress on one of the three capacitors equals the input voltage, while it is equal to half of the input voltage on the other two switched capacitors. The various modes of operation and capacitance calculation are discussed in depth. A comprehensive comparison with various nine-level topologies has been conducted in terms of total component count, total standing voltage, capacitor voltage, and approximate cost to demonstrate the proposed topology's benefits. A 400-W inverter prototype is constructed, and the experimental findings under various operating situations are reviewed.

Keywords: common ground, leakage current, GRID, transformerless, switched capacitor, photo voltaic, multilevel inverter

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Specialty section:
This article was submitted to Smart Grids, a section of the journal Frontiers in Energy Research

Received: *18 April 2022*
Accepted: *16 May 2022*
Published: *29 June 2022*

Citation:
Gopinath NP and Vijayakumar K (2022) Common Ground Nine-Level Boost Inverter for Grid-Connected PV Applications. Front. Energy Res. 10:922786. doi: 10.3389/fenrg.2022.922786

INTRODUCTION

Transformerless inverters (TLIs) for photovoltaic (PV) technology are gaining more popularity due to their simple structure, absence of a transformer, smaller size, reduced weight, and higher efficiency (Islam et al., 2015). The absence of a transformer removes the galvanic isolation between the PV array and the grid, resulting in leakage current through the parasitic capacitance between the PV source and the ground (González et al., 2008; Li et al., 2015). The undesirable leakage current causes many issues related to personnel safety, degrading the PV array characteristics, increased current harmonic distortion, and electromagnetic interference (Sonti et al., 2017). Therefore, it is mandatory to address the leakage current issue in the non-galvanic inverters. Thus, many approaches have been made based on novel topology derivations, new control algorithms, and different pulse modulation schemes to minimize the leakage current (Khan et al., 2020). From the topological point of view, the TLIs mitigate the leakage current using any one of the following methods: 1) decoupling the source from the grid, 2) connecting the grid neutral to the midpoint of the DC link, and 3) direct connection of the source negative terminal with the grid neutral, i.e., both connecting points are at ground potential (Kumari et al., 2021c). The TLIs derived from conventional full bridge (FB) can mitigate the leakage current by decoupling the source and load on the DC side (DC decoupling) or on the AC side (AC decoupling) during the freewheeling mode. In DC decoupling, the high switching stress of the H5 topology (Victor et al., 2008) is shared by two power switches employed on the positive and negative buses, known as the H6 topology (Islam and Mekhilef, 2015). An AC

decoupling topology with a highly efficient and reliable inverter concept (HERIC) is presented in Heribert et al. (2003). However, in DC and AC decoupling methods, the TLIs fail to minimize the leakage current completely. Other drawbacks of decoupling type TLIs include increased conduction losses caused by extra power switches and an inability to meet grid voltage without a boost converter at the input side. Another approach to confront current is to connect the mid-point of the DC link capacitor to the grid neutral, known as neutral point clamped (NPC) or active neutral point clamped (ANPC) topologies (Zhang et al., 2013; Debnath and Chatterjee, 2016; Kumari M. et al., 2021). The requirement of an additional front-end DC–DC boost power processing stage to meet the AC grid amplitude is the main disadvantage of NPC-type topologies. In both topologies (Siddique et al., 2020; Siwakoti et al., 2020), an active neutral point clamped (ANPC) inverter with boosting capability is presented. Since the output of these topologies is equal to the input, they still need front-end boost converters when dealing with the low-voltage paralleled PV string panels. An effective alternative to suppress the leakage current is common ground (CG)-type topologies, in which the common ground is shared between the source and the neutral side of the grid, eliminating the common mode voltage. A CG topology using switched capacitors as a virtual bus is presented in Gu et al. (2013). The switched capacitor is charged during the positive half cycle, and it acts as a virtual source during the negative half cycle to supply load. Like a conventional full-bridge inverter, the maximum output voltage of this topology is the same as the input DC-link voltage. Some five-level inverter topologies (Kadam and Shukla, 2017; Grigoletto, 2020; Sandeep et al., 2020) are presented based on the common ground type, but they are incapable of boosting the input voltage. By adding a switched or flying capacitor to the CG-type structure, the output voltage can be boosted while generating a multi-level output voltage waveform. The topologies of Vosoughi et al. (2020), Kumari et al. (2021b), and Mohamed Ali et al. (2022) overcome the shortcomings of the preceding topologies by boosting the output voltage to twice the input voltage with reduced power components. The topologies of Shaffer et al. (2018) and Sathik et al. (2021) have a CG-type structure with a voltage gain of 2 and 4, respectively. The main drawback of these topologies is the utilization of a higher number of power components to generate five-level output voltage. The topology Habib Khan et al. (2020) can operate in both buck and boost modes to provide the same AC output voltage, but it has a large inrush current. In recent times, a common ground structure with more output voltage levels and high voltage gain has attained more focus among researchers. Thus, a seven-level CG structure (Grigoletto, 2021) with triple voltage gain and nine-level CG type (Chen et al., 2022) with quadruple voltage gain is presented. To generate a seven-level output voltage, the topology (Grigoletto, 2021) requires a total component count of sixteen, which significantly increases the power loss. The high voltage stress of three times the input voltage on five switches and on one capacitor is the main issue with the topology (Chen et al., 2022). By keeping all the aforementioned issues in the literature, this article presents a new common ground type nine-level inverter (CG9-L) topology with the following features:

i) Single phase, nine-level output voltage with integrated boost operation (voltage gain is 2).
ii) The maximum voltage stress on capacitor is equal to the input voltage.
iii) The maximum voltage stress is equal to the output voltage.
iv) Inherent capacitor voltage balancing.
v) Leakage current is suppressed because of the common ground structure.

This article is presented as follows: the proposed topology and its operation followed by capacitance calculation, power loss calculation, result discussion, comparative analysis with other existing MLI's, and conclusion.

PROPOSED CG9-L INVERTER TOPOLOGY

The proposed CG9-L circuit configuration is depicted in **Figure 1A**. Structurally, CG-9L is composed of eleven power switches (S_1 to S_9 and S_B), three switched capacitors (C_1, C_2, and C_3), and two diodes (D_a and D_b). The power switch S_B is bidirectional, and all the other switches are unidirectional. The maximum voltage across the switched capacitor C_1 is equal to the input voltage and that across the remaining two capacitors, C_2 and C_3, is equal to half of the input voltage. The proposed CG9-L design has an inherent voltage balancing feature, and thus, it does not require any additional control circuits or algorithms to maintain the voltage balance of the capacitors. The neutral of the load side and the negative terminal of the input DC source are connected to the ground to establish a common ground feature.

Description of Output Levels

The nine output voltage levels, namely, 0.5 V_{in}, V_{in}, 1.5 V_{in}, 2 V_{in}, 0, −0. 5V_{in}, $-V_{in}$, −1.5 V_{in}, and −2 V_{in}, are synthesized, as shown in **Figures 1B–J**. Based on the different modes of operation, the switched capacitors C_1, C_2, and C_3 are charged and discharged during every switching cycle. The detailed description of all the operating states is given as follows:

First Positive Voltage Level

The first positive output voltage level of the proposed topology is generated by turning on switches S_1, S_4, S_6, S_9, and S_B to generate an output voltage level of $0.5V_{in}$, as shown in **Figure 1B**. The load current completes its path through S_B, the anti-parallel diode of switches S_6 and S_4, D_a, and the negative terminal of the source. Here, the output voltage is positive, and the load current is negative. The capacitors C_1 and C_3 get charged during this mode of operation, and it is expressed as follows:

$$\begin{cases} V_{C1} = V_{in}, \\ V_{C2} = V_{C3} = V_{in}/2, \\ V_O = V_{in} - V_{C2}. \end{cases} \quad (1)$$

Second Positive Voltage Level

The input source is directly connected to the load through the power switches S_1, S_7, and S_9, as shown in **Figure 1C**. The switches S_4 and S_6 are also turned on to charge the capacitors C_2 and C_3. Since all the three capacitors are connected in parallel with the input source

during this mode of operation, they get charged. The capacitor voltage and output voltage are expressed as follows:

$$\begin{cases} V_{C1} = V_{in}, \\ V_{C2} = V_{C3} = V_{in}/2, \\ V_O = V_{in}. \end{cases} \tag{2}$$

Third Positive Voltage Level

The power switches S_1, S_3, S_6, and S_B are switched ON, and output current is conducted. The input source and capacitor C_3 voltages are added together to deliver the load, as shown in **Figure 1D**. Here, the capacitor C_1 is charged, and C_3 is discharged. Here, the output voltage is written as follows:

$$\begin{cases} V_{C1} = V_{in}, \\ V_O = V_{in} + V_{C3}. \end{cases} \tag{3}$$

Fourth Positive Voltage Level

The proposed topology's maximum output voltage level is obtained by turning on the switches S_1, S_3, S_6, and S_7, as shown in **Figure 1E**. During this mode, the input source and capacitor voltages V_{C2} and V_{C3} cumulatively deliver the load requirement. The capacitor C_1 is connected in parallel with the input source and charged to V_{in}. The respective voltages are expressed as

$$\begin{cases} V_{C1} = V_{in}, \\ V_O = V_{in} + V_{C2} + V_{C3}. \end{cases} \tag{4}$$

Zero Output Level

In this mode, the power switches S_4, S_6, and S_8 are switched ON to provide a freewheeling path for the load. As shown in **Figure 1F**, the switches S_1 and S_9 are turned ON to charge the capacitors C_1, C_2, and C_3. The respective voltages are expressed as

$$\begin{cases} V_{C1} = V_{in}, \\ V_{C2} = V_{C3} = V_{in}/2, \\ V_O = 0. \end{cases} \tag{5}$$

First Negative Voltage Level

The switches S_2, S_4, S_6, and S_B are triggered ON to generate an output voltage level of $-0.5V_{in}$, and the respective voltage level is shown in **Figure 1G**. Here, the output voltage is negative, and the load current is positive. The current flows through S_B, the anti-parallel diode of switches S_6, S_4, C_1, and S_2, and the negative terminal of the source. The output voltage is expressed as follows:

$$V_O = -(V_{C1} + V_{C3}) = -V_{in}/2. \tag{6}$$

Second Negative Voltage Level

Here, the power switches S_2, S_4, S_6, and S_8 are triggered ON, and the respective current flow path is shown in **Figure 1H**. The capacitor C_1 is discharged to supply the load and it is written as follows:

$$V_O = -(V_{C1}) = -V_{in}. \tag{7}$$

Third Negative Voltage Level

The power switches S_2, S_4, S_5, and S_B are switched ON, and the load current is conducted. The capacitors C_1 and C_2 are discharging to deliver the load. The respective current flow path is shown in **Figure 1I**, and the output voltage is expressed as follows:

$$V_O = -(V_{C1} + V_{C2}) = -3V_{in}/2. \tag{8}$$

Fourth Negative Voltage Level

This mode of operation generates the negative maximum output voltage level, and the load current flow path is shown in **Figure 1J**. The power switches S_2, S_4, S_5, and S_8 are triggered ON. Here, all three capacitors are discharging to supply the load. The output voltage in this mode is written as

$$V_O = -(V_{C1} + V_{C2} + V_{C3}) = -2V_{in}. \tag{9}$$

CAPACITANCE CALCULATION

The three switched capacitors C_1, C_2, and C_3 in the proposed CG9-L topology are self-balanced using a series-parallel technique (Siddique et al., 2019). The selection of the capacitance value of these capacitors is important in switched capacitor topologies to achieve the desired output voltage waveform. Also, it involves ripple loss, size, and total cost of the inverter. The longest discharging time of capacitors has been used to calculate the capacitance value. The capacitances are estimated by considering the maximum allowable ripple limit of 10% of its maximum voltage (Liu et al., 2014). The time period to calculate the capacitance value is written using a typical nine-level output voltage waveform as follows:

$$t_1 = T_O/20\,;\ t_2 = T_O/10; t_3 = 3T_O/20\,; t_4 = T_O/5; t_5 = T_O/4;$$
$$t_6 = 3T_O/10; t_7 = 7T_O/20;\ t_8 = 2T_O/5;\ t_9 = 9T_O/20;$$

where T_o is the period of the output voltage waveform. The charge on the capacitors C_1, C_2, and C_3 at the resistive load during its LDC period is estimated as follows:

$$Q_{SC,\,C1-R} = 2\int_{t_1}^{t_5} I_{OL}(t)dt, \tag{10}$$

$$Q_{SC,\,C2-R} = Q_{SC,\,C3-R} = 2\int_{t_3}^{t_5} I_{OL}(t)dt. \tag{11}$$

The load current value for purely resistive load can be expressed as follows:

$$\begin{cases} \frac{V_{in}}{2}, & \frac{T_O}{20} \le t \le \frac{T_O}{10} \\ V_{in}, & \frac{T_O}{10} \le t \le \frac{3T_O}{20} \\ \frac{3V_{in}}{2}, & \frac{3T_O}{20} \le t \le \frac{T_O}{5} \\ 2V_{in}, & \frac{T_O}{5} \le t \le \frac{T_O}{4}. \end{cases} \tag{12}$$

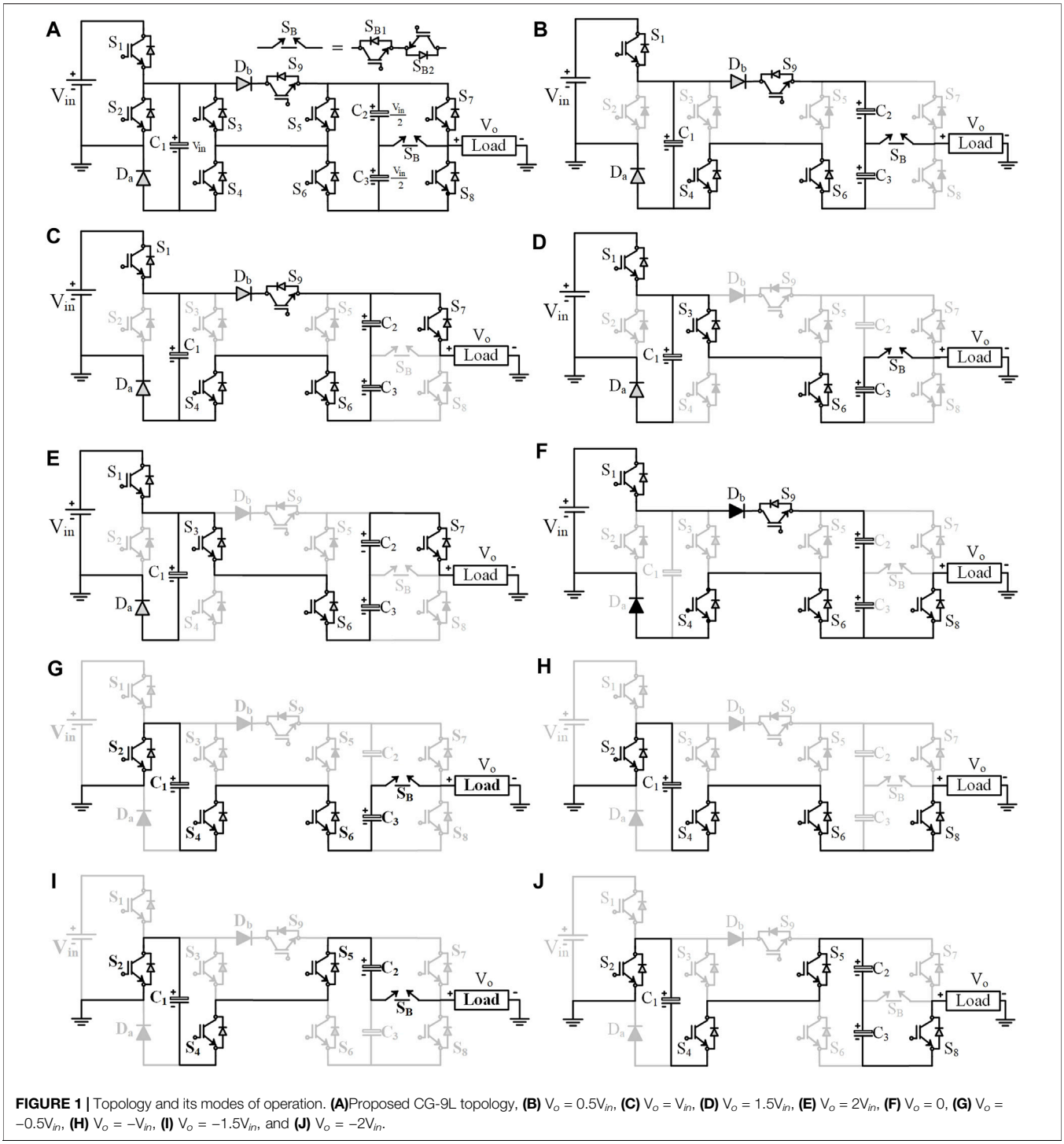

FIGURE 1 | Topology and its modes of operation. **(A)**Proposed CG-9L topology, **(B)** $V_o = 0.5V_{in}$, **(C)** $V_o = V_{in}$, **(D)** $V_o = 1.5V_{in}$, **(E)** $V_o = 2V_{in}$, **(F)** $V_o = 0$, **(G)** $V_o = -0.5V_{in}$, **(H)** $V_o = -V_{in}$, **(I)** $V_o = -1.5V_{in}$, and **(J)** $V_o = -2V_{in}$.

From **Equations 10** and **12**, the charge on the capacitor C_1 during resistive load is estimated as

$$Q_{SC,\,C1-R} = \frac{V_{in}\pi}{R_{LO}}. \tag{13}$$

The optimum value of the capacitance of capacitor C_1 when the load is purely resistive is calculated as

$$C_{1optm-R} \geq \frac{\pi}{R_{LO} \times k \times \omega}. \tag{14}$$

From **Equations 11** and **12**, the charge on the capacitors C_2 and C_3 during the resistive load is calculated as

$$Q_{SC,\,C2-R} = Q_{SC,\,C3-R} = \frac{7V_{in}\pi}{10R_{LO}}. \tag{15}$$

The optimum value of the capacitance of capacitors C_2 and C_3 when the load is purely resistive can be calculated as

$$C_{2\text{optm}-\text{R}},\ C_{3\text{optm}-\text{R}} \geq \frac{7\pi}{10R_{LO} \times k \times \omega}. \tag{16}$$

When the load is resistive-inductive (RL), the load current is expressed as follows:

$$I_{\text{OL}}(\text{t}) = \sin(\omega t - \theta). \tag{17}$$

At resistive-inductive (RL) loading conditions, the charge on the capacitance of capacitors C_1, C_2, and C_3 is calculated as

$$Q_{\text{SC, C1}-\text{RL}} = \frac{2I_{\text{mx}}}{\omega}\left[\cos\left(\frac{\pi}{10} - \theta\right) - \sin\theta\right], \tag{18}$$

$$Q_{\text{SC, C2}-\text{RL}} = Q_{\text{SC, C3}-\text{RL}} = \frac{2I_{\text{mx}}}{\omega}\left[\cos\left(\frac{3\pi}{10} - \theta\right) - \sin\theta\right]. \tag{19}$$

The optimum value of the capacitance of capacitors C_1, C_2, and C_3 during resistive-inductive (RL) loading can be written as follows:

$$C_{1\text{optm}-\text{RL}} \geq \frac{2I_{\text{mx}}}{k \times \omega \times V_{in}}\left[\cos\left(\frac{\pi}{10} - \theta\right) - \sin\theta\right], \tag{20}$$

$$C_{2\text{optm}-\text{RL}} = C_{3\text{optm}-\text{RL}} \geq \frac{2I_{\text{mx}}}{k \times \omega \times V_{in}}\left[\cos\left(\frac{3\pi}{10} - \theta\right) - \sin\theta\right]. \tag{21}$$

where I_{mx} is the maximum load current.

POWER LOSS CALCULATION

The total power loss of a topology depends on three losses: switching losses, conducting losses, and ripple losses. The overall efficiency can be estimated as

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{L-T}} = \frac{P_{OUT}}{P_{OUT} + P_{SL-T} + P_{CD-T} + P_{R-T}}, \tag{22}$$

where P_{SL-T}, P_{CD-T} , and P_{R-T} are the total switching loss, total conduction loss, and total capacitor ripple loss.

Switching Losses

When a power switch transition happens, i.e., when turn ON to turn OFF or turn OFF to turn ON, voltage and current overlapping occurs (Babaei et al., 2014). This causes loss in the power switch called switching loss. The switching losses of each power switch during turning ON (P_{S-on}) and OFF (P_{S-off}) are calculated as follows (Mohamed Ali et al., 2019):

$$P_{S-on} = N_{on}\int_0^{T_{on}} v(t) \times i(t) = \frac{V_{st-on} \times I_{st-on} \times T_{on} \times N_{on}}{6\text{T}}, \tag{23}$$

where $V_{st\text{-}ON}$, $I_{st\text{-}ON}$, and T_{ON} are the voltage across the switch when it is turned ON, current through the power switch during ON period, and turn ON time of the power switch.

$$P_{S-off} = N_{off}\int_0^{T_{off}} v(t) \times i(t) = \frac{V_{st-off} \times I_{st-off} \times T_{off} \times N_{off}}{6\text{T}}, \tag{24}$$

where $V_{st\text{-}OFF}$, $Is_{t\text{-}OFF}$, and T_{OFF} are the open circuit voltage of the switch when it is turned OFF, current through the power switch before turning OFF the power switch, and turn OFF time of the power switch, respectively. The total switching loss can be expressed as

$$P_{SL-T} = f \times \left(P_{S-on} + P_{S-off}\right). \tag{25}$$

Conduction Losses

The internal resistance of a power switch is the source of conduction losses when it is in conduction (Mohamed Ali et al., 2021). The total conduction loss is calculated using the equivalent circuit of the proposed CG9-L topology.

The conduction losses are estimated as

$$\begin{aligned}
P_{cd,1} &= (i_c + i_{L1})^2(R_{n-s} + R_{Esr} + R_{n-D}) + (i_{L1})^2(R_{n-s} + R_{Esr} \\
&\quad + R_{n-D}) + (i_{L11})^2(2R_{n-s} + R_{Esr}) + (R_{n-s} + R_{Lo}), \\
P_{cd,2} &= (i_c + i_{L2})^2(R_{n-s} + R_{Esr} + R_{n-D}) + (i_{L2})^2(R_{n-s} + R_{n-D}) \\
&\quad + (i_{L21})^2(2R_{n-s} + 2R_{Esr}) + (i_{L22})^2(R_{n-s} + R_{Lo}), \\
P_{cd,3} &= (i_c + i_{L3})^2(R_{n-s} + R_{Esr} + R_{n-D}) + (i_{L3})^2(4R_{n-s} + R_{Esr} \\
&\quad + R_{Lo}), P_{cd,4} = (i_c + i_{L4})^2(R_{n-s} + R_{Esr} + R_{n-D}) + (i_{L4})^2(4R_{n-s} \\
&\quad + 2R_{Esr} + R_{Lo}), P_{cd,-1} = (i_{L5})^2(4R_{n-s} + 2R_{Esr} + R_{Lo}), \\
P_{cd,-2} &= (i_{L6})^2(4R_{n-s} + R_{Esr} + R_{Lo}), P_{cd,-3} = (i_{L7})^2(4R_{n-s} \\
&\quad + 2R_{Esr} + R_{Lo}), P_{cd,-4} = (i_{L8})^2(4R_{n-s} + 3R_{Esr} + R_{Lo}),
\end{aligned} \tag{26}$$

where $R_{n-S}, R_{n-D}, and R_{Esr}$ are the on-state resistance of the switch, diode, and equivalent series resistance of capacitors. Also, i_c, i_{L1}-i_{L8}, i_{L11}, i_{L12}, i_{L21}, and i_{L22} are charging current and load currents during different output voltage levels. The average conduction loss for one complete cycle is calculated as

$$P^1_{cd,1} = 2 \times P_{cd,1}\left(\frac{t_2 - t_1}{T_O}\right);$$

$$P^1_{cd,2} = 2 \times P_{cd,2}\left(\frac{t_3 - t_2}{T_O}\right);\ P^1_{cd,3} = 2 \times P_{cd,3}\left(\frac{t_4 - t_3}{T_O}\right);$$

$$P^1_{cd,4} = 2 \times P_{cd,4}\left(\frac{t_5 - t_4}{T_O}\right);\ P^1_{cd,-1} = 2 \times P_{cd,-1}\left(\frac{t_{11} - t_{10}}{T_O}\right);$$

$$P^1_{cd,-2} = 2 \times P_{cd,-2}\left(\frac{t_{12} - t_{11}}{T_O}\right);\ P^1_{cd,-3} = 2 \times P_{cd,-3}\left(\frac{t_{13} - t_{12}}{T_O}\right);$$

$$P^1_{cd,-4} = 2 \times P_{cd,-4}\left(\frac{t_{14} - t_{13}}{T_O}\right).$$

The total conduction loss is estimated as

$$\begin{aligned}
P_{CD-T} &= P^1_{cd,1} + P^1_{cd,2} + P^1_{cd,3} + P^1_{cd,4} + P^1_{cd,-1} + P^1_{cd,-2} + P^1_{cd,-3} \\
&\quad + P^1_{cd,-4}.
\end{aligned} \tag{27}$$

Capacitor Losses

The difference in voltage between the input DC source and the voltage across the capacitor causes capacitor ripple loss. The ripple voltage can be estimated as follows:

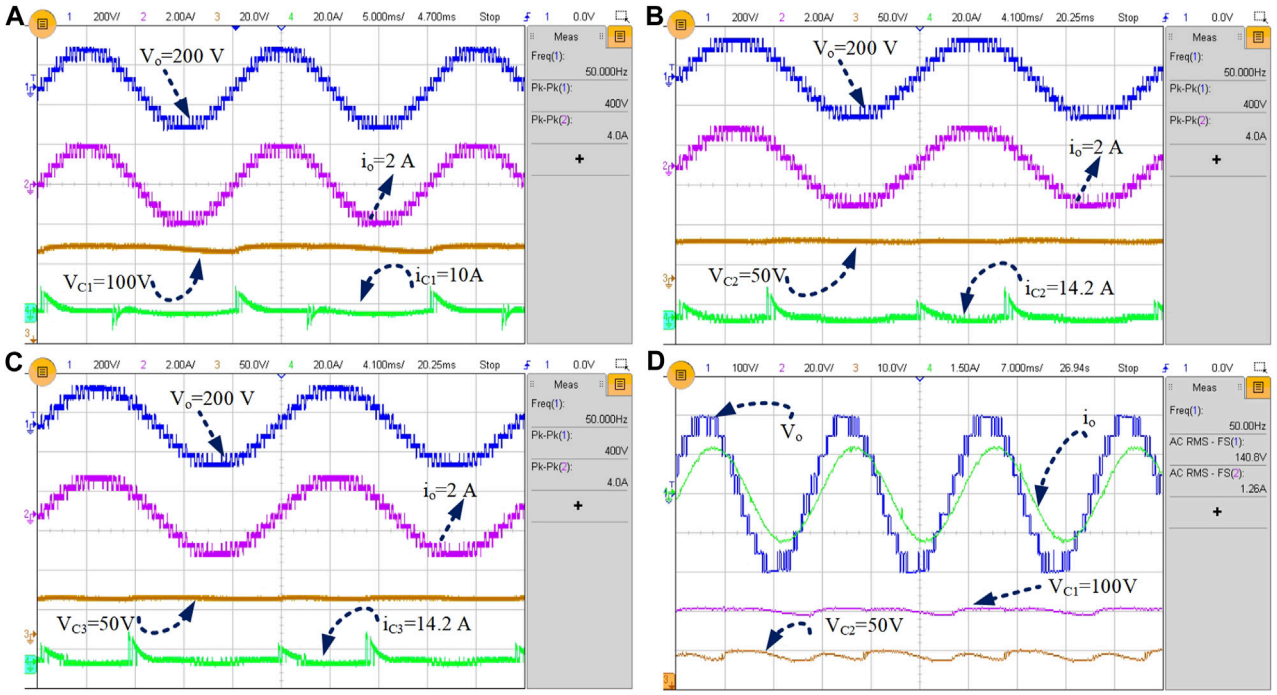

FIGURE 2 | Steady-state operating condition. **(A)** Experimental results of output voltage, load current, voltage across capacitors C_1, and capacitor current i_{c1} at R = 100 Ω. **(B)** Experimental results of the output voltage, load current, voltage across capacitors C_2, and capacitor current i_{c2} at R = 100 Ω. **(C)** Experimental results of output voltage, load current, voltage across capacitors C_3, and capacitor current i_{c3} at R = 100 Ω. **(D)** Experimental results of output voltage, load current, voltage across capacitors C_1, and C_2 at Z_2 = 100 + j100 Ω.

$$\Delta V_C = \frac{1}{C}\int_{t_s}^{t_e} i_c(t)\,dt, \tag{28}$$

where t_s-t_e is the start and end time duration of the longest discharge of the capacitor.

The ripple loss can be calculated (Ponnusamy et al., 2020) as

$$\Delta V_{C1} = \frac{I_{mx}}{\pi \times f \times C_1}\left[\cos\left(\frac{\pi}{10}-\theta\right)-\sin\theta\right], \tag{29}$$

$$\Delta V_{C2} = \Delta V_{C3} = \frac{I_{mx}}{\pi \times f \times C_{2/(3)}}\left[\cos\left(\frac{3\pi}{10}-\theta\right)-\sin\theta\right]. \tag{30}$$

The total capacitor ripple loss can be calculated as follows:

$$P_{R-T} = \Delta V_{C1} + \Delta V_{C2} + \Delta V_{C3}. \tag{31}$$

The total loss of the proposed CG9-L can be calculated as follows:

$$P_{L-T} = P_{SL-T} + P_{CD-T} + P_{R-T}\,. \tag{32}$$

RESULT DISCUSSION

The 400-W experimental prototype of the proposed CG-9L inverter is built in the laboratory using G60N100 IGBT switches, HCPL-3120 drivers, 1000 µF capacitors, Texas Instrument TMS320F28379D digital controller launchpad, and RL load, and its performance is analyzed under various steady-state and dynamic conditions. The switching frequency of the proposed inverter topology is 2.5 kHz. An input voltage of 100 V and load combinations of 100 Ω, 50 + j100 Ω, and 100 + j100 Ω were chosen while analyzing the performance of the proposed topology. The steady-state performance of a proposed topology has been analyzed by using a resistive load of 100 Ω, and the obtained experimental results of the output voltage, output current, and voltage across the capacitors are shown in **Figures 2A–C**. It is observed that the output voltage is 200 V while applying a 100 V input, which verifies the boosting ability of the proposed topology. The steady-state operating condition at a series resistive-inductive load of R = 100 and L = 100 mH with a power factor of 0.95 is also tested, and the results are shown in **Figure 2D**. The rms value of load current is 1.26 A, and the voltage across capacitors C_1 and C_2 is 100 and 50 V, respectively. The dynamic operating conditions such as input change, load change period, and variations in modulation index values have been checked. The experimental results of an output voltage that varies from 160 to 200 V and an output current that varies from 1.5 to 1.85 A when the input voltage is changed from 80 to 100 V are shown in **Figure 3A**. The load is changed from Z_1 = 50 + j100Ω to Z_2 = 100 + j100Ω to test the dynamic behavior. The output voltage is maintained

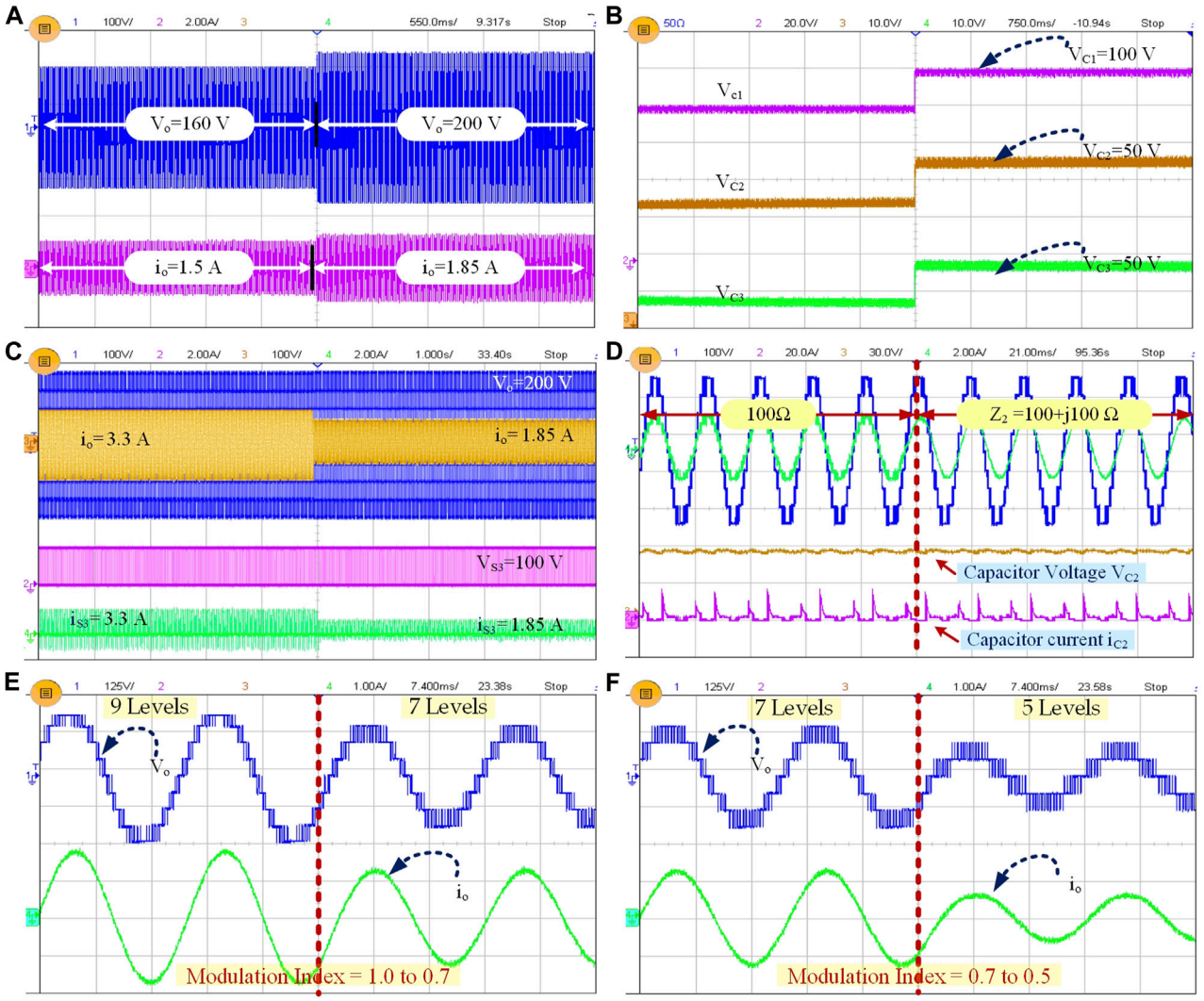

FIGURE 3 | Dynamic operating condition. **(A)** Experimental results of output voltage and load current during step input change. **(B)** Experimental waveform of capacitor voltages V_{C1}, V_{C2}, and V_{C3} during step input change. **(C)** Experimental results of output voltage, load current, voltage, and current of switch S_3 during the load change period Z_1= 50 + j100 Ω to Z_2= 100 + j100 Ω. **(D)** Experimental results of output voltage, load current, voltage, and current of capacitors C_2, during the load change period R = 100 Ω to at Z_2 = 100 + j100 Ω. **(E)** Experimental results of the output voltage and load current during modulation index variations 1.0 to 0.7. **(F)** Experimental results of the output voltage and load current during modulation index variations 0.7 to 0.5.

at 200 V constantly, and the load current changes from 3.3 to 1.85 A. The corresponding results are shown in **Figure 3C**. **Figure 3D** shows the output voltage, current, capacitor voltage V_{C2}, and capacitor current i_{C2} as the load is changed from R = 100 Ω to Z_2 = 100 + j100 Ω. The waveform shows that the capacitor voltage remains stable when the load changes, verifying the capacitor's self-voltage balancing ability. Furthermore, the change in modulation index values has also been analyzed, and the respective waveforms are shown in **Figures 3E,F**. The modulation index values are changed from 1 to 0.7 to 0.5. When the modulation index is 1, all nine voltage levels have been obtained. But when it is 0.7 and 0.5, the levels of output voltage are decreased to seven levels and five levels, respectively. During all these dynamic analyses, the capacitor voltages are maintained constantly with allowable ripple, confirming the self-balancing of capacitors. The inrush current that arises due to the direct parallel connection between the input source and the switched capacitor is reduced by the high impedance path due to the incorporation of an inductor of 33 uH during experimentation. In the MATLAB/Simulink, a power loss of ~10.9 W is obtained, whereas in the experiment, it is 15.4 W. The experimental efficiency is 96.2 % at ~400 W, which is close enough to the simulation efficiency (97.3 %). **Table 1** shows the power loss and efficiency during different loading conditions. The maximum simulation efficiency of 98.4% is achieved at ~200 W with unity power factor, as shown in the simulation and experimental efficiency comparison in **Figure 4**.

TABLE 1 | Power loss and efficiency of the proposed topology.

Power loss	CG-9L topology	
	@ 0.85 Power factor	@ 0.95 Power factor
Switch S_1	0.777	0.441
Switch S_2	0.24	0.138
Switch S_3	0.233	0.135
Switch S_4	0.652	0.338
Switch S_5	0.131	0.075
Switch S_6	0.569	0.33
Switch S_7	0.281	0.153
Switch S_8	0.113	0.075
Switch S_9	0.312	0.161
Switch S_B	0.593	0.323
Diode D_a	0.758	0.413
Diode D_b	0.461	0.237
Capacitor C_1	1.35	0.671
Capacitor C_2	0.28	0.171
Capacitor C_3	0.28	0.171
Total losses (W)	7.03	3.83
Output power (W)	288 W	181 W
Efficiency (%)	97.6	97.9

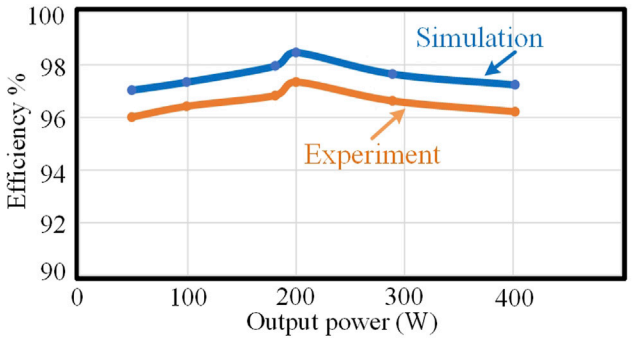

FIGURE 4 | Efficiency curve.

COMPARATIVE ANALYSIS WITH OTHER EXISTING MLI'S

The merits of the proposed CG9-L topology in comparison with other recent 9-L topologies are listed in **Table 2**. The comparison is carried out on the basis of the number of components, N_{sh}—no. of switches, N_{dv}—no. of drivers, N_d—no. of diodes, N_{cp}—no. of capacitors, T_{cc}—total component count, $T_{c\text{-}L}$—number of components counts per level, total standing voltage ($TSV_{p.u.}$), cost function, negative level generation, efficiency, and approximate total cost.

i) The total component utilization ratio of the proposed topology is 2.9, which is less than all remaining topologies except the topologies presented in Iqbal et al. (2021) and Chen et al. (2022). It shows that the CG9-L topology uses minimum power components to produce higher output voltage levels. Despite having a lower component utilization ratio, the voltage stress on some of the switches is high, which is equal to four times the input voltage in topologies (Iqbal et al., 2021; Chen et al., 2022). The total component utilization ratio is calculated as follows:

$$T_{C-L} = \left(N_{sh} + N_{dv} + N_d + N_{cp}\right)\Big/N_L. \tag{33}$$

ii) Even though the topologies presented in Taghvaie and Adabi (2018) and Mohamed Ali et al. (2021) have a lower total standing voltage per unit, it employs more power components than the proposed topology, which increases the total power losses and reduces its efficiency.

iii) Next, the ratio of the total capacitor voltage to the maximum output voltage V_{c-T}/V_{0-mx} is compared. The proposed topology uses three switched capacitors with a total capacitor voltage of $V_{o\text{-}mx}$, which is less than the topologies presented in Nakagawa and Koizumi (2019), Dhara and Somasekhar (2021), Sathik et al. (2021), and Chen et al. (2022) and equals the topologies presented in Zeng et al. (2017) and Mohamed Ali et al. (2021). Despite the low capacitor voltage ratio of the topologies in (Hinago and Koizumi, 2012; Taghvaie and Adabi, 2018; Sandeep, 2019; Iqbal et al., 2021; Jakkula et al., 2022), the common ground feature is absent. Furthermore, the component counts are

TABLE 2 | Comparison with other recent 9L topologies.

Reference	N_{sh}	N_{dv}	N_d	N_{cp}	T_{cc}	$T_{c\text{-}L}$	TSV p.u.	$V_{c\text{-}T}/V_{o\text{-}mx}$	C_f with α= 0.5, 1, and 1.5			CGT	HB	η (%)
									0.5	1	1.5			
Hinago and Koizumi, (2012)	13	13	0	3	29	3.2	6.25	0.75	32.1	35.3	38.4	No	Yes	Not available
Zeng et al. (2017)	10	10	4	4	28	3.1	7.75	1	31.9	35.8	39.6	No	Yes	93%@500W
Taghvaie and Adabi, (2018)	19	19	0	3	41	4.9	4.55	0.75	43.3	45.5	47.8	No	No	91.7%, not available
Nakagawa and Koizumi, (2019)	12	11	0	3	26	2.9	6	1.25	29	32	35	No	No	96%@50W
Sandeep et al. (2019)	12	12	0	2	26	2.9	5.25	0.75	28.6	31.3	33.9	No	No	Not available
Iqbal et al. (2021)	10	10	1	2	23	2.6	5.75	0.75	25.9	28.9	31.6	No	No	94.4 %@500W
Mohamed Ali et al. (2021)	10	10	4	3	27	3	4.75	1	29.4	31.8	34.1	No	No	97%@500W
Sathik et al. (2021)	11	9	8	4	32	3.5	5.5	1.5	34.8	37.5	40.3	No	No	94.7%@500W
Dhara and Somasekhar, (2021)	12	11	2	4	29	3.2	8	1.5	33	37	41	No	Yes	95%@500W
Chen et al. (2022)	9	9	3	4	25	2.8	5.25	1.25	27.6	30.3	32.9	Yes	No	95.2%@1kW
Jakkula et al. (2022)	15	13	0	3	31	3.4	5.75	0.75	33.9	36.8	39.6	No	No	96%@500kW
Proposed	11	10	2	3	26	2.9	5.5	1	28.8	31.5	34.3	Yes	No	96.2%@400W

TABLE 3 | Cost comparison of the proposed topology with other recent topologies.

Device	Part number	Rating	Unit price [a] ($)	Hinago and Koizumi, (2012)	Zeng et al. (2017)	Taghvaie and Adabi, (2018)	Nakagawa and Koizumi, (2019)	Sandeep et al. (2019)	Iqbal et al. (2021)	Mohamed Ali et al. (2021)	Sathik et al. (2021)	Dhara and Somasekhar, (2021)	Chen et al. (2022)	Jakkula et al. (2022)	Proposed
MOSFETs	STP30NF20	200 V, 30 A	2.82	9	—	16	4	3	2	1	2	—	2	11	2
	IRFB4137PBF	300 V, 40 A	4.50	—	3	—	6	9	4	9	7	8	2	—	8
	RB-IRG6I330UPBF	300 V, 28 A	3.28	—	—	3	—	—	2	—	—	—	—	—	—
	RB-IRG4BC30KPBF	600 V, 28 A	3.62	—	—	—	—	—	—	—	—	—	1	—	1
	IPW60R099	600 V, 38 A	7.06	4	7	—	2	—	2	—	2	4	4	4	—
Gate driver	HCPL-3120	—	4.98	13	10	19	11	12	10	10	9	11	9	13	10
Diode	FFPF30UP20STU	200 V, 30 A	1.99	—	4	—	—	—	1	4	8	2	3	—	2
Capacitors	ESMQ161VSN102MQ30S	160 V, 1000 uF	3.12	3	4	3	1	1	1	2	2	2	3	3	2
	B43416C3108A000	300 V, 1000 uF	7.35	—	—	—	2	1	1	1	2	2	—	—	1
	ALF20G102EP500	500 V, 1000 uF	13.84	—	—	—	—	—	—	—	—	—	1	—	—
			Total cost ($)	128	133	159	125	119	106	115	133	144	120	133	112

[a]*The prices may vary based on market growth and availability.*

high for topologies (Hinago and Koizumi, 2012; Taghvaie and Adabi, 2018; Jakkula et al., 2022), resulting in higher power losses.

iv) Furthermore, the cost function (C_f) is formulated as follows.

$$C_f = \left(N_{sh} + N_{dv} + N_d + N_{cp}\right) + \alpha \times TSV_{p.u.} \quad (34)$$

and compared with all other topologies. The cost function is calculated with weight factors α = 0.5, 1, and 1.5, and the respective values are listed in **Table 2**. The cost function of the proposed topology is slightly higher than the topologies presented in (Iqbal et al., 2021; Chen et al., 2022) and less than all other topologies.

v) The approximate cost of the topologies in USD has been calculated and is listed in **Table 3**. To ensure a fair comparison, all topologies were considered with the goal of producing an output voltage of 400 V, and component ratings were chosen as shown in **Table 3**. From **Table 3**, it is clear that the cost of the proposed topology is the least, except for the topology presented in Iqbal et al. (2021).

The main advantage of the proposed topology is the suppression of leakage current due to its direct connection between the negative terminal of the source side and the neutral of the load side. This common ground connection feature is absent in all other structures except (Chen et al., 2022) listed in **Table 2**.

CONCLUSION

This study presented a nine-level inverter with leakage current suppression, voltage boosting, self-voltage balancing, and low voltage stress on capacitors based on a single-phase switching capacitor. The CG feature suppresses the leakage current, making the proposed topology suitable for the transformerless application. The functioning of the proposed topology and capacitance calculation has been discussed. A comprehensive comparison based on power components and capacitor voltage highlights the advantages of the recommended design over the other nine-level topologies. In addition, a complete cost examination confirmed the planned topology's cost efficiency. The modelling and experimental findings showed that the suggested topology may be implemented under various dynamic operating circumstances without affecting the switched capacitors. Simulation yields a maximum efficiency of ~97.3 % at 400 W, with a measured result of 96.2%. The suggested topology qualifies as a possible contender for grid-connected photovoltaic application due to the advantages discussed throughout this research.

DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/Supplementary Material; further inquiries can be directed to the corresponding author.

AUTHOR CONTRIBUTIONS

NG: conceived the idea, designed the experiments, and wrote the manuscript. KV: supervision, formal analysis, review and editing, and validation. Both authors read and approved the final manuscript.

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